



## Connection Diagrams



FIGURE 2.

## Ordering Information

Ordering Number	Package Type	NSC Package Drawing	Supplied As
LM5109AMA	SOIC-8	M08A	95 Units in anti static rails
LM5109AMAX	SOIC-8	M08A	2500 Units on Tape & Reel
LM5109ASD	LLP-8	SDC08A	1000 Units on Tape & Reel
LM5109ASDX	LLP-8	SDC08A	4500 Units on Tape & Reel

## Pin Descriptions

Pin #		Name	Description	Application Information
SO-8	LLP-8			
1	1	V <sub>DD</sub>	Positive gate drive supply	Locally decouple to V <sub>SS</sub> using low ESR/ESL capacitor located as close to IC as possible.
2	2	HI	High side control input	The HI input is compatible with TTL input thresholds. Unused HI input should be tied to ground and not left open
3	3	LI	Low side control input	The LI input is compatible with TTL input thresholds. Unused LI input should be tied to ground and not left open.
4	4	V <sub>SS</sub>	Ground reference	All signals are referenced to this ground.
5	5	LO	Low side gate driver output	Connect to the gate of the low-side N-MOS device.
6	6	HS	High side source connection	Connect to the negative terminal of the bootstrap capacitor and to the source of the high-side N-MOS device.
7	7	HO	High side gate driver output	Connect to the gate of the high-side N-MOS device.
8	8	HB	High side gate driver positive supply rail	Connect the positive terminal of the bootstrap capacitor to HB and the negative terminal of the bootstrap capacitor to HS. The bootstrap capacitor should be placed as close to IC as possible.

Note: For LLP-8 package it is recommended that the exposed pad on the bottom of the package be soldered to ground plane on the PCB and the ground plane should extend out from underneath the package to improve heat dissipation.

**Absolute Maximum Ratings** (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

$V_{DD}$ to $V_{SS}$	-0.3V to 18V
HB to HS	-0.3V to 18V
LI or HI to $V_{SS}$	-0.3V to $V_{DD} + 0.3V$
LO to $V_{SS}$	-0.3V to $V_{DD} + 0.3V$
HO to $V_{SS}$	$V_{HS} - 0.3V$ to $V_{HB} + 0.3V$
HS to $V_{SS}$ (Note 6)	-5V to 90V
HB to $V_{SS}$	108V
Junction Temperature	-40°C to +150°C

Storage Temperature Range -55°C to +150°C

ESD Rating HBM (Note 2) 1.5 kV

**Recommended Operating Conditions**

$V_{DD}$	8V to 14V
HS (Note 6)	-1V to 90V
HB	$V_{HS} + 8V$ to $V_{HS} + 14V$
HS Slew Rate	< 50 V/ns
Junction Temperature	-40°C to +125°C

**Electrical Characteristics**

Specifications in standard typeface are for  $T_J = +25^\circ\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12V$ ,  $V_{SS} = V_{HS} = 0V$ , No Load on LO or HO (Note 4).

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>SUPPLY CURRENTS</b>						
$I_{DD}$	$V_{DD}$ Quiescent Current	LI = HI = 0V		0.3	<b>0.6</b>	mA
$I_{DDO}$	$V_{DD}$ Operating Current	f = 500 kHz		1.8	<b>2.9</b>	mA
$I_{HB}$	Total HB Quiescent Current	LI = HI = 0V		0.06	<b>0.2</b>	mA
$I_{HBO}$	Total HB Operating Current	f = 500 kHz		1.4	<b>2.8</b>	mA
$I_{HBS}$	HB to $V_{SS}$ Current, Quiescent	$V_{HS} = V_{HB} = 90V$		0.1	<b>10</b>	$\mu\text{A}$
$I_{HBSO}$	HB to $V_{SS}$ Current, Operating	f = 500 kHz		0.5		mA
<b>INPUT PINS LI and HI</b>						
$V_{IL}$	Low Level Input Voltage Threshold		<b>0.8</b>	1.8		V
$V_{IH}$	High Level Input Voltage Threshold			1.8	<b>2.2</b>	V
$R_I$	Input Pulldown Resistance		<b>100</b>	200	<b>500</b>	k $\Omega$
<b>UNDER VOLTAGE PROTECTION</b>						
$V_{DDR}$	$V_{DD}$ Rising Threshold	$V_{DDR} = V_{DD} - V_{SS}$	<b>6.0</b>	6.7	<b>7.4</b>	V
$V_{DDH}$	$V_{DD}$ Threshold Hysteresis			0.5		V
$V_{HBR}$	HB Rising Threshold	$V_{HBR} = V_{HB} - V_{HS}$	<b>5.7</b>	6.6	<b>7.1</b>	V
$V_{HBH}$	HB Threshold Hysteresis			0.4		V
<b>LO GATE DRIVER</b>						
$V_{OLL}$	Low-Level Output Voltage	$I_{LO} = 100\text{ mA}$ $V_{OHL} = V_{LO} - V_{SS}$		0.38	<b>0.65</b>	V
$V_{OHL}$	High-Level Output Voltage	$I_{LO} = -100\text{ mA}$ , $V_{OHL} = V_{DD} - V_{LO}$		0.72	<b>1.20</b>	V
$I_{OHL}$	Peak Pullup Current	$V_{LO} = 0V$		1.0		A
$I_{OLL}$	Peak Pulldown Current	$V_{LO} = 12V$		1.0		A
<b>HO GATE DRIVER</b>						
$V_{OLH}$	Low-Level Output Voltage	$I_{HO} = 100\text{ mA}$ $V_{OLH} = V_{HO} - V_{HS}$		0.38	<b>0.65</b>	V
$V_{OHH}$	High-Level Output Voltage	$I_{HO} = -100\text{ mA}$ $V_{OHH} = V_{HB} - V_{HO}$		0.72	<b>1.20</b>	V
$I_{OHH}$	Peak Pullup Current	$V_{HO} = 0V$		1.0		A
$I_{OLH}$	Peak Pulldown Current	$V_{HO} = 12V$		1.0		A
<b>THERMAL RESISTANCE</b>						
$\theta_{JA}$	Junction to Ambient	SOIC-8 (Note 3), (Note 5)		160		°C/W
		LLP-8 (Note 3), (Note 5)		40		

## Switching Characteristics

Specifications in standard typeface are for  $T_J = +25^\circ\text{C}$ , and those in **boldface type** apply over the full **operating junction temperature range**. Unless otherwise specified,  $V_{DD} = V_{HB} = 12\text{V}$ ,  $V_{SS} = V_{HS} = 0\text{V}$ , No Load on LO or HO.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
<b>LM5109A</b>						
$t_{LPHL}$	Lower Turn-Off Propagation Delay (LI Falling to LO Falling)			30	<b>56</b>	ns
$t_{HPHL}$	Upper Turn-Off Propagation Delay (HI Falling to HO Falling)			30	<b>56</b>	ns
$t_{LPLH}$	Lower Turn-On Propagation Delay (LI Rising to LO Rising)			32	<b>56</b>	ns
$t_{HPLH}$	Upper Turn-On Propagation Delay (HI Rising to HO Rising)			32	<b>56</b>	ns
$t_{MON}$	Delay Matching: Lower Turn-On and Upper Turn-Off			2	<b>15</b>	ns
$t_{MOFF}$	Delay Matching: Lower Turn-Off and Upper Turn-On			2	<b>15</b>	ns
$t_{RC}, t_{FC}$	Either Output Rise/Fall Time	$C_L = 1000\text{ pF}$		15	-	ns
$t_{PW}$	Minimum Input Pulse Width that Changes the Output			50		ns

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

**Note 2:** The human body model is a 100 pF capacitor discharged through a 1.5k $\Omega$  resistor into each pin.

**Note 3:** 4 layer board with Cu finished thickness 1.5/1/1/1.5 oz. Maximum die size used. 5x body length of Cu trace on PCB top. 50 x 50mm ground and power planes embedded in PCB. See Application Note AN-1187.

**Note 4:** Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

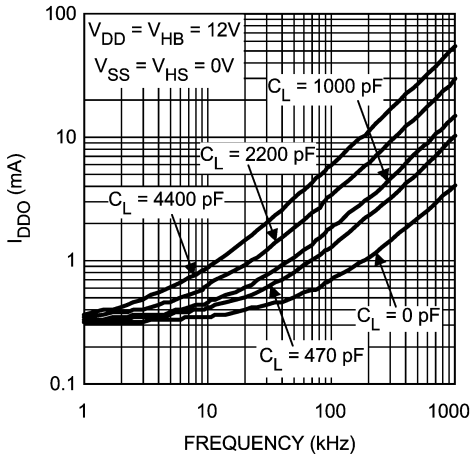
**Note 5:** The  $\theta_{JA}$  is not a constant for the package and depends on the printed circuit board design and the operating conditions.

**Note 6:** In the application the HS node is clamped by the body diode of the external lower N-MOSFET, therefore the HS voltage will generally not exceed -1V. However in some applications, board resistance and inductance may result in the HS node exceeding this stated voltage transiently.

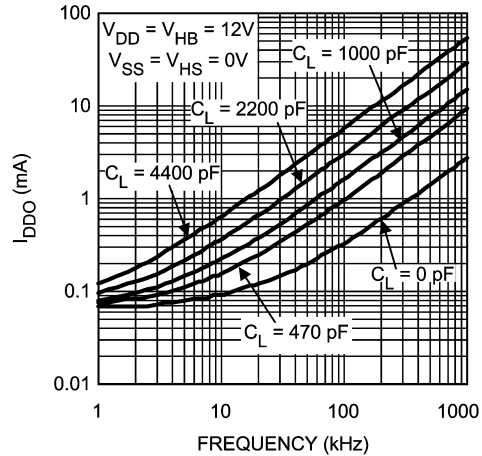
If negative transients occur on HS, the HS voltage must never be more negative than  $V_{DD} - 15\text{V}$ . For example, if  $V_{DD} = 10\text{V}$ , the negative transients at HS must not exceed -5V.

# Typical Performance Characteristics

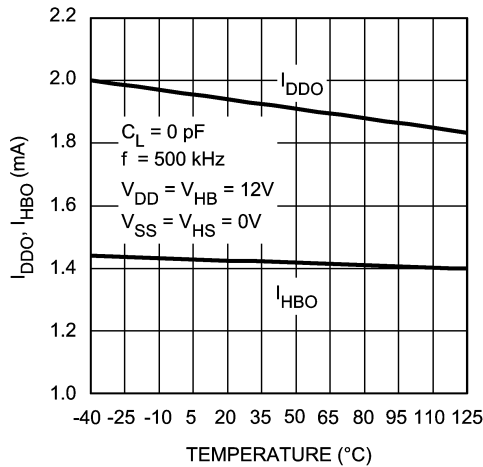
**V<sub>DD</sub> Operating Current vs Frequency**



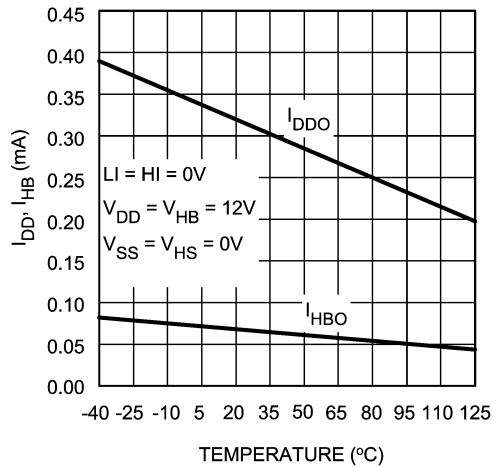
**HB Operating Current vs Frequency**



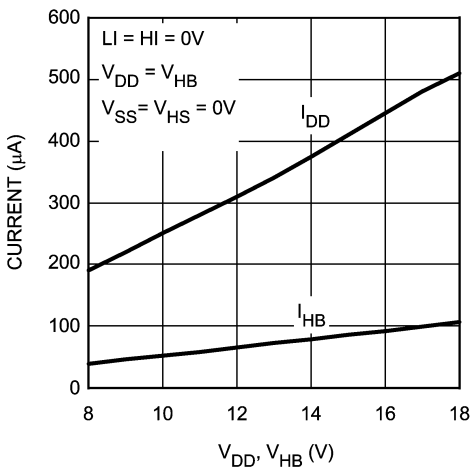
**Operating Current vs Temperature**



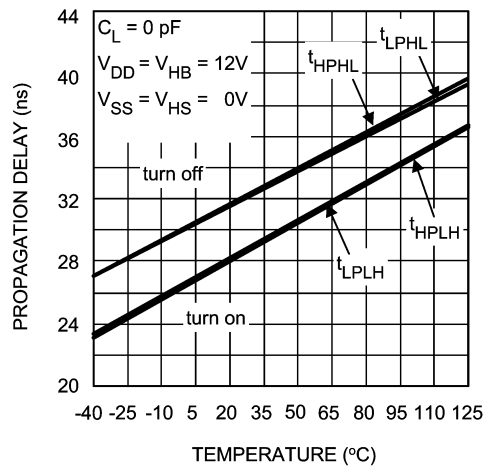
**Quiescent Current vs Temperature**



**Quiescent Current vs Voltage**

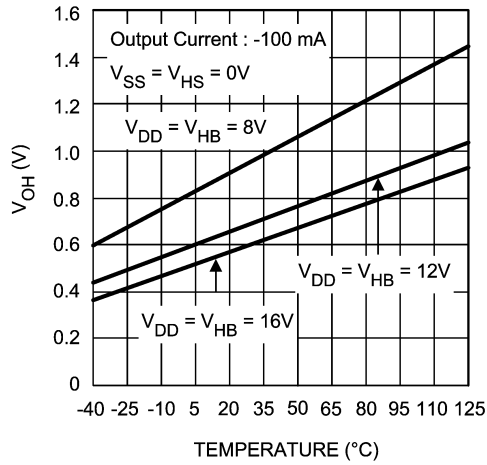


**Propagation Delay vs Temperature**



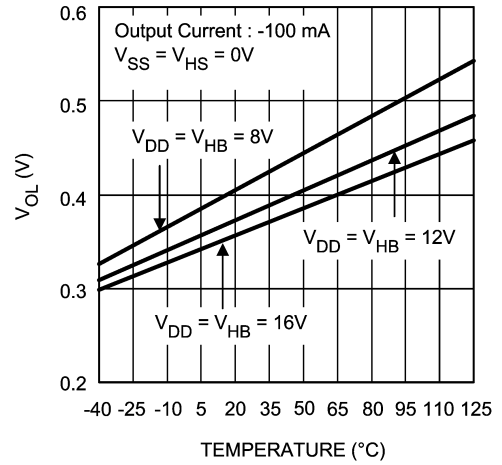
# Typical Performance Characteristics (Continued)

LO and HO High Level Output Voltage vs Temperature



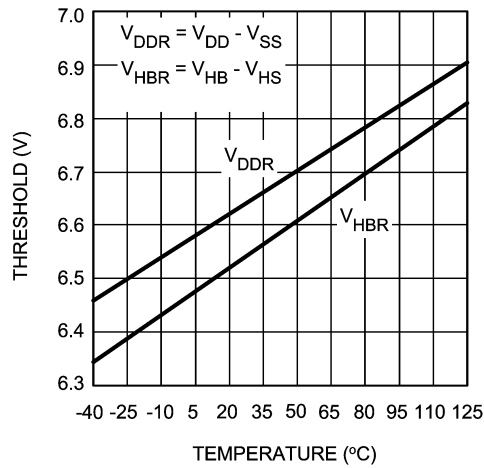
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LO and HO Low Level Output Voltage vs Temperature



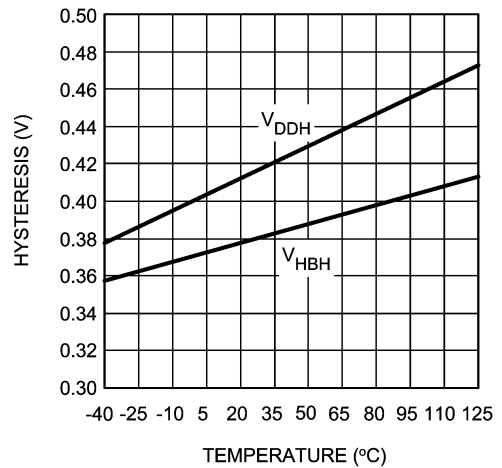
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Undervoltage Rising Thresholds vs Temperature



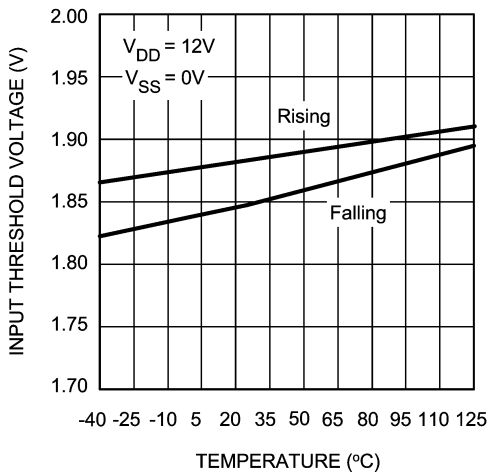
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Undervoltage Hysteresis vs Temperature



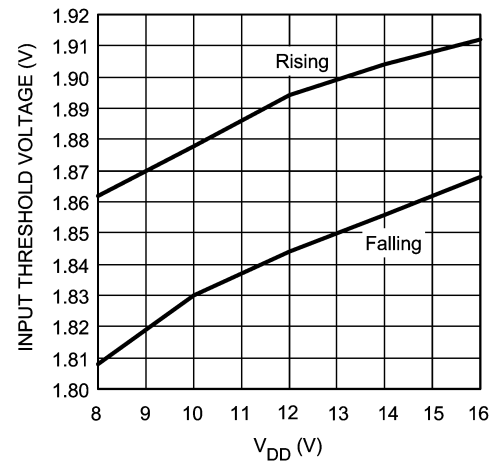
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Input Thresholds vs Temperature



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Input Thresholds vs Supply Voltage



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## Timing Diagram

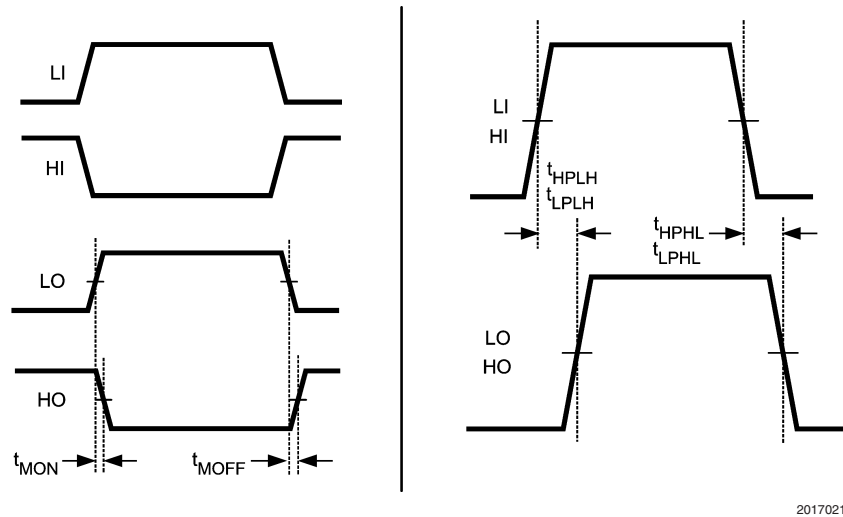


FIGURE 3.

## Layout Considerations

Optimum performance of high and low-side gate drivers cannot be achieved without taking due considerations during circuit board layout. The following points are emphasized:

1. Low ESR / ESL capacitors must be connected close to the IC between VDD and VSS pins and between HB and HS pins to support high peak currents being drawn from VDD and HB during the turn-on of the external MOSFETs.
2. To prevent large voltage transients at the drain of the top MOSFET, a low ESR electrolytic capacitor and a good quality ceramic capacitor must be connected between the MOSFET drain and ground (VSS).
3. In order to avoid large negative transients on the switch node (HS) pin, the parasitic inductances between the source of the top MOSFET and the drain of the bottom MOSFET (synchronous rectifier) must be minimized.
4. Grounding considerations:
  - a) The first priority in designing grounding connections is to confine the high peak currents that charge and discharge the MOSFET gates to a minimal physical area. This will decrease the loop inductance and minimize noise issues on the gate terminals of the MOSFETs. The gate driver should be placed as close as possible to the MOSFETs.
  - b) The second consideration is the high current path that includes the bootstrap capacitor, the bootstrap diode, the local ground referenced bypass capacitor, and the low-side MOSFET body diode. The bootstrap capacitor is recharged on a cycle-by-cycle basis through the bootstrap diode from the ground referenced VDD bypass capacitor. The recharging occurs in a short time interval

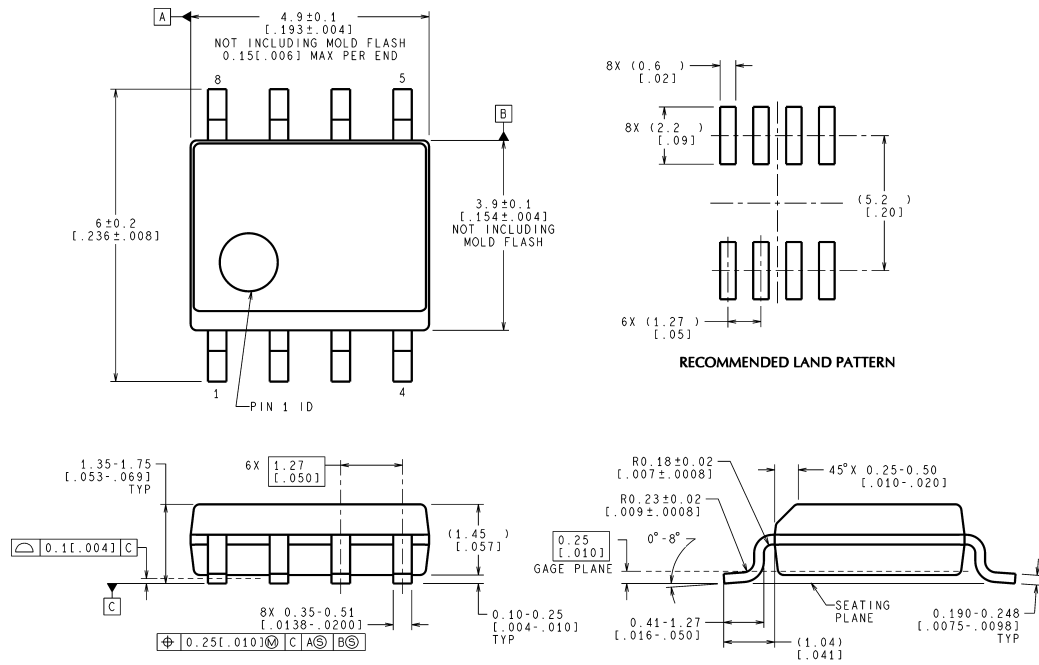
and involves high peak current. Minimizing this loop length and area on the circuit board is important to ensure reliable operation.

## HS Transient Voltages Below Ground

The HS node will always be clamped by the body diode of the lower external FET. In some situations, board resistances and inductances can cause the HS node to transiently swing several volts below ground. The HS node can swing below ground provided:

1. HS must always be at a lower potential than HO. Pulling HO more than -0.3V below HS can activate parasitic transistors resulting in excessive current flow from the HB supply, possibly resulting in damage to the IC. The same relationship is true with LO and VSS. If necessary, a Schottky diode can be placed externally between HO and HS or LO and GND to protect the IC from this type of transient. The diode must be placed as close to the IC pins as possible in order to be effective.
2. HB to HS operating voltage should be 15V or less. Hence, if the HS pin transient voltage is -5V, VDD should be ideally limited to 10V to keep HB to HS below 15V.
3. Low ESR bypass capacitors from HB to HS and from VDD to VSS are essential for proper operation. The capacitor should be located at the leads of the IC to minimize series inductance. The peak currents from LO and HO can be quite large. Any series inductances with the bypass capacitor will cause voltage ringing at the leads of the IC which must be avoided for reliable operation.

# Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS MILLIMETER  
VALUES IN [ ] ARE INCHES  
DIMENSIONS IN ( ) FOR REFERENCE ONLY

M08A (Rev K)

Controlling dimension is inch. Values in [ ] are millimeters.

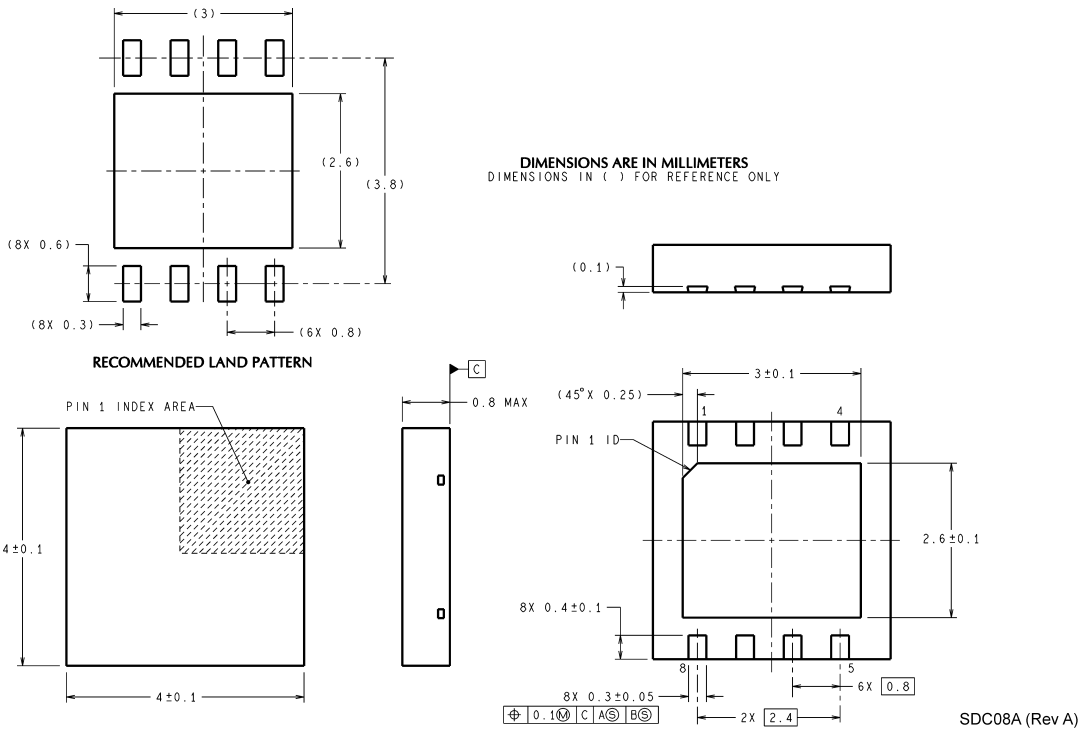
Notes: Unless otherwise specified.

1. Standard lead finish to be 200 micrometers/5.08 micrometers minimum lead/tin (solder) on copper.
2. Dimension does not include mold flash.
3. Reference JEDEC registration MS-012, Variation AA, dated May 1990.

## SOIC-8 Outline Drawing NS Package Number M08A



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



Notes: Unless otherwise specified.

1. For solder thickness and composition, see "Solder Information" in the packaging section of the National Semiconductor web page ([www.national.com](http://www.national.com)).
2. Maximum allowable metal burr on lead tips at the package edges is 76 microns.
3. No JEDEC registration as of May 2003.

**LLP-8 Outline Drawing  
NS Package Number SDC08A**

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