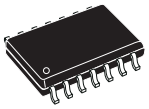
L6386AD

High-voltage high and low side driver

Features

- High voltage rail up to 600 V
- dV/dt immunity ±50 V/nsec in full temperature range
- Driver current capability:
  - 400 mA source,
  - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1nF load
- CMOS/TTL Schmitt trigger inputs with hysteresis and pull down
- Under voltage lock out on lower and upper driving section
- Integrated bootstrap diode
- Outputs in phase with inputs

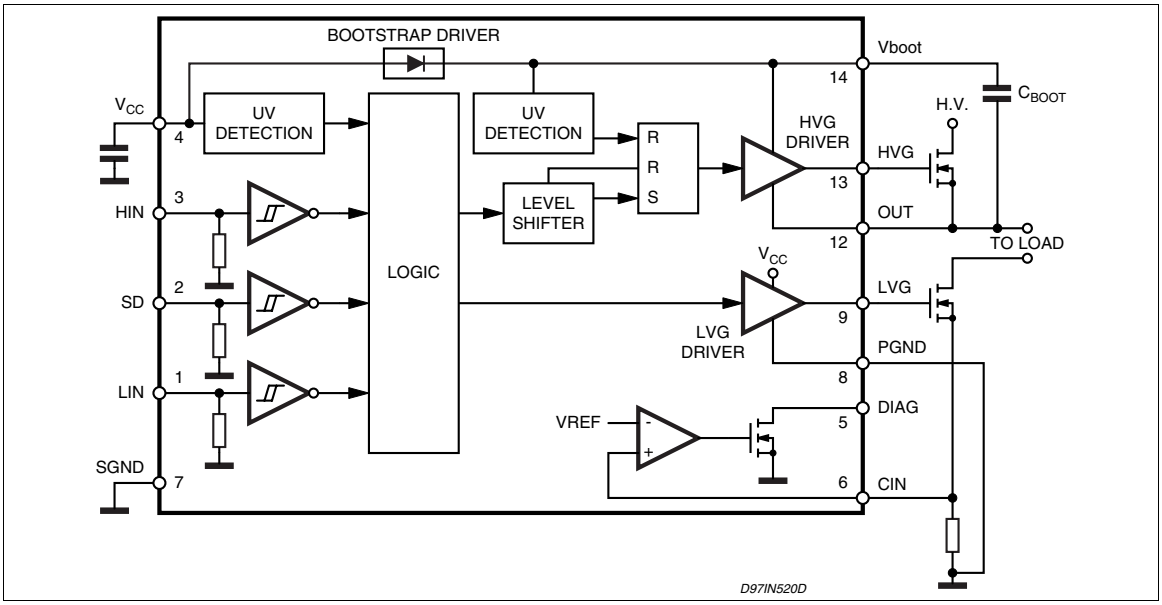


SO-14

Description

The L6386AD is an high-voltage device, manufactured with the BCD "OFF-LINE" technology. It has a driver structure that enables to drive independent referenced Channel Power MOS or IGBT. The high-side (floating) section is enabled to work with voltage rail up to 600 V. The Logic Inputs are CMOS/TTL compatible for ease of interfacing with controlling devices.

Figure 1. Block diagram



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Contents

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1 Electrical data

1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{out}	Output voltage	-3 to V_{boot} - 18	V
V_{cc}	Supply voltage	- 0.3 to +18	V
V_{boot}	Floating supply voltage	-1 to 618	V
V_{hvg}	High-side gate output voltage	- 1 to V_{boot}	V
V_{lvg}	Low-side gate output voltage	-0.3 to V_{cc} +0.3	V
V_i	Logic input voltage	-0.3 to V_{cc} +0.3	V
V_{diag}	Open drain forced voltage	-0.3 to V_{cc} +0.3	V
V_{cin}	Comparator input voltage	-0.3 to 10 V	V
dV_{out}/dt	Allowed output slew rate	50	V/ns
P_{tot}	Total power dissipation (T_J = 85 °C)	750	mW
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-50 to 150	°C

Note: ESD immunity for pins 12, 13 and 14 is guaranteed up to 900V (Human Body Model)

1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	SO-14	Unit
$R_{th(JA)}$	Thermal Resistance Junction to ambient	165	°C/W

1.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
V_{out}	12	Output voltage		(1)		580	V
V_{BS} (2)	14	Floating supply voltage		(1)		17	V
f_{sw}		Switching frequency	HVG,LVG load C_L = 1 nF			400	kHz
V_{cc}	4	Supply voltage				17	V
T_J		Junction temperature		-45		125	°C

1. If the condition V_{boot} - V_{out} < 18 V is guaranteed, V_{out} can range from -3 to 580 V
2. V_{BS} = V_{boot} - V_{out}

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2 Pin connection

Figure 2. Pin connection (Top view)

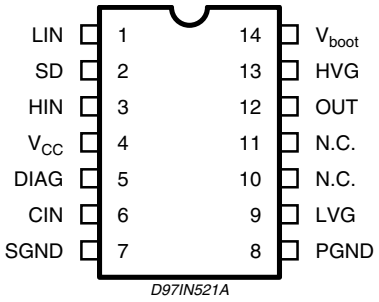

Table 4. Pin description

N°	Pin	Type	Function
1	LIN	I	Low-side driver logic input
2	SD(1)	I	Shut down logic input
3	HIN	I	High-side driver logic input
4	V_{CC}		Low voltage supply
5	DIAG	O	Open drain diagnostic output
6	CIN	I	Comparator input
7	SGND		Ground
8	PGND		Power ground
9	LVG (1)	O	Low-side driver output
10, 11	N.C.		Not connected
12	OUT	O	High-side driver floating driver
13	HVG (1)	O	High-side driver output
14	V_{boot}		Bootstrapped supply voltage

1. The circuit guarantees 0.3V maximum on the pin (@ Isink = 10 mA), with VCC >3V. This allows to omit the "bleeder" resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low; the gate driver assures low impedance also in SD condition.

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3 Electrical characteristics

3.1 AC operation

Table 5. AC operation electrical characteristcs (V_{CC} = 15 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
t_{on}	1,3 vs 9,13	High/low-side driver turn-on propagation delay	V_{out} = 0 V		110	150	ns
t_{off}		High/low-side driver turn-off propagation delay			110	150	ns
t_{sd}	2 vs 9,13	Shut down to high/low side propagation delay			105	150	
t_r	9, 13	Rise time	C_L = 1000 pF		50		ns
t_f		Fall time	C_L = 1000 pF		30		ns

3.2 DC operation

Table 6. DC operation electrical characteristcs (V_{CC} = 15 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
Low supply voltage section							
V_{ccth1}	4	V_{cc} UV turn on threshold		9.1	9.6	10.1	V
V_{ccth2}		V_{cc} UV turn off threshold		7.9	8.3	8.8	V
V_{cchys}		V_{cc} UV hysteresis			1.3		V
I_{qccu}		Undervoltage quiescent supply current	V_{cc} ≤9 V		200		µA
I_{qcc}		Quiescent current	V_{cc} = 15 V		250	320	µA
Bootstrapped supply section							
V_{bth1}	14	V_{boot} UV turn on threshold		8.5	9.5	10.5	V
V_{bth2}		V_{boot} UV turn off threshold		7.2	8.2	9.2	V
V_{bhys}		V_{boot} UV hysteresis			1.3		V
I_{qboot}		V_{boot} quiescent current	HVG ON			200	µA
I_{lk}		High voltage leakage current	Vhvg = Vout = Vboot = 600 V			10	µA
$R_{DS(on)}$		Bootstrap driver on resistance (1)	V_{cc} ≥ 12.5 V; Vin = 0 V		125		Ω

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Table 6. DC operation electrical characteristcs (continued)(V_{CC} = 15 V; T_J = 25 °C)

Symbol	Pin	Parameter	Test condition	Min	Typ	Max	Unit
Driving buffers section							
I_{so}	9, 13	High/low side source short circuit current	$V_{IN} = V_{ih}$ (t_p < 10 µs)	300	400		mA
I_{si}	9, 13	High/low side sink short circuit current	$V_{IN} = V_{il}$ (tp < 10 µs)	500	650		mA
Logic inputs							
V_{il}	1,2, 3	Low level logic voltage				1.5	V
V_{ih}		High level logic voltage		3.6			V
I_{ih}		High level logic input current	V_{IN} = 15 V		50	70	µA
I_{il}		Low level logic input current	V_{IN} = 0 V			1	µA
Sense comparator							
V_{io}		Input offset voltage		-10		10	mV
I_{io}	6	Input bias current	$V_{cin} \geq 0.5$		0.2		µA
V_{ol}	2	Open drain low level output voltage	I_{od} = -2.5 mA			0.8	V
V_{ref}		Comparator reference voltage		0.46	0.50	0.54	V

1. $R_{DS(on)}$ is tested in the following way:

$$R_{DSON} = \frac{(V_{CC} - V_{CBOOT1}) - (V_{CC} - V_{CBOOT2})}{I_1(V_{CC}, V_{CBOOT1}) - I_2(V_{CC}, V_{CBOOT2})}$$

where I_1 is pin 14 current when $V_{CBOOT} = V_{CBOOT1}$, I_2 when $V_{CBOOT} = V_{CBOOT2}$

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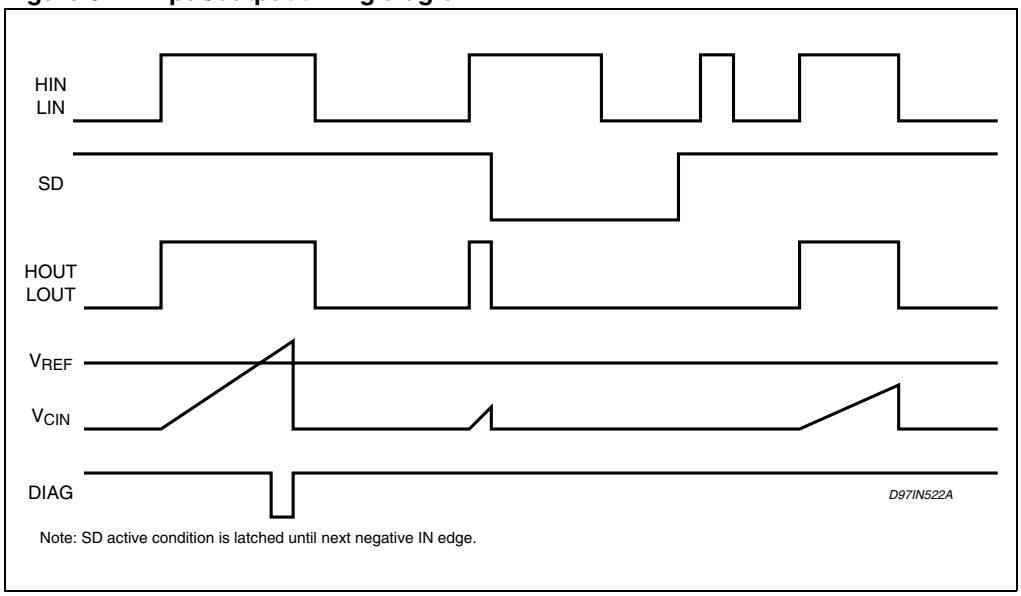
3.3 Timing diagram

Figure 3. Input/output timing diagram



Note: SD active condition is latched until next negative IN edge.

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4 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 4* a). In the L6386AD a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low side driver (LVG), with in series a diode, as shown in *Figure 4* b. An internal charge pump (*Figure 4* b) provides the DMOS driving voltage. The diode connected in series to the DMOS has been added to avoid undesirable turn on of it.

4.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOS can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOS total gate charge:

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

$$C_{BOOT} >>> C_{EXT}$$

e.g.: if Q_{gate} is 30 nC and V_{gate} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage losses.

e.g.: HVG steady state consumption is lower than 200 µA, so if HVG T_{ON} is 5ms, C_{BOOT} has to supply 1 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives great advantages: the external fast recovery diode can be avoided (it usually has great leakage current).

This structure can work only if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of the C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$ (typical value: 125 Ω). At low frequency this drop can be neglected. Anyway increasing the frequency it must be taken in to account.

The following equation is useful to compute the drop on the bootstrap DMOS:

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q_{gate} is the gate charge of the external power MOS, R_{dson} is the on resistance of the bootstrap DMOS, and T_{charge} is the charging time of the bootstrap capacitor.

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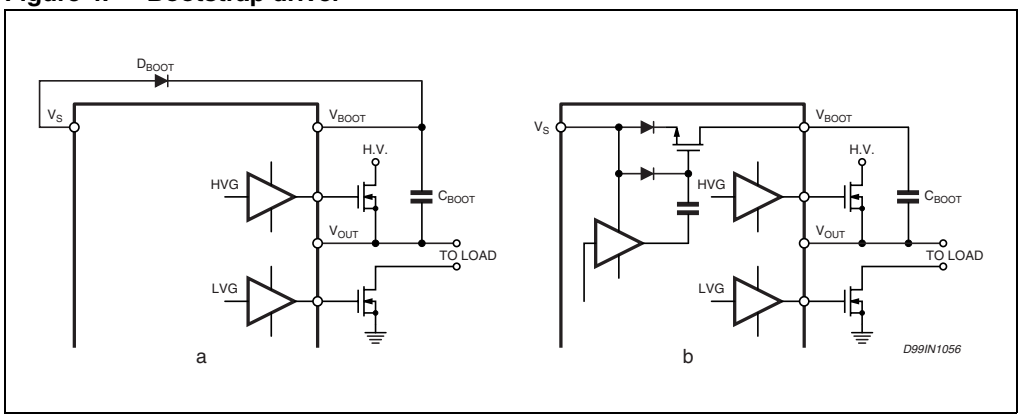
For example: using a power MOS with a total gate charge of 30 nC the drop on the bootstrap DMOS is about 1 V, if the T_{charge} is 5 µs. In fact:

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

V_{drop} has to be taken into account when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Figure 4. Bootstrap driver



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5 Typical characteristic

Figure 5. Typical rise and fall times vs load capacitance

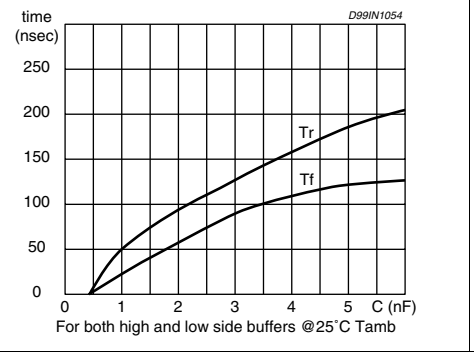

Figure 6. Quiescent current vs supply voltage

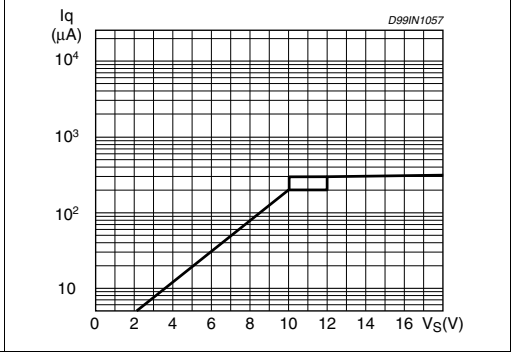

Figure 7. Turn on time vs temperature

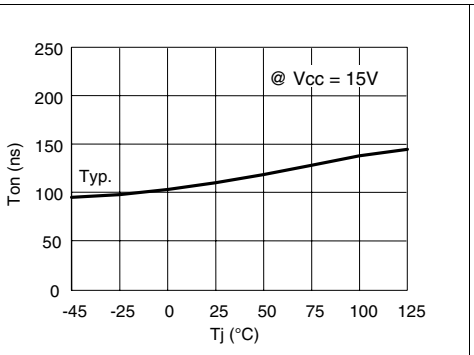

Figure 8. V_{BOOT} UV turn on threshold vs temperature

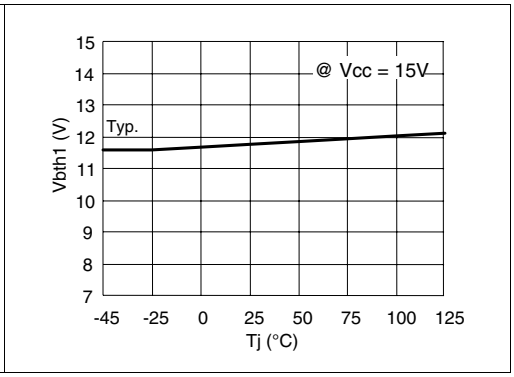

Figure 9. Turn Off time vs temperature

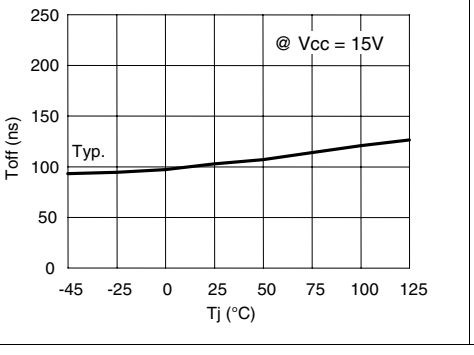

Figure 10. V_{BOOT} UV turn off threshold vs temperature

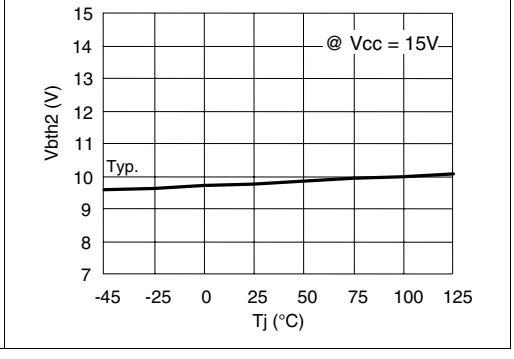

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Figure 11. Shutdown time vs temperature

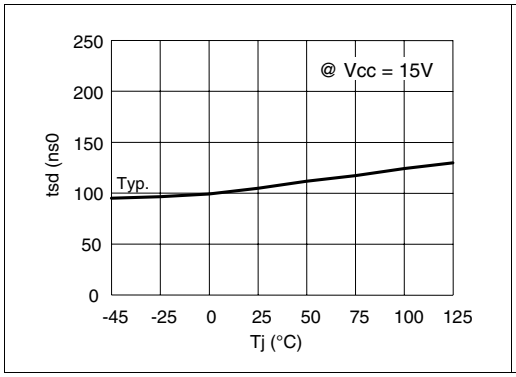

Figure 12. V_{BOOT} UV hysteresis

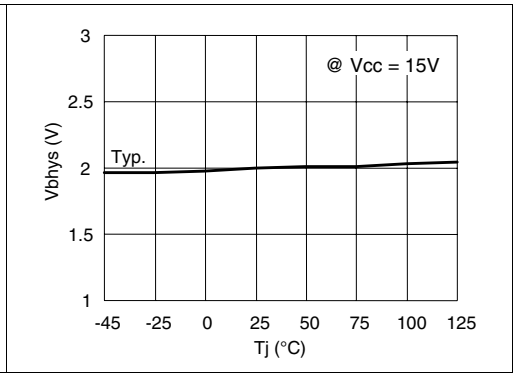

Figure 13. V_{CC} UV turn on threshold vs temperature

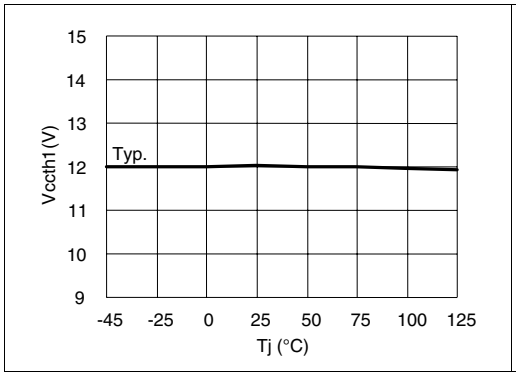

Figure 14. Output source current vs temperature

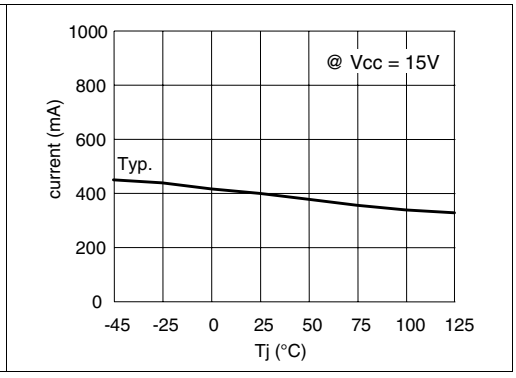

Figure 15. V_{CC} UV turn off threshold vs temperature

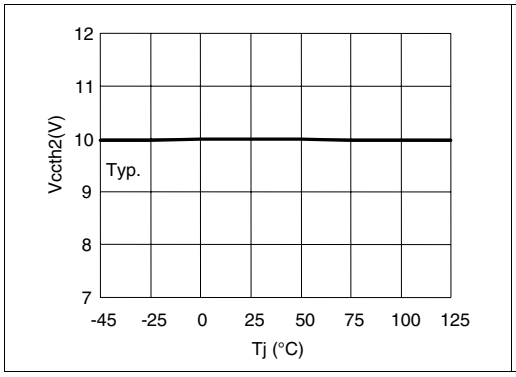

Figure 16. Output sink current vs temperature

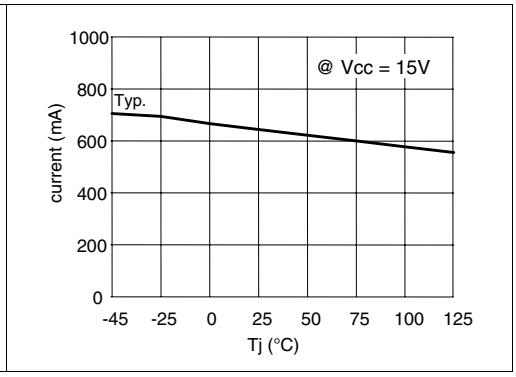

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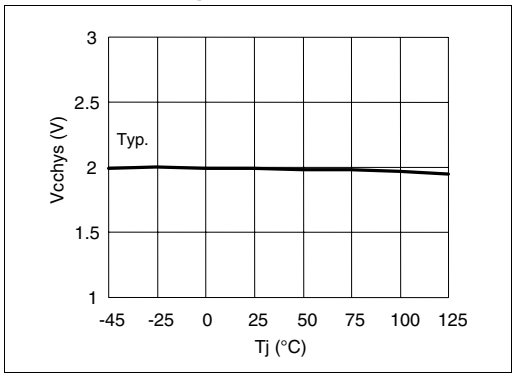
Figure 17. V_{CC} UV hysteresis vs temperature



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6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

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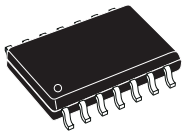
Figure 18. SO-14 mechanical data and package dimensions

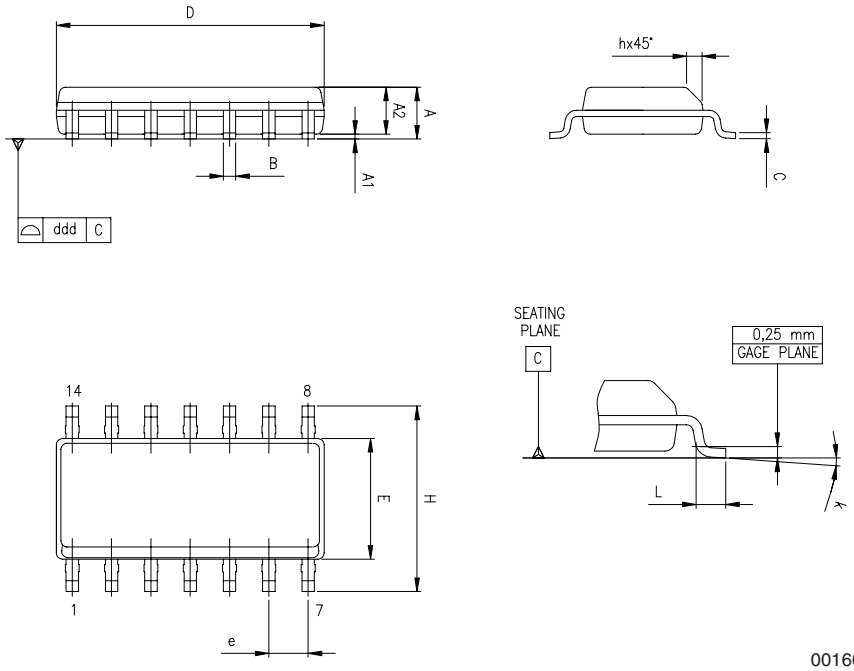
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.30	0.004		0.012
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.01
D (1)	8.55		8.75	0.337		0.344
E	3.80		4.0	0.150		0.157
e		1.27			0.050	
H	5.8		6.20	0.228		0.244
h	0.25		0.50	0.01		0.02
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

(1) "D" dimension does not include mold flash, protusions or gate burrs. Mold flash, protusions or gate burrs shall not exceed 0.15mm per side.

OUTLINE AND MECHANICAL DATA



SO-14



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7 Order codes

Table 7. Order codes

Order codes	Package	Packaging
L6386AD	SO-14	Tube
L6386AD013TR	SO-14	Tape and reel

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8 Revision history

Table 8. Document revision history

Date	Revision	Changes
14-Jul-2008	1	First release

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