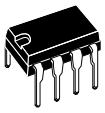
TD351

Advanced IGBT/MOSFET Driver

- **1A sink / 0.75A source min. gate drive**
- **Active Miller clamp feature**
- **Adjustable and accurate two steps turn-off level and delay**
- **Input compatible with pulse transformer or optocoupler**
- **UVLO protection**
- **2kV ESD protection**



N
DIP-8
(Plastic Package)

D
SO-8
(Plastic Micropackage)

Description

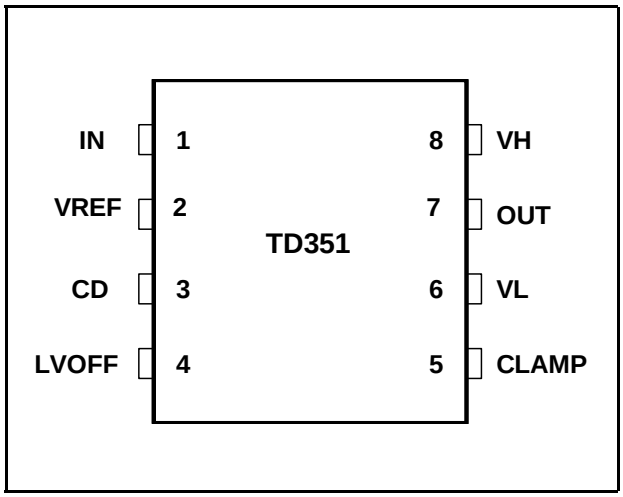
TD351 is an advanced gate driver for IGBT and power MOSFET. Control and protection functions are included and allow the design of high reliability systems

Innovative active Miller clamp function avoids the need of negative gate drive in most applications and allows the use of a simple bootstrap supply for the high side driver

TD351 includes a two-level turn-off feature with adjustable level and delay. This function protects against excessive overvoltage at turn-off in case of overcurrent or short-circuit condition. Same delay is applied at turn-on to prevent pulse width distortion.

TD351 is compatible with both pulse transformer and optocoupler signals.

Pin Connections (top view)



Applications

- **1200V 3-phase inverter**
- **Motor control systems**
- **UPS**

Order Codes

Part Number	Temperature Range	Package	Packaging	Marking
TD351IN	-40°C, +125°C	DIP	Tube	TD351I
TD351ID		SO	Tube	TD351I
TD351IDT		SO	Tape & Reel	TD351I

1 Block Diagram

Figure 1: System and internal block diagram

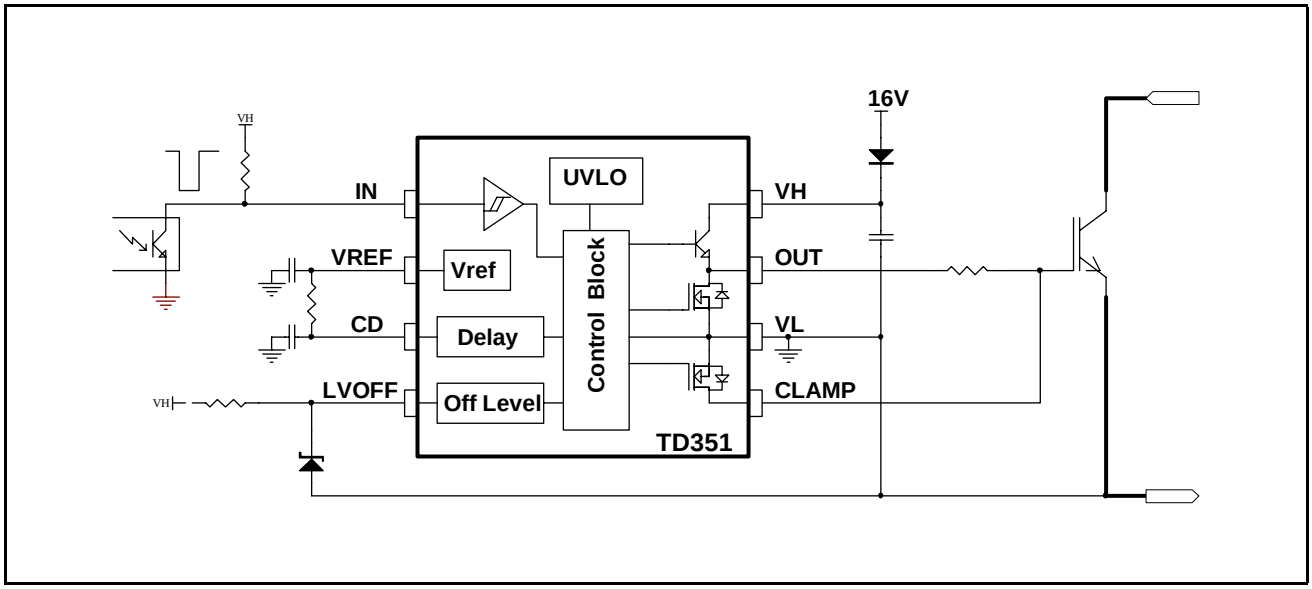


Table 1: Pin Description

Name	Pin Number	Type	Function
IN	1	Analog input	Input
VREF	2	Analog output	+5V reference voltage
CD	3	Timing capacitor	Turn on/off delay
LVOFF	4	Analog input	Turn off level
CLAMP	5	Analog output	Miller clamp
VL	6	Power supply	Signal ground
OUT	7	Analog output	Gate drive output
VH	8	Power supply	Positive supply

2 Absolute Maximum Ratings

Table 2: parameters and their absolute maximum ratings

Symbol	Parameter	Value	Unit
VHL	Maximum Supply Voltage (VH - VL)	28	V
Vout	Voltage on OUT, CLAMP, LVOFF pins	VL-0.3 to VH+0.3	V
Vter	Voltage on other pins (IN, CD, VREF)	-0.3 to 7	V
Pd	Power dissipation	500	mW
Tstg	Storage temperature	-55 to 150	°C
Tj	Maximum Junction Temperature	150	°C
Rhja	Thermal Resistance Junction-Ambient	150	°C/W
ESD	Electrostatic discharge	2	kV

Table 3: Operating Conditions

Symbol	Parameter	Value	Unit
VH	Positive Supply Voltage vs. VL	UVLO to 26	V
Toper	Operating Free Air Temperature Range	-40 to 125	°C

3 Electrical Characteristics

Table 4: Electrical characteristics for T_{amb} = -20 to 125°C, VH=16V (unless otherwise specified)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Input						
Vton	IN turn-on threshold voltage		0.8	1.0		V
Vtoff	IN turn-off threshold voltage			4.0	4.2	V
tonmin	Minimum pulse width		100	135	220	ns
Iinp	IN Input current	IN input voltage < 4.5V			1	µA
Voltage reference - Note 1						
Vref	Voltage reference	T=25°C	4.85	5.00	5.15	V
Iref	Maximum output current		10			mA
Clamp						
Vtclamp	CLAMP pin voltage threshold			2.0		V
VCL	Clamp low voltage	Icsink=500mA			2.5	V
Delay						
Vtdel	Voltage threshold			2.5		V
Rdel	Discharge resistor	I=1mA			500	Ω
Off Level						
Iblvoff	LVOFF peak input current (sink)	LVOFF=12V		90	200	µA
Violv	Offset voltage	LVOFF=12V	-0.3	-0.15	0	V
Outputs						
Isink	Output sink current	Vout=6V	1000	1700		mA
Isrc	Output source current	Vout=VH-6V	750	1300		mA
VOL1	Output low voltage 1	Iosink=20mA			0.35	V
VOL2	Output low voltage 2	Iosink=500mA			2.5	V
VOH1	Output high voltage 1	Iosource=20mA	VH-2.5			V
VOH2	Output high voltage 2	Iosource=500mA	VH-4.0			V
tr	Rise time	CL=1nF, 10% to 90%			100	ns
tf	Fall time (2 step turn-off disabled)	CL=1nF, 90% to 10%			100	ns
tdon	Turn on propagation delay	10% output change: Rd=4.7k, no Cd Rd=10k, Cd=220pF	 1.8	 2.0	 600 2.2	 ns µs
tdoff	Turn off propagation delay (2-level turn-off disabled)	10% output change			550	ns
Δtw	Input to output pulse distortion	10% output change, Δtw=Twout-Twin		50	100	ns
Under Voltage Lockout (UVLO)						
UVLOH	UVLO top threshold		10	11	12	V
UVLOL	UVLO bottom threshold		9	10	11	V
Vhyst	UVLO hysteresis	Vhyst=UVLOH-UVLOL	0.5	1		V
Supply current						
Iin	Quiescent current	input low, no load			2.5	mA

Note: 1.Recommended capacitor range on VREF pin is 10nF to 100nF

4 Functional Description

4.1 Input stage

TD351 input is compatible with optocouplers or pulse transformers. The input is triggered by the signal edge and allows the use of low-sized, low-cost pulse transformer. Input is active low: output is driven high when input is driven low. The IN input is internally clamped at about 5V to 7V.

When using an open collector optocoupler, the resistive pull-up resistor can be connected to either VREF or VH. Recommended pull-up resistor value with VH=16V are from 4.7k to 22k.

When driven by a pulse transformer, the input positive and negative pulse widths at the Vton and Vtoff threshold voltages must be larger than the minimum pulse width t_{onmin} (see fig. 4). This feature acts as a filter against invalid input pulses smaller than t_{onmin}.

4.2 Voltage reference

A voltage reference is used to create accurate timing for the turn-on delay with external resistor and capacitor. The same circuitry is also used for the two-level turn-off delay.

A decoupling capacitor (10nF to 100nF) on VREF pin is required to ensure good noise rejection.

4.3 Active Miller clamp:

The TD351 offers an alternative solution to the problem of the Miller current in IGBT switching applications. Instead of driving the IGBT gate to a negative voltage to increase the safety margin, the TD351 uses a dedicated CLAMP pin to control the Miller current. When the IGBT is off, a low impedance path is established between IGBT gate and emitter to carry the Miller current, and the voltage spike on the IGBT gate is greatly reduced.

During turn-off, the gate voltage is monitored and the clamp output is activated when gate voltage goes below 2V (relative to VL). The clamp voltage is VL+4V max for a Miller current up to 500mA. The clamp is disabled when the IN input is triggered again.

The CLAMP function doesn't affect the turn-off characteristic, but only keeps the gate to the low level throughout the off time. The main benefit is that negative voltage can be avoided in many cases, allowing a bootstrap technique for the high side driver supply.

4.4 Two level turn-off

During turn-off, gate voltage can be reduced to a programmable level in order to reduce the IGBT current (in the event of over-current). This action avoids both dangerous overvoltage across the IGBT, and RBSOA problems, especially at short circuit turn-off.

Turn-off (T_a) delay is programmable through external resistor R_d and capacitor C_d for accurate timing. T_a is approximately given by:

T_a (µs) = 0.7. R_d (kOhms). C_d (nF)

Turn-off delay (T_a) is also used to delay the input signal to prevent distortion of input pulse width.

The Two level turn-off sequence can be disabled by connecting LVOFF pin to VH and connecting CD pin to VREF with a 4.7k resistor.

4.5 Minimum Input ON-time

Input signals with ON-time smaller than T_a are ignored. ON-time signals larger than $T_a+2.R_{del}.C_d$ (R_{del} is the internal discharge switch resistance, C_d is the external timing capacitor) are transmitted to the output stage after the T_a delay with minimum width distortion ($\Delta T_w=T_{wout}-T_{win}$). For ON-time input signals close to T_a (between T_a and $T_a+2.R_{del}.C_d$), the 2-level duration is slightly reduced and the total output width can be smaller than the input width (see fig. 5).

4.6 Output stage

The output stage is able to sink/source 1.7A/1.3A typical at 25°C and 1.0A/0.75A min. over the full temperature range. This current capability is specified near the usual IGBT Miller plateau.

4.7 Undervoltage protection

Undervoltage detection protects the application in the event of a low VH supply voltage (during start-up or a fault situation). During undervoltage, the OUT pin is driven low (active pull-down for VH>2V, passive pull-down for VH<2V.

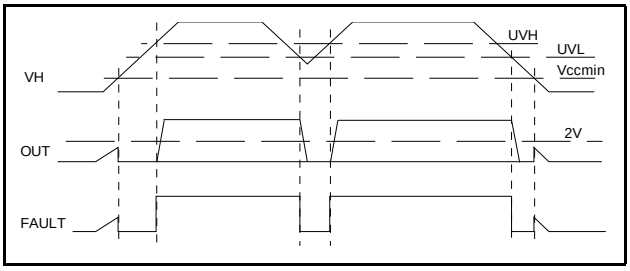
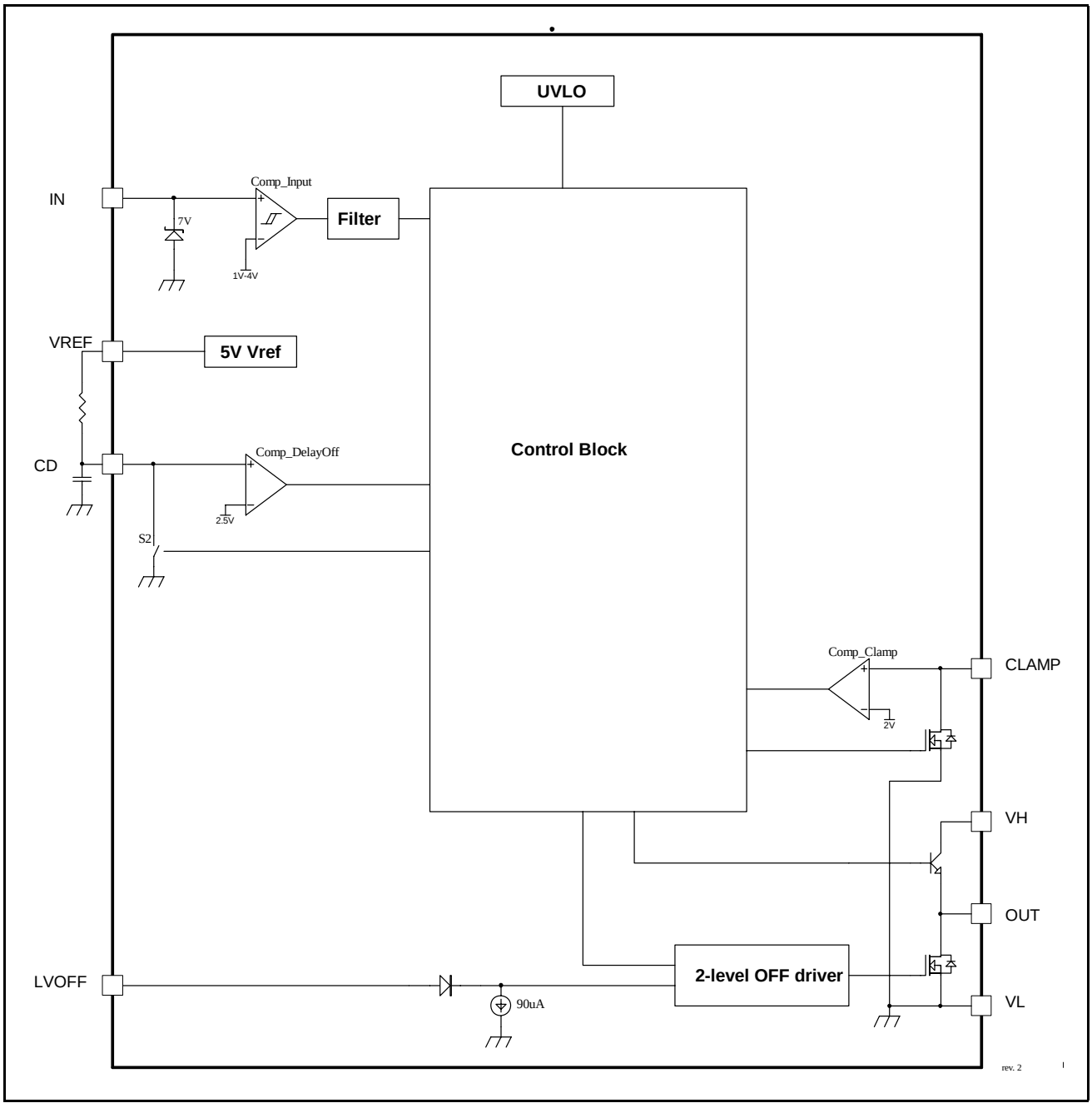


Figure 2: Detailed internal schematic



5 Timing Diagrams

Figure 3: General turn-on and 2-level turn-off sequence

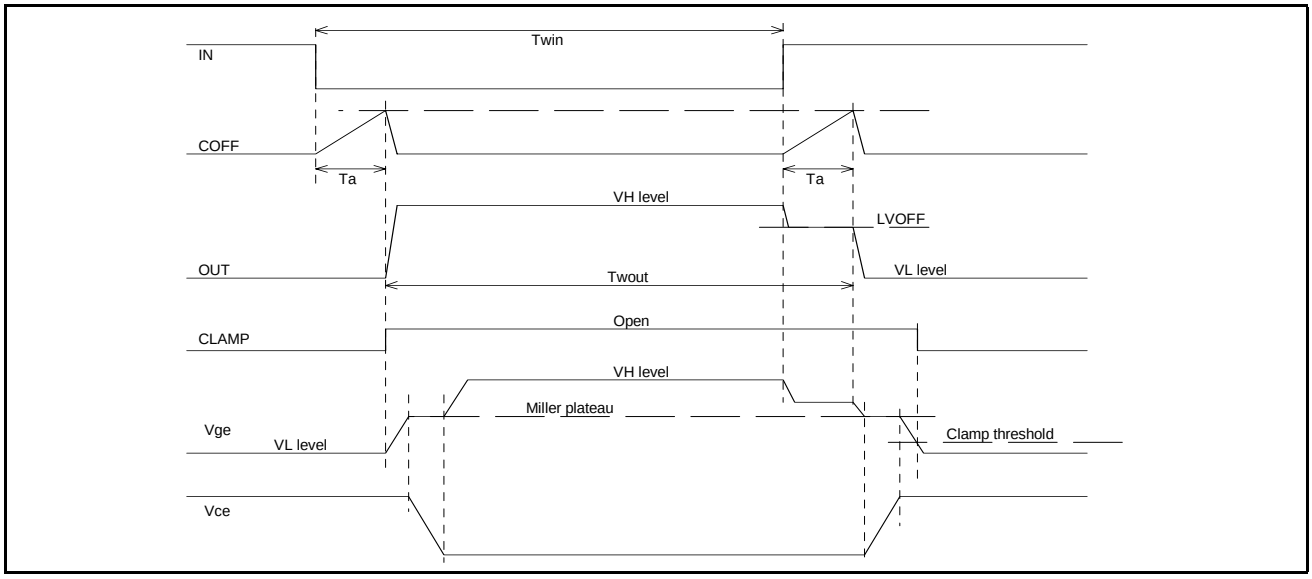


Figure 4: input and output waveform dynamic parameters

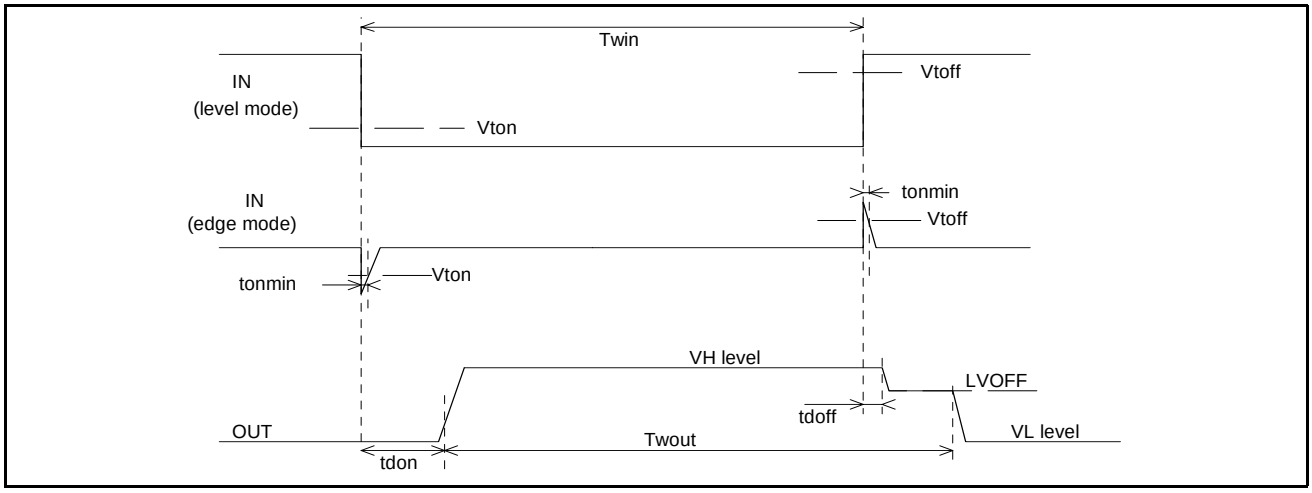
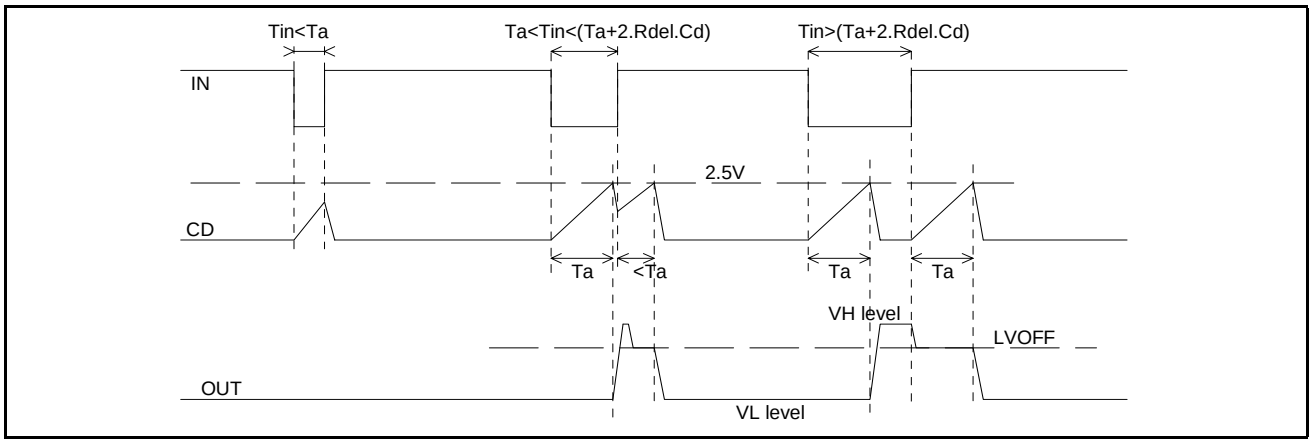


Figure 5: Minimum ON-time



6 Typical Performance Curves

Figure 6: Quiescent current vs temperature

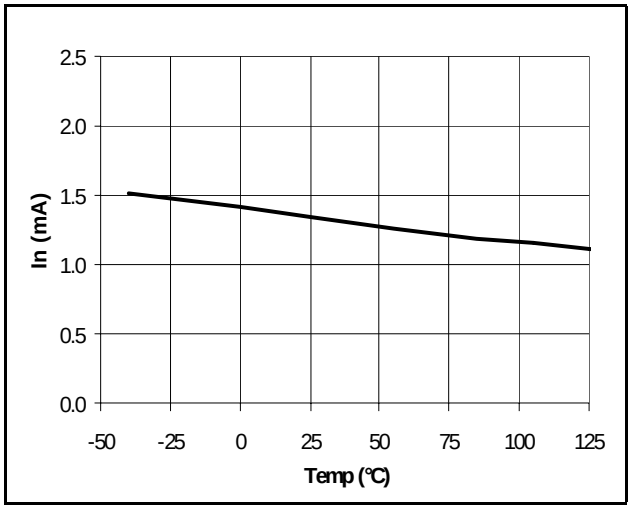


Figure 7: Low level output voltage vs temp.

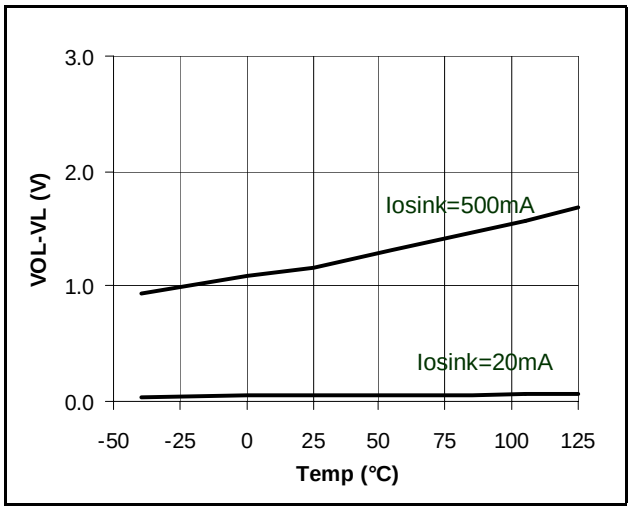


Figure 8: Sink current vs temperature

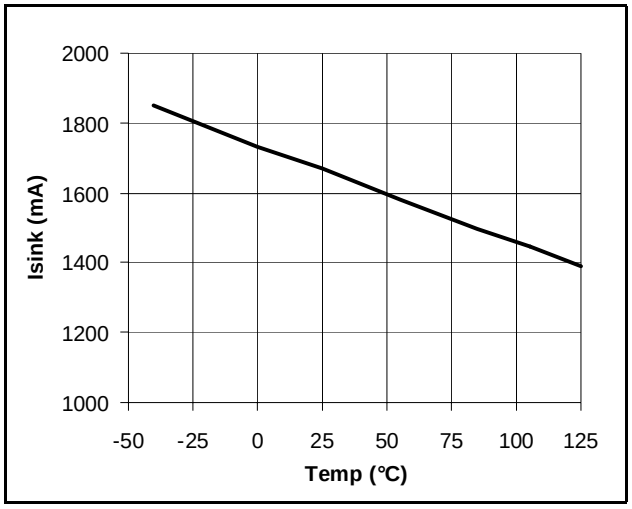


Figure 9: Rdel resistance vs temperature

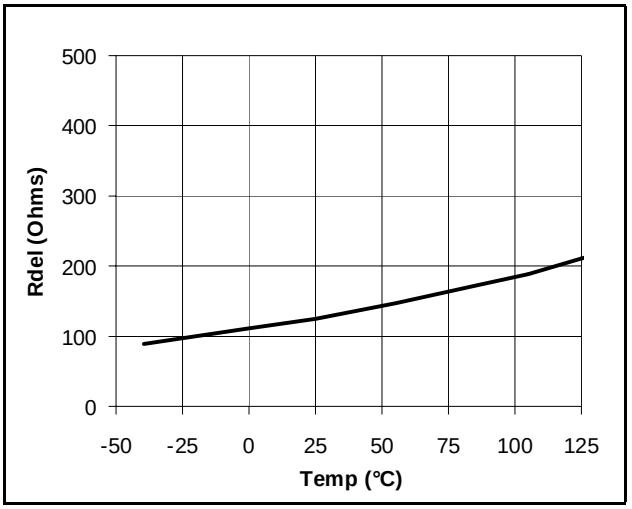


Figure 10: High level output voltage vs temp.

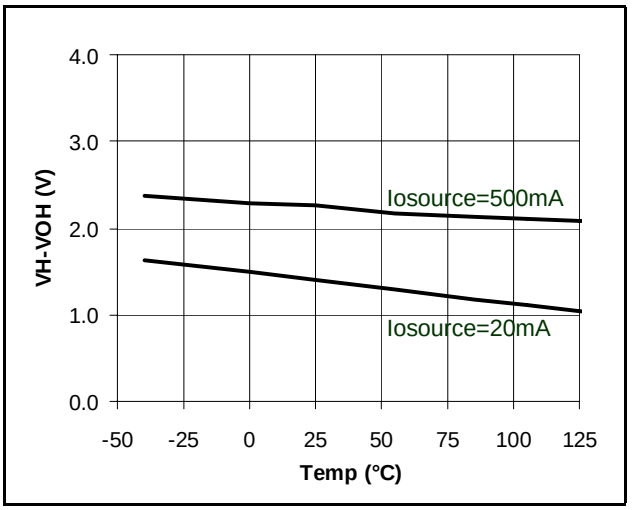
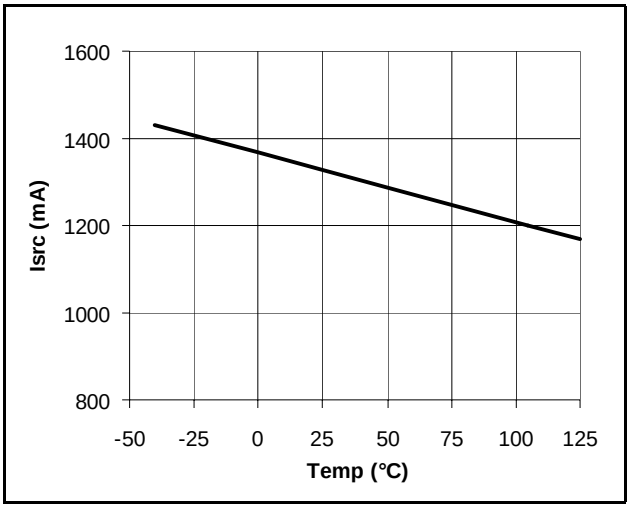


Figure 11: Source current vs temperature



7 Application Diagrams

Figure 12: Single supply IGBT drive with active Miller clamp

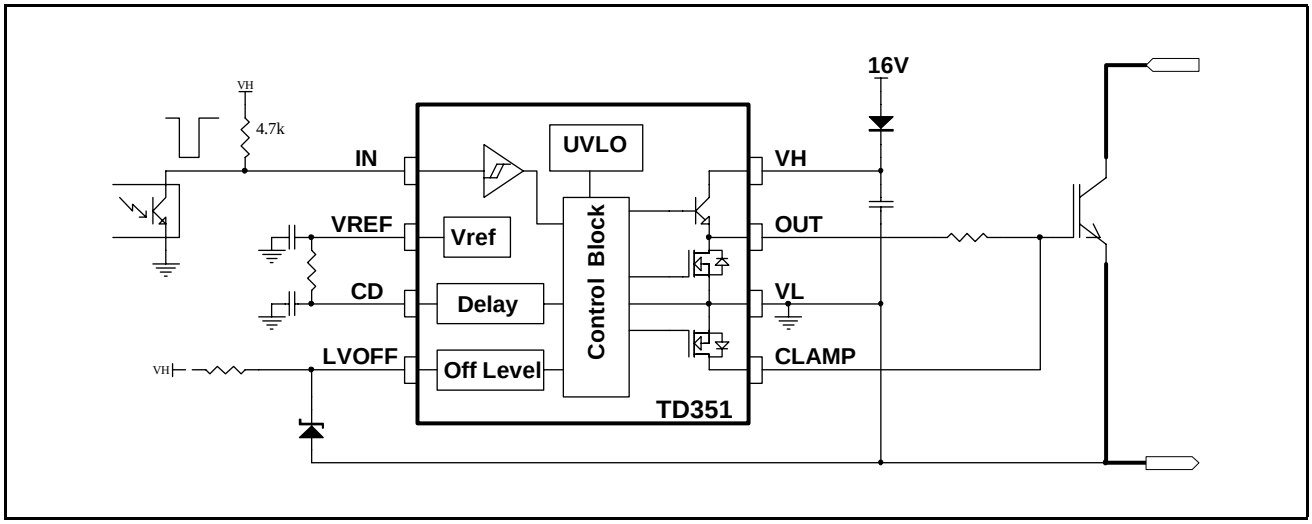


Figure 13: Use of pulse transformer signals

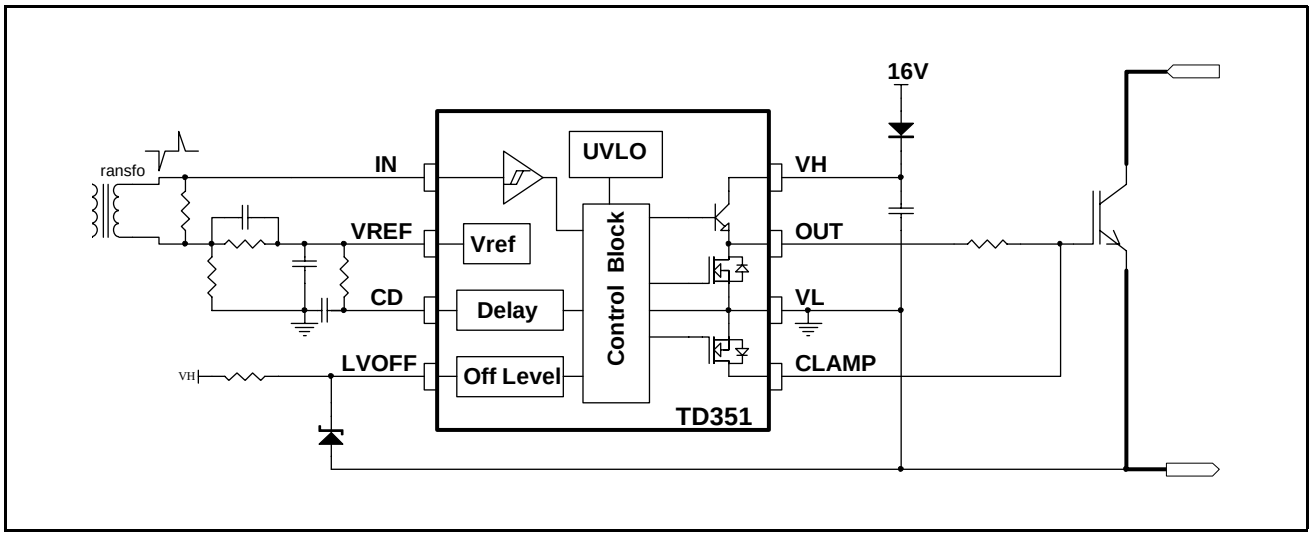
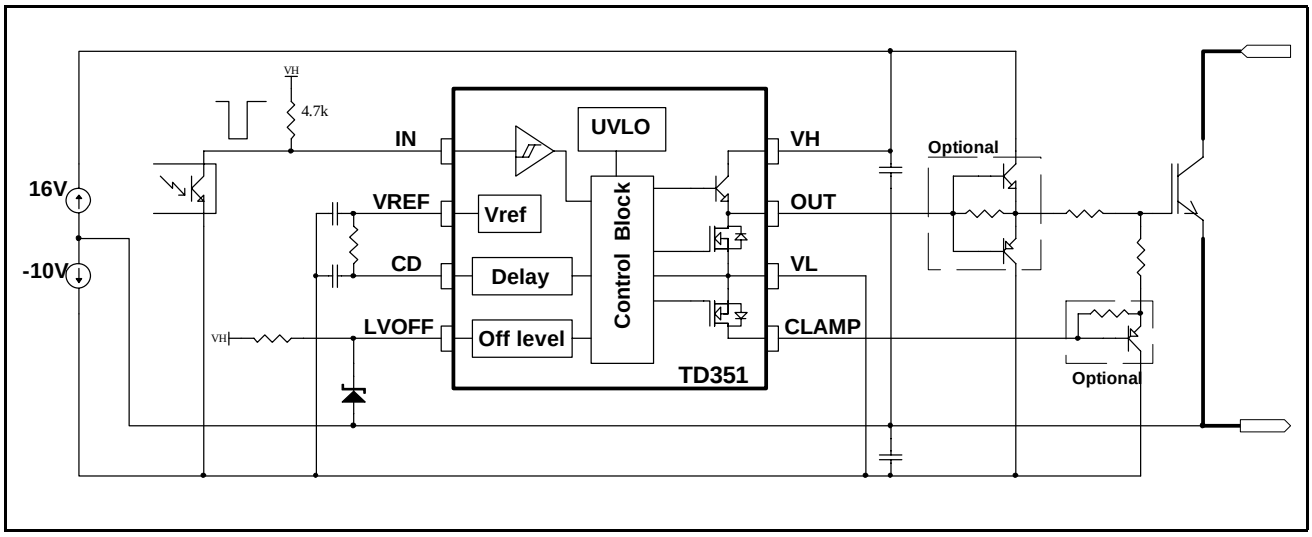


Figure 14: Large IGBT drive with negative voltage gate drive and optional current buffers

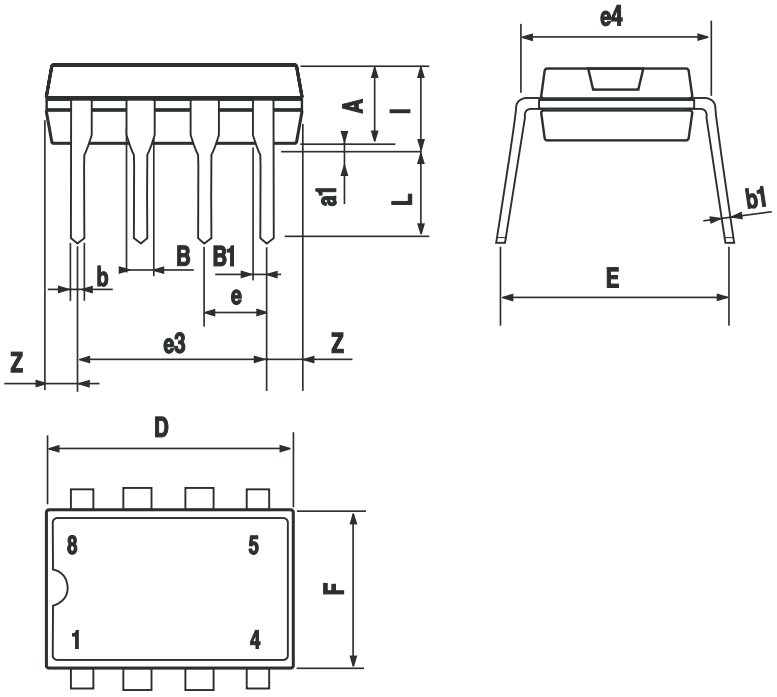


8 Package Mechanical Data

8.1 DIP-8 Package

Plastic DIP-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063



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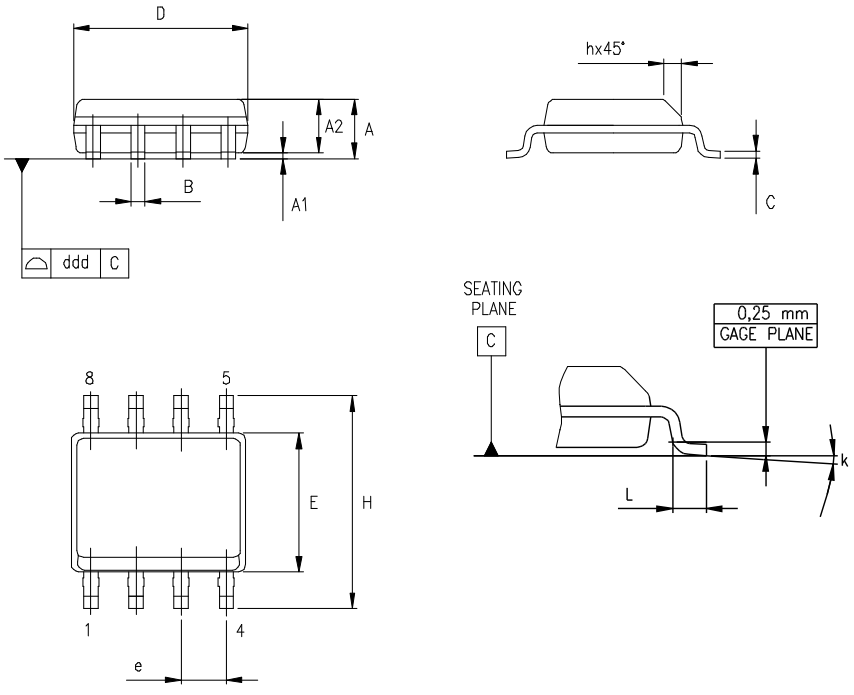
8.2 SO-8 Package

SO-8 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.04		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D	4.80		5.00	0.189		0.197
E	3.80		4.00	0.150		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	8° (max.)					
ddd			0.1			0.04



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9 Revision History

Date	Revision	Description of Changes
01 Nov 2004	1	First Release