NCP5623C

Triple Output I2C Controlled RGB LED Driver

The NCP5623C mixed analog circuit is a triple output LED driver dedicated to the RGB illumination or backlight LCD display.

The built−in DC/DC converter is based on a high efficient charge pump structure with operating mode 1x and 2x. It provides a 94% peak efficiency. The tiny package makes the device suitable for room limited portable applications.

Features

- 2.7 to 5.5 V Input Voltage Range
- RGB Function Fully Supported
- Programmable Integrated Gradual Dimming
- 90 mA Output Current Capability
- 94% Peak Efficiency
- Built−in Short Circuit Protection
- Provides Three Independent LED Drives
- Support I2C Protocol
- Embedded OVP / Open Load Protection
- This is a Pb−Free Device

Typical Applications

- Multicolor Illuminations
- Portable Back Light
- Digital Cellular Phone Camera Photo Flash
- LCD and Key Board Simultaneous Drive

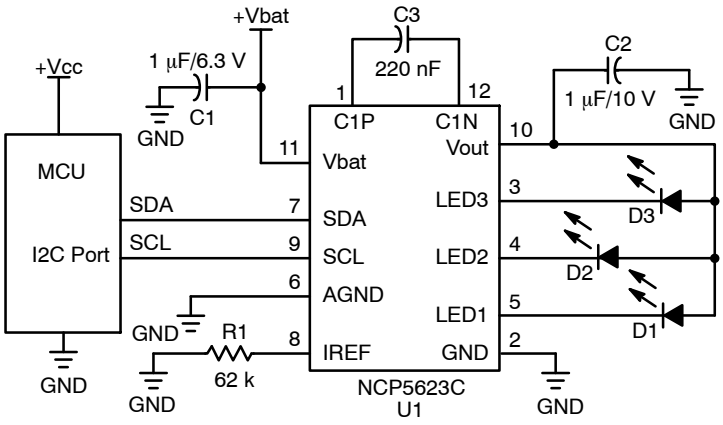
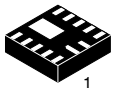


Figure 1. Typical Multiple White LED Driver

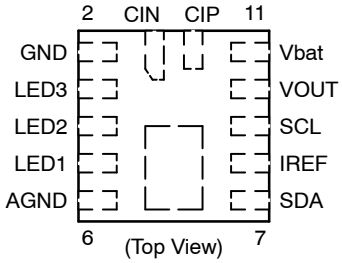
ON Semiconductor®

http://onsemi.com

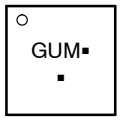
LLGA12
MU SUFFIX
CASE 513AA



PIN ASSIGNMENT



MARKING DIAGRAM



GU = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NCP5623CMUTBG	LLGA12 (Pb−Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

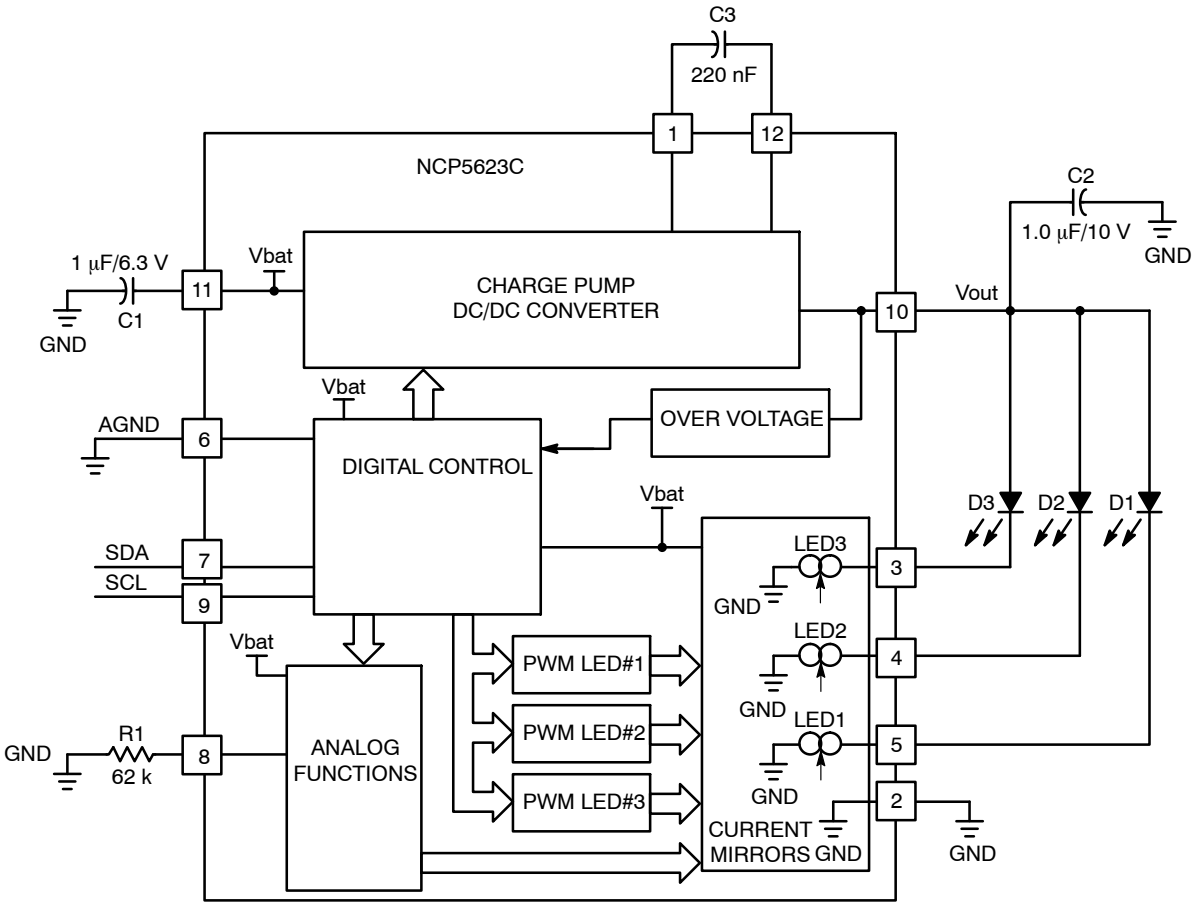


Figure 2. Simplified Block Diagram

PIN ASSIGNMENT

PIN	Name	Type	Description
1	C1P	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1N, pin 12 (Note 1).
2	GND	POWER	This pin is the GROUND signal for the analog and digital blocks and must be connected to the system ground. This pin is the GROUND reference for the DC/DC converter and the output current control. The pin must be connected to the system ground, a ground plane being strongly recommended.
3	LED3	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the LED3, intended to be used in illumination application (Note 2). The Anode of the associated LED shall be connected to the Vout pin.
4	LED2	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the LED2, intended to be used in illumination application (Note 2). The Anode of the associated LED shall be connected to the Vout pin.
5	LED1	INPUT, POWER	This pin sinks to ground and monitors the current flowing into the LED1, intended to be used in illumination application (Note 2).
6	AGND	ANALOG GROUND	This pin copies the Analog Ground and must be connected to the system ground plane.
7	SDA	INPUT, DIGITAL	This pin carries the data provided by the I2C protocol. The content of the SDA byte is used to program the mode of operation and to set up the output current (Note 1).
8	I_{REF}	INPUT, ANALOG	This pin provides the reference current, based on the internal band−gap voltage reference, to control the output current flowing in the LED. A 1% tolerance, or better, resistor shall be used to get the highest accuracy of the LED biases. An external current mirror can be used to bias this pin to dynamically set up the I−LED peak current. In no case shall the voltage at I_{REF} pin be forced either higher or lower than the 600 mV provided by the internal reference.
9	SCL	INPUT, DIGITAL	This pin carries the I2C clock to control the Charge Pump converter and to set up the output current. The SCL clock is associated with the SDA signal.
10	VOUT	OUTPUT, POWER	This pin provides the output voltage supplied by the Charge Pump converter. The Vout pin must be bypassed by 1 μF ceramic capacitor located as close as possible to the V_{OUT} pin to properly bypass the output voltage to ground. The circuit shall not operate without such bypass capacitor connected across the Vout pin and Ground (Note 1). The output voltage is internally clamped to 5.5 V maximum in the event of a no load situation. On the other hand, the output current is limited to 40 mA (typical) in the event of a short circuit to ground.
11	VBAT	INPUT, POWER	This pin is the input Battery voltage to supply the analog and digital blocks. The pin must be decoupled to ground by a 1μF or higher ceramic capacitor (Note 1).
12	C1N	POWER	One side of the external charge pump capacitor (C_{FLY}) is connected to this pin, associated with C1P, pin 1 (Note 1)

1. Using low ESR ceramic capacitor, X5R type, is mandatory to optimize the Charge Pump efficiency and to reduce the EMI.
2. The peak current is 37 mA for each LED, the total charge pump output DC current being limited to 75 mA

MAXIMUM RATINGS

Symbol	Rating	Value	Unit
V_{BAT}	Power Supply (see Figure 3)	−0.3 < Vbat < 7.0	V
Vout	Output Power Supply	7.0	V
SDA, SCL, SHDI2C	Digital Input Voltage Digital Input Current	−0.3 < V < V_{BAT} 1	V mA
ESD	Human Body Model: R = 1500 Ω, C = 100 pF (Note 3) Machine Model	2 200	kV V
 P_D $R_{\theta JC}$ $R_{\theta JA}$	LLGA12 package Power Dissipation @ T_A = +85°C (Note 4) Thermal Resistance Junction to Case Thermal Resistance Junction to Air	 200 51 200	 mW °C/W °C/W
T_A	Operating Ambient Temperature Range	−40 to +85	°C
T_J	Operating Junction Temperature Range	−40 to +125	°C
T_{Jmax}	Maximum Junction Temperature	+150	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
	Latch−up current maximum rating per JEDEC standard: JESD78.	±100	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) ±2.0 kV per JEDEC standard: JESD22−A114
   Machine Model (MM) ±200 V per JEDEC standard: JESD22−A115
4. The maximum package power dissipation limit must not be exceeded.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.

POWER SUPPLY SECTION:

(Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
11	V_{bat}	Power Supply	2.7		5.5	V
10	I_{out}	Continuous DC current in the load, PWM = 100% @ Vf = 3.4 V, Vbat = 3.0 V @ Vf = 3.4 V, 3.3 V < Vbat < 5.5 V	 55 75			mA
10	Isch	Continuous Output Short Circuit Current 2.85 V < Vbat < 4.2 V		45	90	mA
10	Vout	Output Voltage Compliance (OVP)	4.4		5.7	V
10	Tstart	DC/DC Start time (Cout = 1 μF) 3.0 V < Vbat = nominal < 5.5 V from last CNTL positive pulse delay to full load operation		150		μs
10	I_{stdb}	Stand By Current 3.0 V ≤ Vbat ≤ 4.2 V, Iout = 0 mA		0.8	1.0	μA
10	I_{op}	Operating Current, @Iout = 0 mA, 3.0 V ≤ Vbat ≤ 4.2 V		350		μA
3,4,5	I_{TOL}	RGB Output Current Tolerance @Vbat = 3.6 V, I_{LED} = 10 mA −25°C < Ta < 85°C		±3		%
3,4,5	I_{MATCH}	RGB Output Current LED Matching @Vbat = 3.6 V, I_{LED} = 5.0 mA		±0.5		%
	Fpwr	Charge Pump Operating Frequency −40°C < Ta < 85°C	0.8	1	1.2	MHz
	E_{PWR}	Efficiency @ Vbat = 3.6 V − LED1 to LED3 = 5 mA, Vf = 2.8 V (Total = 15 mA) − LED1 to LED3 = 20 mA, Vf = 3.2 V (Total = 60 mA)		 94.2 92.3		%

ANALOG SECTION:

(Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
8	I_{REF}	Reference current @Vref = 600 mV (Note 7)	3	12.5	20	μA
8	V_{REF}	Reference Voltage (Note 7)	−3%	600	+3%	mV
	I_{LEDR}	Reference Current (IREF) current ratio		2400		
8	Rbias	External Reference current Bias resistor (Note 6)	30	48	200	kΩ
3,4,5	F_{PWM}	Internal PWM Frequency (Note 8)		2.1		kHz

6. The overall output current tolerance depends upon the accuracy of the external resistor. Using 1% or better resistor is recommended.
7. The external circuit must not force the I_{REF} pin voltage either higher or lower than the 600 mV specified. The system is optimized with a 12.5 μA reference current.
8. This parameter, derived from the 1 MHz clock, is guaranteed by design, not tested in production.

DIGITAL PARAMETERS SECTION:

(Typical values are referenced to T_A = +25°C, Min & Max values are referenced −40°C to +85°C ambient temperature, unless otherwise noted), operating conditions 2.85 V < Vbat < 5.5 V, unless otherwise noted.

Pin	Symbol	Rating	Min	Typ	Max	Unit
9	F_{SCL}	Input I2C clock frequency			400	kHz
7,9	V_{IH}	Positive going Input High Voltage Threshold, SDA, SCL signals (Note 9)	1.6		V_{BAT}	V
7,9	V_{IL}	Negative going Input High Voltage Threshold, SDA, SCL signals (Note 9)	0		0.4	V

NOTE: Digital inputs undershoot ≤ 0.30 V to ground, Digital inputs overshoot < 0.30 V to V_{BAT}

9. Test guaranteed by design and fully characterized, not implemented in production.
10. The fall time − t_f − for both SCL and SDA input signals must be 120 ns maximum.

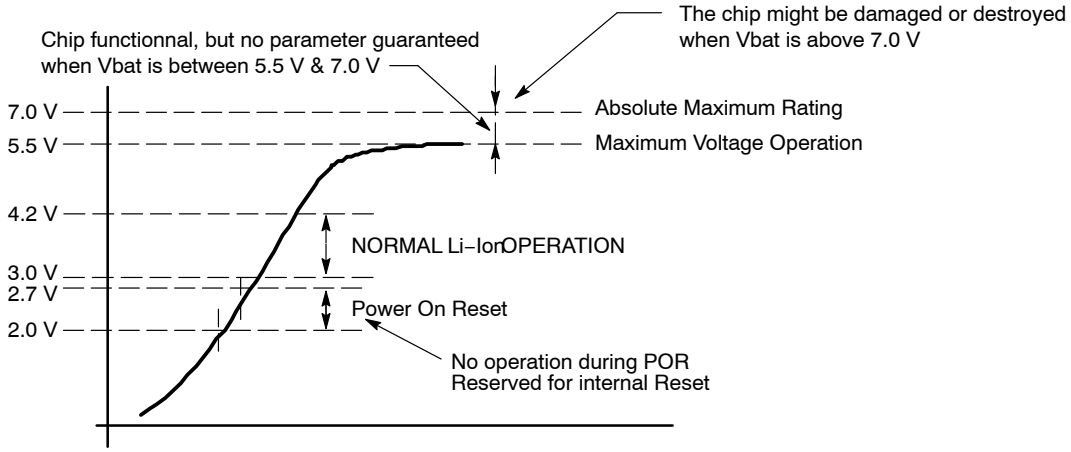


Figure 3. Understanding Integrated Circuit Voltage Limitations

DC/DC OPERATION

The converter is based on a charge pump technique to generate a DC voltage capable to supply the RGB LED load. The system regulates the current flowing into each LED, not the DC Vout value, by means of internal current mirrors associated with the diodes.

Consequently, Vout = Vbat * Mode, with Mode = 1 or Mode = 2, the extra voltage Vout – Vf being sustained by the current mirror structure.

The average forward current of each LED can be independently programmed (by means of the associated PWM) to achieve the RGB function. The maximum LED current, setup by the external bias resistor connected across IREF pin and Ground, is associated to the digital content of the I2C register (see Table 1). This peak current applies to the three LED simultaneously, but, thanks to the RGB function, the average output current of each LED is controlled by the independent PWM controllers. Consequently, the luminosity of each RGB diode can be independently adjusted to cope with a given illumination need. Since the peak current is constant, the color of the RGB diodes is the one defined by the specifications of each individual LED.

The built−in OVP circuit continuously monitors the V_{out} voltage and stops the converter when the voltage is above 5.7 V. The converter resumes to normal operation when the voltage drops below 4.4 V (no latch−up mechanism). Consequently, the chip can operate under no load conditions during any test procedures.

LOAD CURRENT CALCULATION

The load current is derived from the 600 mV reference voltage provided by the internal Band Gap associated to the external resistor connected across I_{REF} pin and Ground. Note : due to the internal structure of this pin, no voltage, either downward or upward, shall be forced at the I_{REF} pin.

The reference current is multiplied by the constant k = 2400 to yield the output load current. Since the reference voltage is based on a temperature compensated Band Gap, a tight tolerance resistor will provide a very accurate load current. The resistor is calculated from the Ohm's law (R_{bias} = Vref/I_{REF}) and a more practical equation can be arranged to define the resistor value for a given maximum output current:

R_{bias} = (Vref*k)/Iout [1]

R_{bias} = (0.6*2400)/Iout

R_{bias} = 1440/Iout [2]

Since the Iref to ILED ratio is very high, it is strongly recommended to set up the reference current at 12.5 μA to optimize the tolerance of the output current. Although it is possible to use higher or lower value, as defined in the analog section, a 48 kΩ / 1% resistor will provide the best compromise, the dimming being performed by the appropriate PWM registers.

On the other hand, care must be observed to avoid leakage current flowing into either the IREF pin of the bias resistor network.

Finally, for any desired ILED current, the curve provided Figure 4 can be recalculated according to the equation:

$$ILED = \frac{IREF \cdot k}{31 - n} \quad \text{(eq. 1)}$$

$$ILED = \frac{\frac{Vref}{R} \cdot 2400}{31 - n} \quad \text{(eq. 2)}$$

with: n = step value @ $1 \le n \le 31$
R = reference resistance
k = internal multiplier constant = 2400
Note: n = 0 forces ILED to zero
n = 30 and n = 31 yields the same LED current

LOAD CONNECTION

The primary function of the NCP5623C is to control three LED arranged in the RGB color structure (reference OSRAM LATB G66x). The brightness of each LED is independently controlled by a set of dedicated PWM structure embedded into the silicon chip. The peak current, identical for each LED, is programmable by means of the I2C data byte. With 32 steps per PWM, the chip provides 32768 colors hue in a standard display.

Moreover, a built−in gradual dimming provides a smooth brightness transition for any current level, in both Upward and Downward direction. The dimming function is controlled by the I2C interface: see Table 2.

The NCP5623C chip is capable to drive the three LED simultaneously, as depicted in Figure 1, but the load can be arranged to accommodate several LED if necessary in the application. Finally, the three current mirrors can be connected in parallel to drive a single power full LED, thus yielding 90 mA current capability in a single LED.

I2C PROTOCOL

The NCP5623C is programmed by means of the standard I2C protocol controlled by an external MCU. The communication takes place with two serial bytes sharing the same I2C frame:

– Byte#1 → physical I2C address

– Byte#2 → Selected internal registers & function

B7	B6	B5	B4	B3	B2	B1	B0
Byte#1 : I2C Physical Address, based 7 bits : % 011 1001 → $39 *							
0	1	1	1	0	0	1	R/W
Byte#2 : DATA register							
RLED2	RLED1	RLED0	BLED4	BLED3	BLED2	BLED1	BLED0

*Note: according to the I2C specifications, the physical address is based on 7 bits out of the SDA byte, the 8th bit representing the R/W command. Since the NCP5623C is a receiver only, the R/W command is 0 and the hexadecimal byte send by the MCU is %0111 0010 = $72

B[7:5] : Internal Register Selection:

B7	B6	B5	Function
0	0	0	Chip Shut Down → all LED current = zero
0	0	1	Set up the maximum Output LED Current
0	1	0	PWM1 : LED1 control
0	1	1	PWM2 : LED2 control
1	0	0	PWM3 : LED3 control
1	0	1	Set the Upward Iend target
1	1	0	Set the Downward Iend target
1	1	1	Set the number of steps and activate the Gradual Dimming

The contain of bits B[4:0] depends upon the type of function selected by bits B[7:5] as depicted in Table 1

Table 1. Internal Register Bits Assigment

B7	B6	B5	B4	B3	B2	B1	B0	Comments
0	0	0	X	X	X	X	X	Shut down
0	0	1	16	8	4	2	1	Output LED Step, see Figure 4 (Note 11)
0	1	0	BPWM16	BPWM8	BPWM4	BPWM2	BPWM1	PWM1
0	1	1	BPWM16	BPWM8	BPWM4	BPWM2	BPWM1	PWM2
1	0	0	BPWM16	BPWM8	BPWM4	BPWM2	BPWM1	PWM3
1	0	1	GDIM5 16	GDIM4 8	GDIM3 4	GDIM2 2	GDIM1 1	Set Gradual Dimming Upward Iend Target (Note 12)
1	1	0	GDIM5 16	GDIM4 8	GDIM3 4	GDIM2 2	GDIM1 1	Set Gradual Dimming Downward Iend Target (Note 12)
1	1	1	GDIM5 128 ms	GDIM4 64 ms	GDIM3 32 ms	GDIM2 16 ms	GDIM1 8 ms	Gradual Dimming Step Number & run

11. The programmed current applies to the three LED simultaneously, the gradual dimming is not engaged
12. The bit values represent the steps count, not the ILED current: see equations 1 & 2, page 7, to derive the ILED value.

GRADUAL DIMMING

The purpose of that function is to gradually Increase or Decrease the brightness of the backlight LED upon command from the external MCU. The function is activated and controlled by means of the I2C protocol.

In order to avoid arithmetic division functions at silicon level, the period (either upward or downward) is equal to the time defined for each step, multiplied by the number of steps.

To operate such a function, the MCU will provide three information:

1 – The target current level (either upward or downward)

2 – The time per step

3 – The Upward or Downward mode of operation

When a new gradual dimming sequence is requested, the output current increases, according to an exponential curve, from the existing start value to the end value. The end current value is defined by the contain of the Upward or Downward registers, the width of each step is defined by the third register, the number of step being in the 1 to 30 range. In the event of software error, the system checks that neither the maximum output current (30 mA), nor the zero level are forced out of their respective bounds. Similarly, software errors shall not force the NCP5623C into an uncontrolled mode of operation.

The dimming is built with 30 steps and the time delay encoded into the second byte of the I2C transaction: see Table 1.

When the gradual dimming is deactivated (B7 = B6 = 0, B5 = 1), the output current is straightforwardly set up to the level defined by the contain of the related register upon acknowledge of the output current byte.

The gradual dimming sequence must be set up before a new output current data byte is send to the NCP5623C . At this point, the brightness sequence takes place when the new data byte is acknowledged by the internal I2C decoder. Since the six registers are loaded on independent byte flow associated to the I2C address, any parameter of the NCP5623C chip can be updated ahead of the next function as depicted in Table 2.

Table 2. Basic Programming Sequences

I2C Address	COMMAND Bits[7:0]	Operation	Note
$72	000X XXXX	System Shut Down	Bits[4:0] are irrelevant
$72	0010 0000 0011 1111	Set Up the ILED current	ILED register Bits[4:0] contain the IMAX value as defined by the Iref value
$72	0100 0000 0101 1111	Set Up the PWM1	PWM1 Bits[4:0] contain the PWM value
$72	0110 0000 0111 1111	Set Up the PWM2	PWM2 Bits[4:0] contain the PWM value
$72	1000 0000 1001 1111	Set Up the PWM3	PWM3 Bits[4:0] contain the PWM value
$72	1010 0000 1011 1111	Set Up the IEND Upward	UPWARD Bits[4:0] contain the IEND value
$72	1100 0000 1101 1111	Set Up the IEND Downward	DWNWRD Bits[4:0] contain the IEND value
$72	1110 0000 1111 1111	Set Up the Gradual Dimming time and run the sequence	GRAD Bits[4:0] contain the TIME value

The number of step for a given sequence, depends upon the start and end output current range: since the IPEAK value is encoded in the Bits[4:0] binary scale, a maximum of 31 steps is achievable during a gradual dimming operation.

The number of steps will be automatically recalculated by the chip according to the equation:

Nstep = | existing step position − new step position |

As an example, assuming the previously programmed step was 5 and the new one is 15, then we will have 10 steps to run between the actual location to the end value. If the timing was set at 16 ms, the total gradual dimming sequence will be 160 ms.

To select the direction of the gradual dimming (either Upward or Downward), one shall send the appropriate register before to activate the sequence as depicted below:

1010 1111 → 1110 0011 → select an UPWARD sequence with 24 ms/step, the end IPEAK current being (IREF * 2400) / (31 − 16) mA.

1100 0001 → 1110 0100 → select the DOWNWARD sequence with 32 ms/step, the end IPEAK current being (IREF * 2400) / (31 − 1) mA.

Table 3. Output Current Programmed Value (ILED = F(Step))

Step	ILED (mA)	Step	ILED (mA)	Step	ILED (mA)	Step	ILED (mA)
0 / $00	0	9 / $09	1.25	18 / $12	2.12	27 $1B	6.90
1 / $01	0.92	10 / $0A	1.31	19 / $13	2.30	28 / $1C	9.20
2 / $02	0.95	11 / $0B	1.38	20 / $14	2.50	29 / $1D	13.80
3 / $03	0.98	12 / $0C	1.45	21 / $15	2.76	30 / $1E	27.60
4 / $04	1.02	13 / $0D	1.53	22 / $16	3.06	31 / $1F	27.60
5 / $05	1.06	14 / $0E	1.62	23 / $17	3.45		
6 / $06	1.10	15 / $0F	1.72	24 / $18	3.94		
7 / $07	1.15	16 / $10	1.84	25 / $19	4.60		
8 / $08	1.20	17 / $11	1.97	26 / $1A	5.52		

NOTE: The table assumes I_{REF} = 11.5 μA

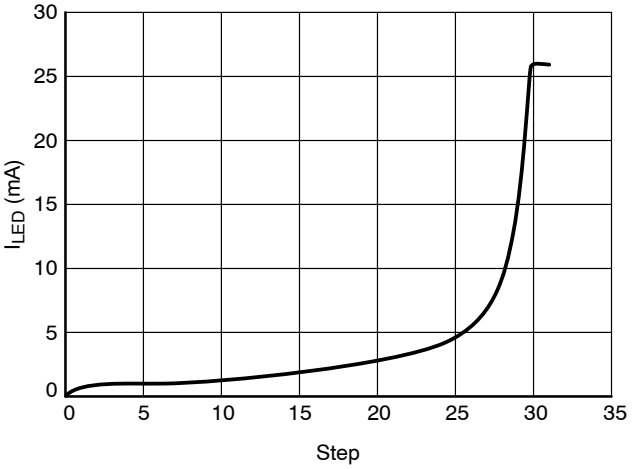


Figure 4. Output Current Programmed Value (ILED = F(Step))

PWM OPERATION

The built−in PWM are fully independent and can be programmed to any value during the normal operation of the NCP5623C chip. The PWM operate with five bits, yielding a 32 steps range to cover the full modulation (0 to 100%) of the associated LED:

- PWM = $00 → the associated LED is fully OFF, whatever be the programmed ILED value
- PWM > $00 but < $1F → the brightness of the associated LED is set depending upon the PWM modulation value
- PWM = $1F → the associated LED is fully ON, the current being the one defined by the ILED value.

Each PWM is programmable, via the I2C port as depicted, at any time under any sequence arrangement as requested by the end system's designer. The PWM does not change the ILED value, but merely modulate the ON/OFF ratio of the associated LED. Each step of the PWM represent 100/32 = 3.125% of the full range, the clock being 2.1 kHz (typical).

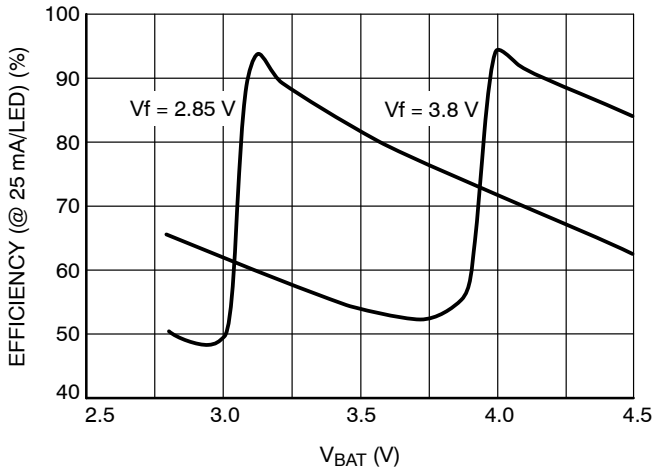


Figure 5. NCP5623C Typical Efficiency as a Function of the Vf

NOTE: Efficiency is measured with the three PWM equal to 100%

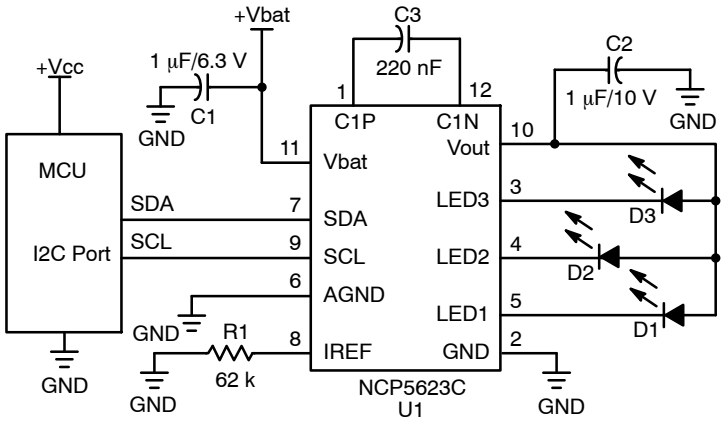
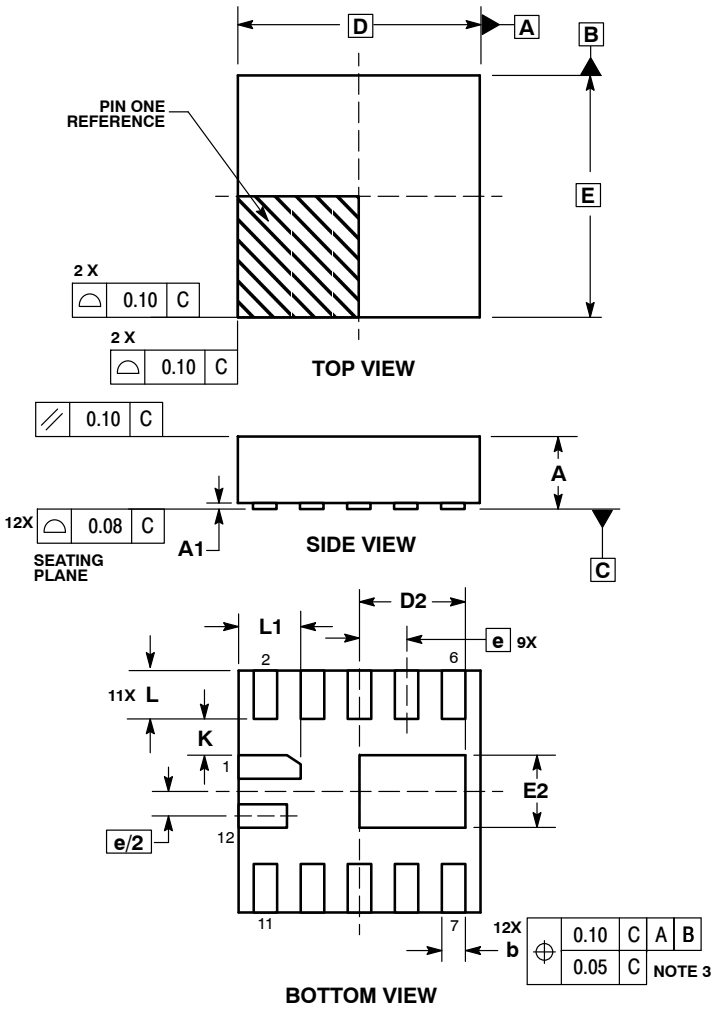


Figure 6. Basic RGB Application

PACKAGE DIMENSIONS

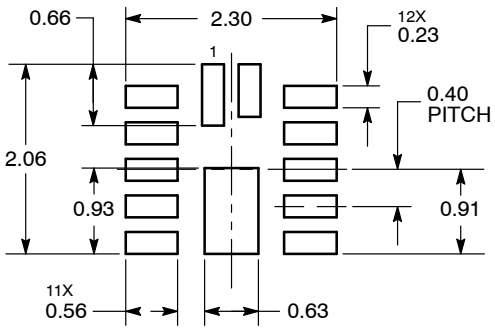
LLGA12
CASE 513AA−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.50	0.60
A1	0.00	0.05
b	0.15	0.25
D	2.00 BSC	
D2	0.80	1.00
E	2.00 BSC	
E2	0.55	0.65
e	0.40 BSC	
K	0.25	−−−
L	0.30	0.50
L1	0.40	0.60

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

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