6-Channel LED Driver

ISL97672

The ISL97672 is an integrated power LED driver that controls 6 channels of LED current for LCD backlight applications. The ISL97672 is capable of driving up to 78 LEDs from 4.5V to 26V or 48 LEDs from a boost supply of 2.7V to 26V and a separate 5V bias supply on the VIN pin.

The ISL97672 compensates for non-uniformity of the forward voltage drops in the LED strings with its 6 voltage controlled-current source channels. Its headroom control monitors the highest LED forward voltage string for output regulation, to minimize the voltage headroom and power loss in a typical multi-string operation.

The ISL97672 allows direct PWM mode by following the external signal from 0Hz to 30KHz at 0.4% to 100% duty cycle and maintaining a typical ±0.7% current matching between channels.

The ISL97672 features a separate EN pin and extensive protection functions that flag whenever a fault occurs. The protections include string open and short circuit detections, OVP, OTP, thermal shutdown and an optional input overcurrent protection with fault disconnect switch.

Related Literature* (see page 16)

- See AN1581, "ISL97671/2/3/4IRZ-EVAL Quick Start Guide"

Features

- 6 Channels
- 4.5V to 26.5V Input
- 45V Output Max
- Up to 40mA LED Current per channel
- Direct PWM Dimming without Phase Shift
- PWM Dimming Linearity 0.4%~100% <30kHz
- Adjustable 200kHz to 1.4MHz Switching Frequency
- Dynamic Headroom Control
- Protections with Flag Indication
  - String Open/Short Circuit, V_{OUT} Short Circuit, Overvoltage and Over-Temperature Protections
  - Optional Master Fault Protection
- Current Matching ±0.7%
- 20 Ld 4mmx3mm QFN Package

Applications* (see page 16)

- Notebook Displays LED Backlighting
- LCD Monitor LED Backlighting
- Automotive Displays LED Backlighting
- Automotive or Traffic Lighting

Typical Application Circuit

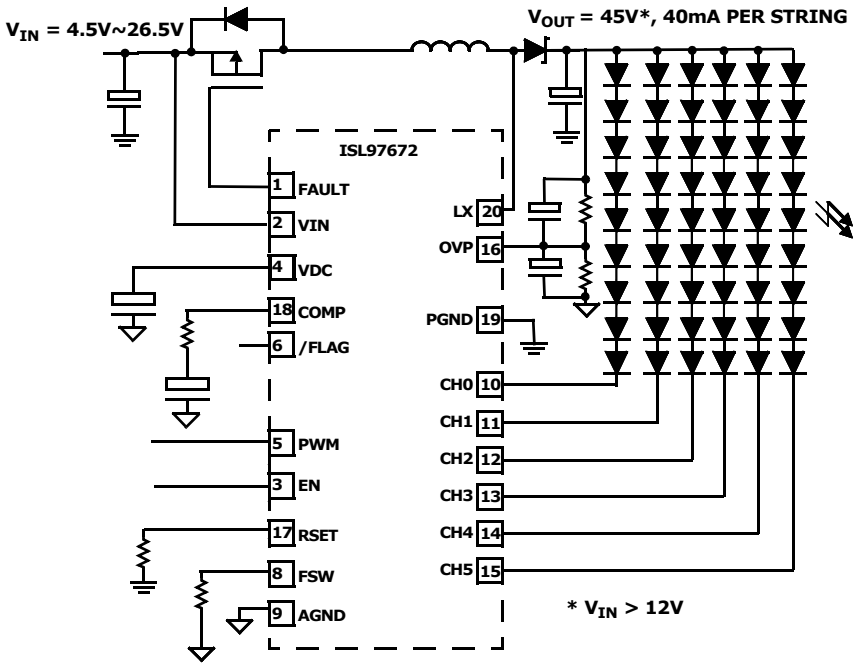


FIGURE 1. ISL97672 TYPICAL APPLICATION DIAGRAM

Block Diagram

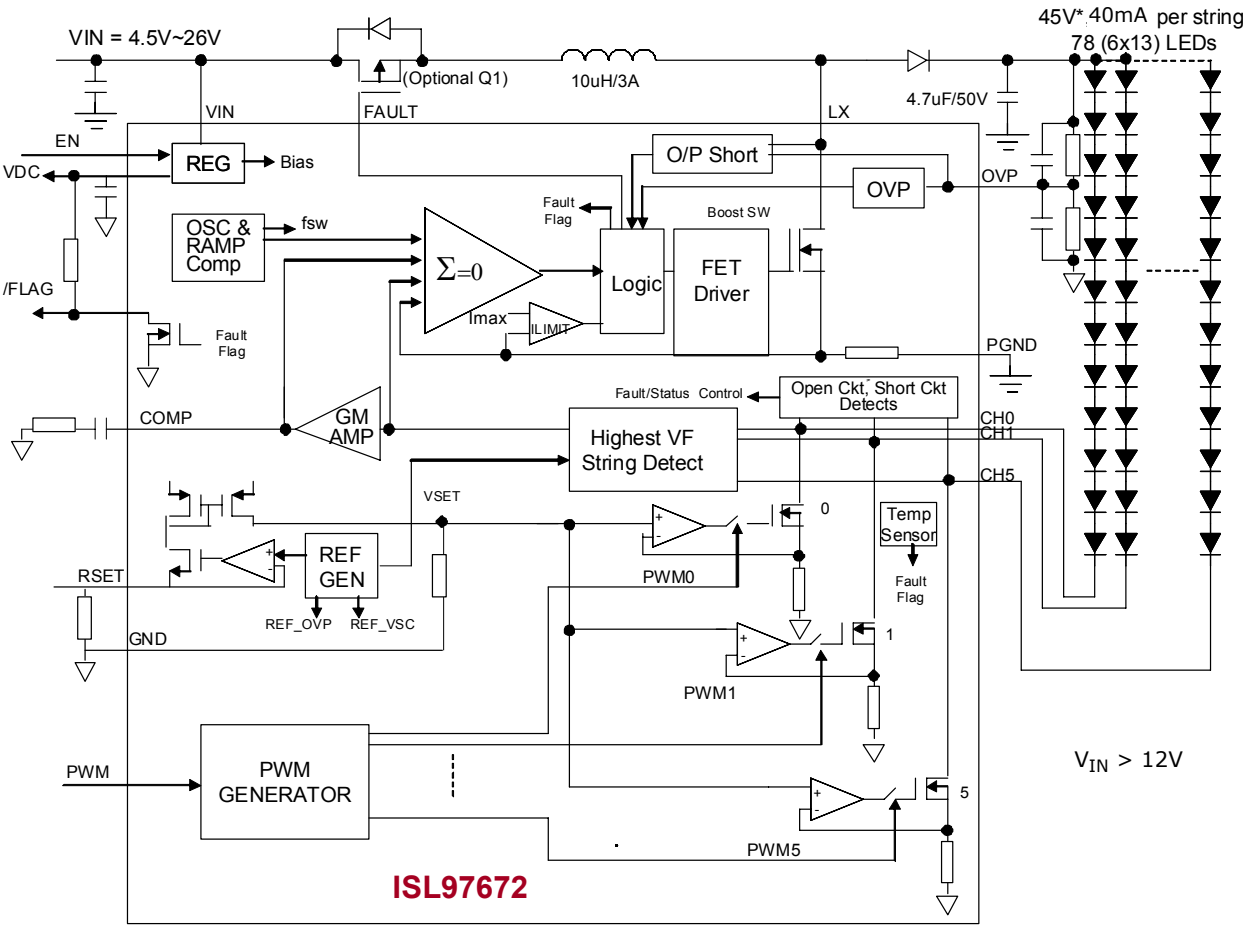


FIGURE 2. ISL97672 BLOCK DIAGRAM

Ordering Information

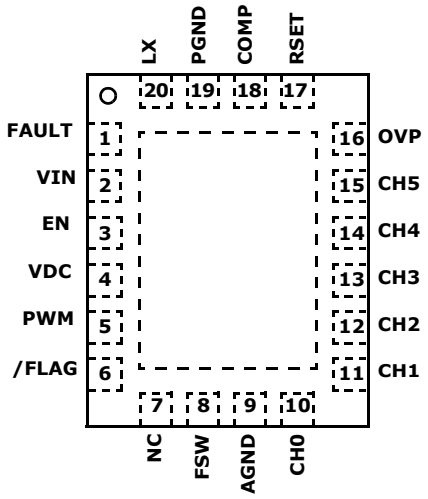
PART NUMBER (Notes 1, 2, 3)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97672IRZ	7672	20 Ld 4x3 QFN	L20.3x4
ISL97672IRZ-EVAL	Evaluation Board		

NOTES:

1. Add "-T" or "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97672. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL97672
(20 LD 4X3 QFN)
TOP VIEW



Pin Descriptions (I = Input, O = Output, S = Supply)

PIN NAME	PIN #	TYPE	DESCRIPTION
FAULT	1	O	Fault disconnect switch
VIN	2	S	Input voltage for the device and LED power
EN	3	I	The device needs 4ms for initial power-up Enable. It will be disabled if it is not biased for longer than 28ms.
VDC	4	S	De-couple capacitor for internally generated supply rail.
PWM	5	I	PWM brightness control pin.
/FLAG	6	O	/Flag = 0 for any fault conditions. /Flag =1 for normal condition. Open drain that needs pull up.
NC	7	I	No Connect
FSW	8	I	Boost switching frequency set pin by connecting a resistor. See "Switching Frequency" on page 10 for resistor calculation
AGND	9	S	Analog Ground for precision circuits
CH0	10	I	Input 0 to current source, FB, and monitoring
CH1	11	I	Input 1 to current source, FB, and monitoring
CH2	12	I	Input 2 to current source, FB, and monitoring
CH3	13	I	Input 3 to current source, FB, and monitoring
CH4	14	I	Input 4 to current source, FB, and monitoring
CH5	15	I	Input 5 to current source, FB, and monitoring
OVP	16	I	Overvoltage protection input
RSET	17	I	Resistor connection for setting LED current, (see Equation 1 for calculating the ILEDpeak)
COMP	18	O	Boost compensation pin
PGND	19	S	Power ground (LX Power return)
LX	20	O	Input to boost switch

Absolute Maximum Ratings (T_A = +25°C)

VIN, EN. . . . . -0.3V to 28V
FAULT . . . . . VIN - 8.5V to VIN + 0.3V
VDC, COMP, RSET, PWM, OVP, /FLAG, FSW . . . -0.3V to 5.5V
CH0 - CH5, LX . . . . . -0.3V to 45V
PGND, AGND . . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to AGND pin
ESD Rating
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A). 300V
Charged Device Model 1kV
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
20 Ld QFN Package (Notes 4, 5, 7)	40	2.5

Thermal Characterization (Typical)	PSI_{JT} (°C/W)
20 Ld QFN Package (Note 6)	1

Absolute Maximum Junction Temperature . . . . . +150°C
Recommended Max Operating Junction Temperature . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . .-40°C to +85°C

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside assumed under ideal case temperature.
6. PSI_{JT} is the junction-to-top thermal resistance. If the package top temperature can be measured, with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.
7. Refer to JESD51-7 high effective thermal conductivity board layout for proper via and plane designs.

Electrical Specifications

All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
GENERAL						
VIN (Note 9)	Backlight Supply Voltage	T_C = <+60°C T_A = +25°C	4.5		26.5	V
IVIN_STBY	VIN Shutdown Current				10	µA
V_{OUT}	Output Voltage	4.5V < V_{IN} ≤ 26V, F_{SW} = 600kHz			**45**	V
		8.55V < V_{IN} ≤ 26V, F_{SW} = 1.2MHz			**45**	V
		4.5V < V_{IN} ≤ 8.55V, F_{SW} = 1.2MHz			**V_{IN}/0.19**	V
Vuvlo	Undervoltage Lock-out Threshold		2.6		**3.3**	V
Vuvlo_hys	Undervoltage Lock-out Hysteresis			275		mV
ENABLE AND PWM GENERATOR						
VIL	Guaranteed Range for PWM Input Low Voltage				**0.8**	V
VIH	Guaranteed Range for PWM Input High Voltage		**1.5**		**VDD**	V
FPWM	PWM Input Frequency Range		**200**		**30,000**	Hz
t_{ON}	Minimum On Time		**250**		**350**	ns

Electrical Specifications All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
REGULATOR						
VDC	LDO Output Voltage	V_{IN} > 6V	**4.55**	4.8	**5**	V
IVDC_STBY	Standby Current	EN = 0V			**5**	µA
IVDC	Active Current	EN = 5V		5		mA
VLDO	VDC LDO Droop Voltage	V_{IN} > 5.5V, 20mA		20	**200**	mV
ENLow	Guaranteed Range for EN Input Low Voltage				**0.5**	V
ENHi	Guaranteed Range for EN Input High Voltage		**1.8**			V
t_{ENLow}	EN low time before shut-down			30.5		ms
BOOST						
SWILimit	Boost FET Current Limit		**1.5**	2.0	2.7	A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance	T_A = +25°C		235	300	mΩ
SS	Soft-start	100% LED Duty Cycle		7		ms
Eff_peak	Peak Efficiency	V_{IN} = 12V, 72 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		92.9		%
		V_{IN} = 12V, 60 LEDs, 20mA each, L = 10µH with DCR 101mΩ, T_A = +25°C		90.8		%
$\Delta I_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		%
Dmax	Boost Maximum Duty Cycle	FSW = 600kHz	**90**			%
		FSW = 1.2MHz	**81**			%
Dmin	Boost Minimum Duty Cycle	FSW = 600kHz			**9.5**	%
		FSW = 1.2MHz			**17**	%
f_S	Minimum Switching Frequency	RFSW = 200kΩ	**175**	200	**235**	kHz
f_S	Maximum Switching Frequency	RFSW = 33kΩ	**1.312**	1.50	**1.69**	MHz
$I_{LX\_leakage}$	LX Leakage Current	LX = 45V, EN = 0			10	µA
CURRENT SOURCES						
I_{MATCH}	Channel-to-Channel Current Matching	R_{SET} =20.1kΩ (I_{OUT} = 20mA)		**±**0.7	**±1.0**	%
I_{ACC}	Current Accuracy		**-1.5**		**+1.5**	%
$V_{headroom}$	Dominant Channel Current Source Headroom at IIN Pin	I_{LED} = 20mA T_A = +25°C		500		mV
V_{RSET}	Voltage at RSET Pin	R_{SET} = 20.1kΩ	**1.2**	1.22	**1.24**	mV
I_{LEDmax}	Maximum LED Current per Channel	V_{IN} = 12V, V_{OUT} = 45V, Fsw = 1.2MHz, T_A = +25°C		40		mA
FAULT DETECTION						
VSC	Short Circuit Threshold	PWM Dimming = 100%	5.2	5.85	6.6	V
Temp_shtdwn	Temperature Shutdown Threshold			150		°C
Temp_Hyst	Temperature Shutdown Hysteresis			23		°C

Electrical Specifications All specifications below are tested at T_A = +25°C; V_{IN} = 12V, EN = 5V, R_{SET} = 20.1kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 8)	TYP	MAX (Note 8)	UNIT
VOVPlo	Overvoltage Limit on OVP Pin		**1.19**		**1.25**	V
OVPfault	OVP Short Detection Fault Level			400		mV
FLAG_ON	Fault Flag	When Fault Occurs		0.4		V
FAULT PIN						
I_{FAULT}	Fault Pull-down Current	V_{IN} = 12V	**12**	21	**30**	µA
V_{FAULT}	Fault Clamp Voltage with Respect to V_{IN}	V_{IN} = 12, V_{IN}-V_{FAULT}	**6**	7	**8.3**	V
LXstart_thres	LX Start-up Threshold		**1.3**	1.4	**1.5**	V
ILXStartup	LX Start-up Current	VDC = 5.0V	**1**	3.5	**5**	mA

NOTES:

8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
9. At maximum V_{IN} of 26.5VV, minimum V_{OUT} is 28V. Minimum V_{OUT} can be lower at lower V_{IN}.
10. Limits established by characterization and are not production tested.

Typical Performance Curves

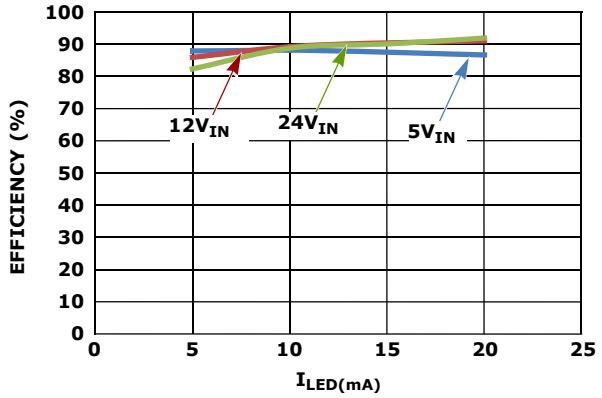


FIGURE 3. EFFICIENCY vs up to 20mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

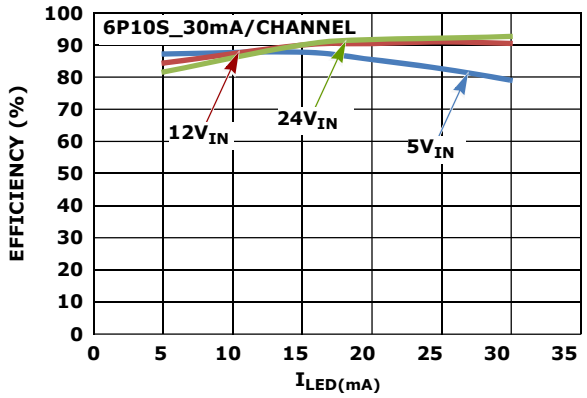


FIGURE 4. EFFICIENCY vs up to 30mA LED CURRENT (100% LED DUTY CYCLE) vs V_{IN}

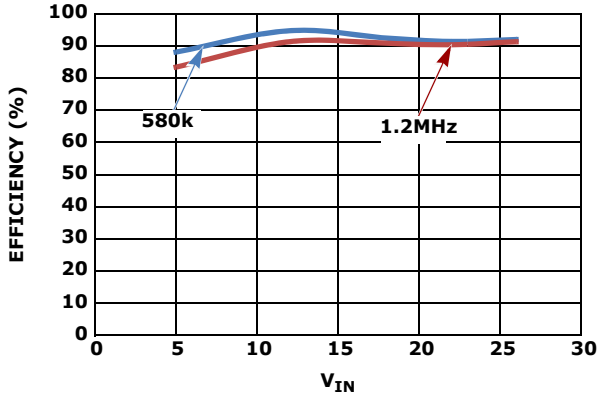


FIGURE 5. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 20mA (100% LED DUTY CYCLE)

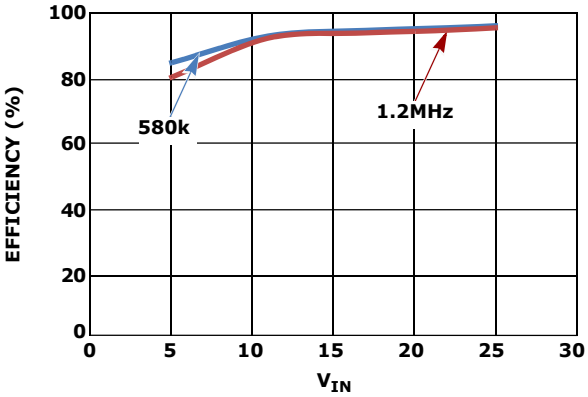


FIGURE 6. EFFICIENCY vs V_{IN} vs SWITCHING FREQUENCY AT 30mA (100% LED DUTY CYCLE)

Typical Performance Curves (Continued)

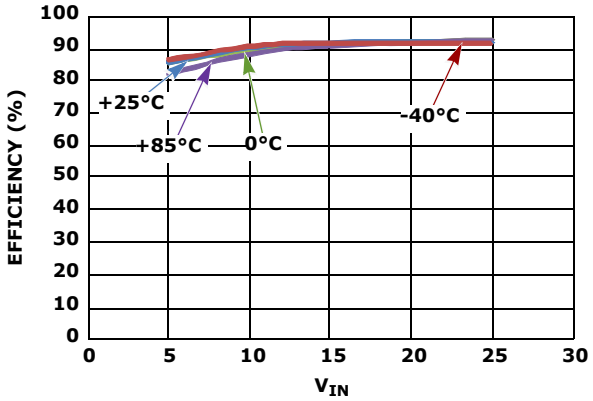


FIGURE 7. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA (100% LED DUTY CYCLE)

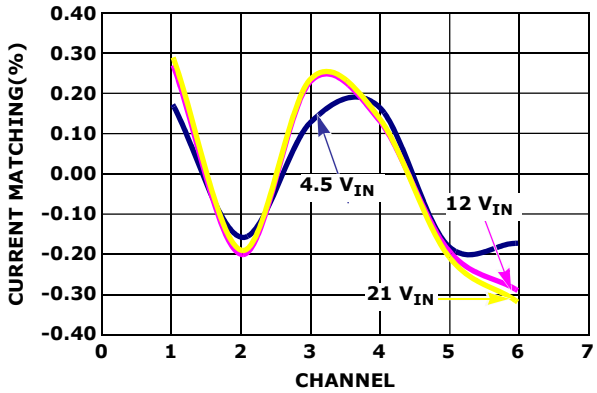


FIGURE 8. CHANNEL-TO-CHANNEL CURRENT MATCHING

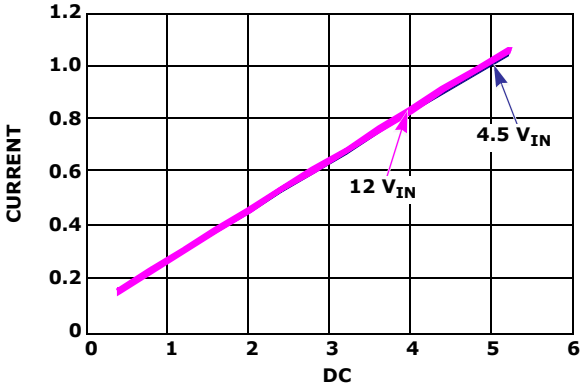


FIGURE 9. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE vs V_{IN}

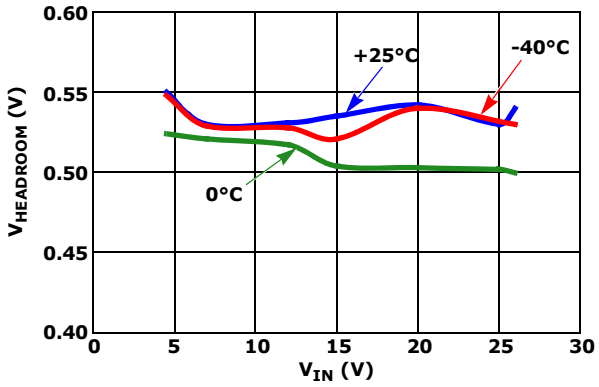


FIGURE 10. $V_{HEADROOM}$ vs V_{IN} AT 20mA

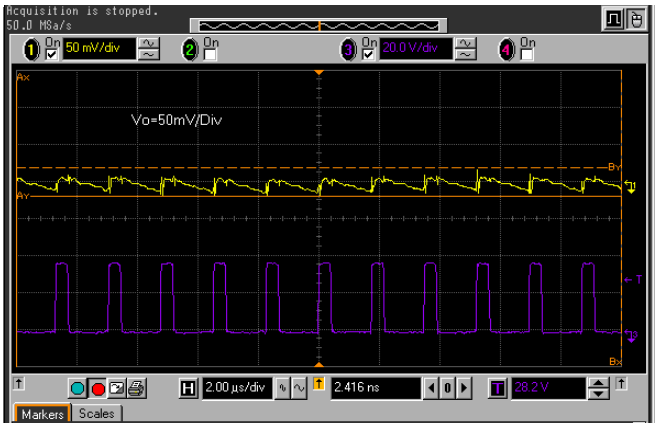


FIGURE 11. V_{OUT} RIPPLE VOLTAGE, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

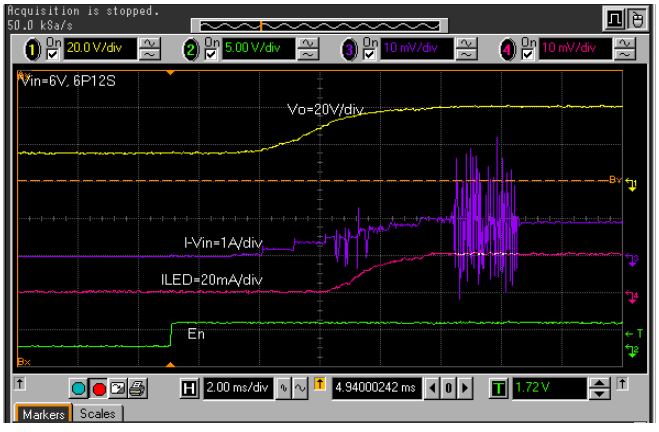


FIGURE 12. IN-RUSH and LED CURRENT AT V_{IN} = 6V FOR 6P12S AT 20mA/CHANNEL

Typical Performance Curves (Continued)

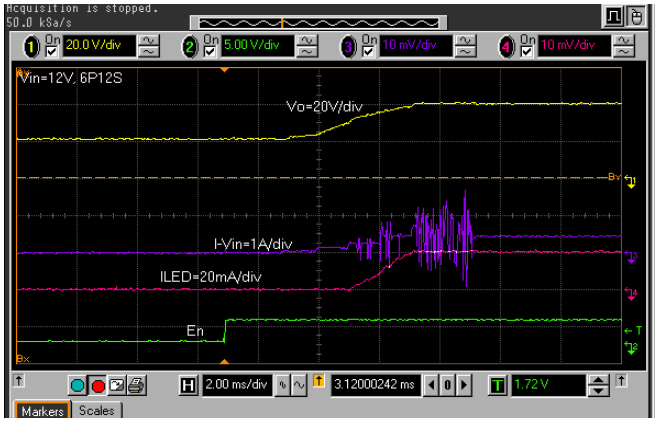


FIGURE 13. IN-RUSH AND LED CURRENT AT V_{IN} = 12V FOR 6P12S AT 20mA/CHANNEL

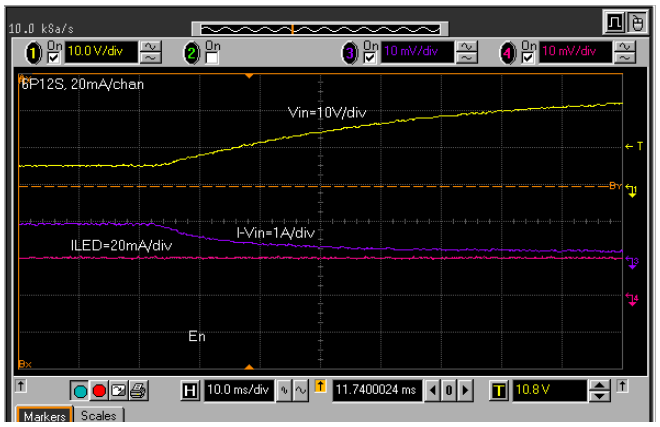


FIGURE 14. LINE REGULATION WITH V_{IN} CHANGE FROM 6V TO 26V, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

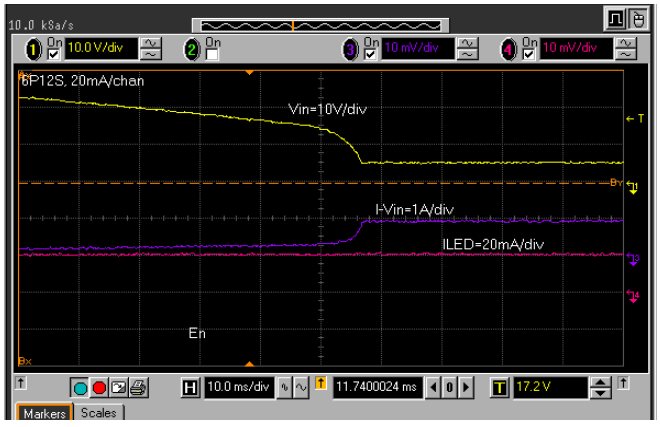


FIGURE 15. LINE REGULATION WITH V_{IN} CHANGE FROM 26V TO 6V FOR 6P12S AT 20mA/CHANNEL

FIGURE 16. LOAD REGULATION WITH I_{LED} CHANGE FROM 0% TO 100% PWM DIMMING, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

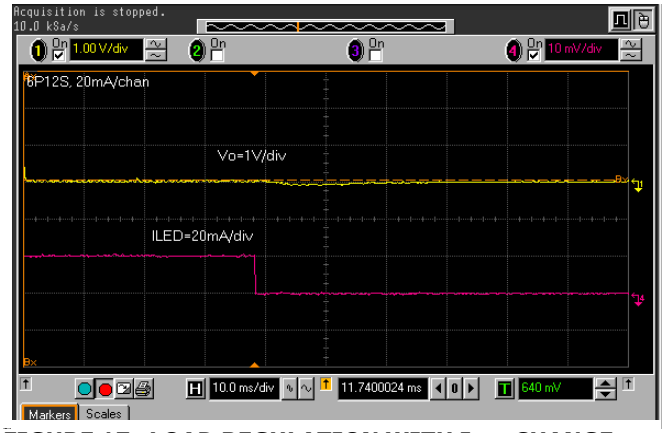


FIGURE 17. LOAD REGULATION WITH I_{LED} CHANGE FROM 100% TO 0% PWM DIMMING, V_{IN} = 12V, 6P12S AT 20mA/CHANNEL

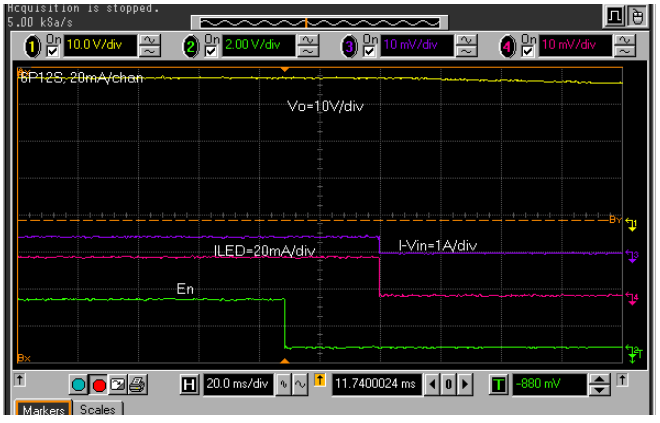


FIGURE 18. ISL97671 SHUTS DOWN AND STOPS SWITCHING ~ 30ms AFTER EN GOES LOW

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97672 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the notebook backlight application where the power can be a series of drained batteries or instantly changed to an AC/DC adapter without rendering a noticeable visual nuisance. The number of LEDs that can be driven by ISL97672 depends on the type of LED chosen in the application. The ISL97672 is capable of boosting up to 45V and typically driving 13 LEDs in series for each of the 8 channels, enabling a total of 104 pieces of the 3.2V/20mA type of LEDs.

Enable

The Enable pin is used to enable the device. If there is no signal for longer than 28ms, the device will enter shutdown. Do not let Enable pin floating thus a 10k or higher pull-down resistor should be added.

OVP and V_{OUT}

The Over Voltage Protection (OVP) pin has a function of setting the overvoltage trip level as well as limiting the V_{OUT} regulation range.

The ISL97672 OVP threshold is set by R_{UPPER} and R_{LOWER} such that:

$V_{OUT\_}ovp = 1.21V*(R_{UPPER}+R_{LOWER})/R_{LOWER}$

and V_{OUT} can only regulate between 61% and 100% of the $V_{OUT\_}ovp$ such that:

Allowable V_{OUT} = 61% to 100% of $V_{OUT\_}ovp$

For example, if 10 LEDs are used with the worst case V_{OUT} of 35V. If R1 and R2 are chosen such that the OVP level is set at 40V, then the V_{OUT} is allowed to operate between 24.4V and 40V. If the requirement is changed to a 6 LEDs of 21V V_{OUT} application, then the OVP level must be reduced and users should follow V_{OUT} = (61% ~100%) OVP level requirement. Otherwise, the headroom control will be disturbed such that the channel voltage can be much higher than expected and sometimes it can prevent the driver from operating properly.

The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if R_{UPPER}/R_{LOWER} = 33/1, then C_{UPPER}/C_{LOWER} = 1/33 with C_{UPPER} = 100pF and C_{LOWER} = 3.3nF.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 19.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $401.8/R_{SET}$.

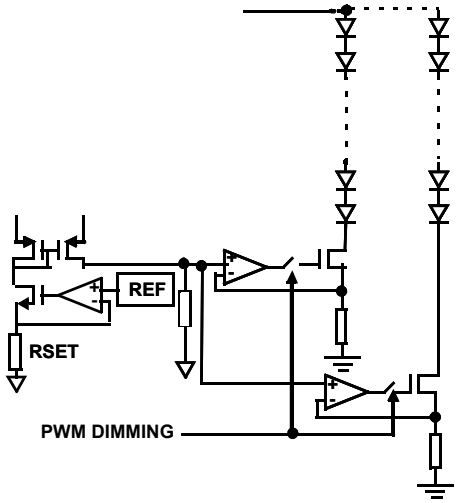


FIGURE 19. SIMPLIFIED CURRENT SOURCE CIRCUIT

The source terminals of the current source MOSFETs are designed to run at 500mV to optimize power loss versus accuracy requirements. The sources of errors of the channel-to-channel current matching come from the op amp's offset, internal layout and reference and these parameters are optimized for current matching and absolute current accuracy. The absolute accuracy is also determined by the external R_{SET}. A 1% tolerance resistor should be used.

Dynamic Headroom Control

The ISL97672 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the CH0-CH5 pins. When this lowest channel voltage is lower than the short circuit threshold, V_{SC}, such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest channel pin is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other channel pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same current. The output voltage will regulate cycle by cycle and it is always referenced to the highest forward voltage string in the architecture.

Dimming Controls

The ISL97672 allows two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

MAXIMUM DC CURRENT SETTING

The initial brightness should be set by choosing an appropriate value for R_{SET}. This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{401.8}{R_{SET}} \quad \text{(EQ. 1)}$$

For example, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 1 yields Equation 2:

$$R_{SET} = 401.8/0.02 = 20.1k\Omega \quad \text{(EQ. 2)}$$

PWM CURRENT CONTROL

The ISL97672 employs direct PWM dimming such that the output PWM dimming follows directly with the input PWM signal without modifying the input frequency. The average LED current of each channel can be calculated as Equation 3:

$$I_{LED(ave)} = I_{LED} \times PWM \quad \text{(EQ. 3)}$$

Switching Frequency

The boost switching frequency can be adjusted by a resistor as Equation 4:

$$f_{SW} = \frac{(5\times10^{10})}{R_{FSW}} \quad \text{(EQ. 4)}$$

where f_{SW} is the desirable boost switching frequency and R_{FSW} is the setting resistor.

5V Low Dropout Regulator

A 5V LDO regulator is present at the VDC pin to develop the necessary low voltage supply which is used by the chips internal control circuitry. Because VDC is an LDO pin, it requires a bypass capacitor of 1µF or more for the regulation. The VDC pin can be used as a coarse reference with few mA sourcing capability.

Inrush Control and Soft-Start

The ISL97672 has separately built-in independent inrush control and soft-start functions. The inrush control function is built around the short circuit protection FET, and is only available in applications which include this device. At start-up, the fault protection FET is turned on slowly due to a 30µA pull-down current output from the FAULT pin. This discharges the fault FET's gate-source capacitance, turning on the FET in a controlled fashion. As this happens, the output capacitor is charged slowly through the weakly turned on FET before it becomes fully enhanced. This results in a low inrush current. This current can be further reduced by adding a capacitor (in the 1nF to 5nF range) across the gate source terminals of the FET.

Once the chip detects that the fault protection FET is turned on hard, it is assumed that inrush is complete. At this point, the boost regulator will begin to switch and the current in the inductor will ramp-up. The current in the boost power switch is monitored and the switching terminated in any cycle where the current exceeds the current limit. The ISL97672 includes a soft-start feature where this current limit starts at a low value (275mA). This is stepped up to the final 2.2A current limit in seven further steps of 275mA. This is stepped up to the final 2.2A current limit in 7 further steps of 275mA. These steps will happen over at least 8ms, and will be extended at low LED PWM frequencies if the LED duty cycle is low. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

For systems with no master fault protection FET, the inrush current will flow towards C_{OUT} when VIN is applied and it is determined by the ramp rate of VIN and the values of C_{OUT} and L.

Fault Protection and Monitoring

The ISL97672 features extensive protection functions to cover all the perceivable failure conditions. The failure mode of a LED can be either open circuit or as a short. The behavior of an open circuited LED can additionally take the form of either infinite resistance or, for some LEDs, a zener diode, which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97672 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 1 for more details.

A fault condition that results in an input current that exceeds the devices electrical limits will result in a shutdown of all output channels.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are above approximately 5V (the action taken is described in Table 1).

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97672 monitors the current in each channel such that any string which reaches the intended output current is considered "good". Should the current subsequently fall below the target, the channel will be considered an "open circuit". Furthermore, should the boost output of the ISL97672 reaches the OVP limit or should the lower over-temperature threshold be reached, all channels which are not "good" will immediately be considered as "open circuit". Detection of an "open circuit" channel will result in a time-out before disabling of the affected channel. This time-out is sped up when the device is above the lower over-temperature threshold in an attempt to prevent the upper over-temperature trip point from being reached.

Some users employ some special types of LEDs that have zener diode structure in parallel with the LED for ESD

enhancement and enabling open circuit operation. When this type of LED is open circuited, the effect is as if the LED forward voltage has increased but no lighting. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, so as to make sure that multiple failures on one string do not cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channels look as if they have LED shorts. See Table 1 for details regarding responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as Equation 5:

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ. 5)}$$

These resistors should be large to minimize the power loss. For example, a 1MkΩ R_{UPPER} and 30kΩ R_{LOWER} sets OVP to 41.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the PWM Off time. Parallel capacitors should also be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 2.45V, the device will stop switching and be reset. Operation will restart only if the V_{IN} is back in the normal operating range.

Input Overcurrent Protection

During normal switching operation, the current through the internal boost power FET is monitored. If the current exceeds the current limit, the internal switch will be turned off. This monitoring happens on a cycle-by-cycle basis in a self protecting way.

Additionally, the ISL97672 monitors the voltage at the LX and OVP pins. At start-up, a fixed current is injected out of the LX pins and into the output capacitor. The device will not start-up unless the voltage at LX exceeds 1.2V. The OVP pin is also monitored such that if it rises above and subsequently falls below 20% of the target OVP level, the input protection FET will also be switched off.

Over-Temperature Protection (OTP)

The ISL97672 includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel which is outputting current at a level significantly below the regulation target will be treated as "open circuit" and disabled after a time-out period. This time-out period is also reduced to 800µs when it is above the lower threshold. The intention of the lower threshold is to allow bad channels to be isolated and disabled before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off. Once the device has cooled to approximately +100°C, the device will restart with the DC LED current level reduced to 75% of the initial setting. If the dissipation problem persists, subsequent hitting of the limit will cause identical behavior, with the current reduced in steps to 50% and finally 25%. Unless disabled via the EN pin, the device stays in an active state throughout.

For the extensive fault protection conditions, please refer to Figure 20 and Table 1 for details.

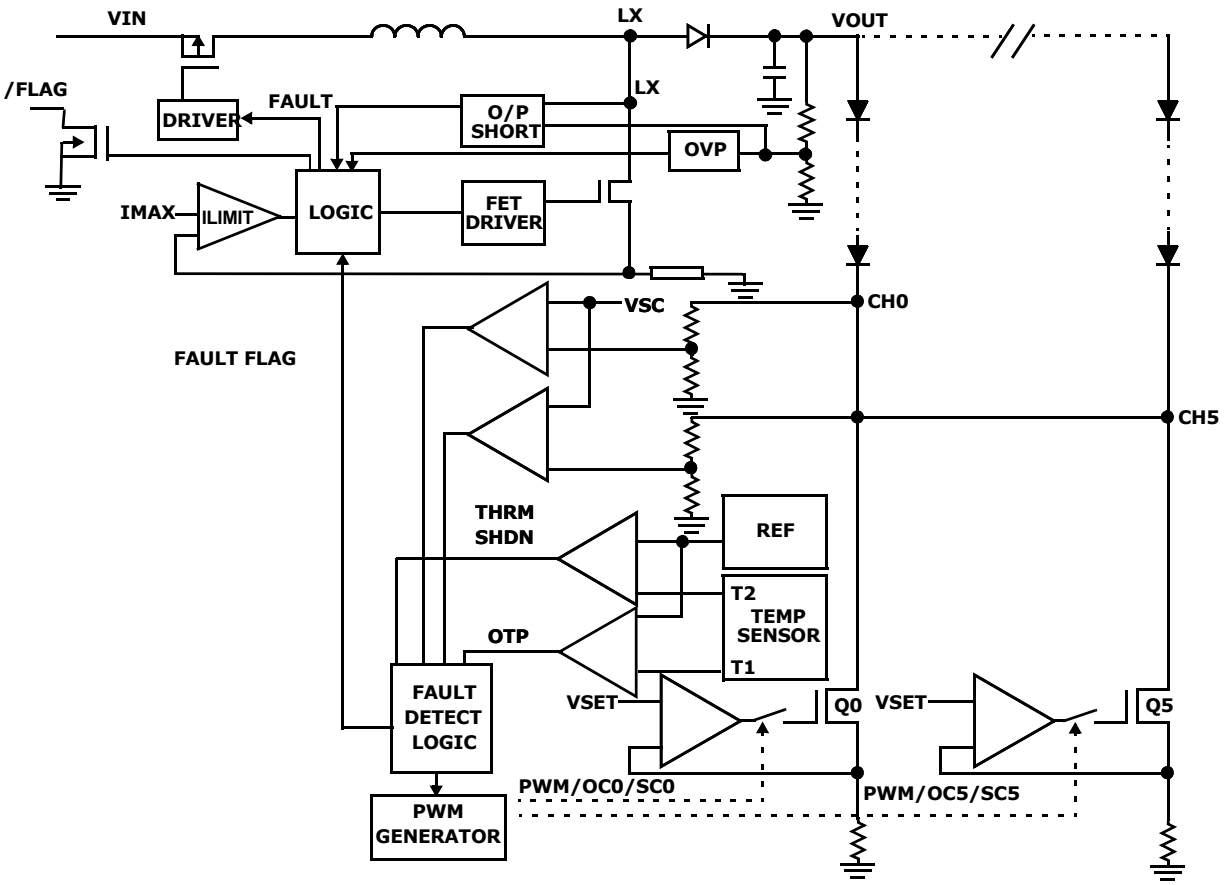


FIGURE 20. SIMPLIFIED FAULT PROTECTIONS

TABLE 1. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH0 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and CH0 < 4V	CH0 ON and burns power.	CH1 through CH5 Normal	Highest VF of CH1 through CH5
2	CH0 Short Circuit	Upper OTP triggered but VCH0 < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further.	Same as CH0	Highest VF of CH1 through CH5
3	CH0 Short Circuit	Upper OTP not triggered but CH0 > 4V	CH1 disabled after 6 PWM cycle time-out.	CH1 through CH5 Normal	Highest VF of CH1 through CH5
4	CH0 Open Circuit with infinite resistance	Upper OTP not triggered and CH0 < 4V	V_{OUT} will ramp to OVP. CH1 will time-out after 6 PWM cycles and switch off. V_{OUT} will drop to normal level.	CH1 through CH5 Normal	Highest VF of CH1 through CH5
5	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered and CH0 < 4V	CH1 remains ON and has highest VF, thus V_{OUT} increases.	CH1 through CH5 ON, Q1 through Q5 burn power	VF of CH0

TABLE 1. PROTECTIONS TABLE (Continued)

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
6	CH0 LED Open Circuit but has paralleled Zener	Upper OTP triggered but CH0 < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further	Same as CH0	VF of CH0
7	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered but CHx > 4V	CH0 remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases, then CH-X switches OFF after 6 PWM cycles. This is an unwanted shut off and can be prevented by setting OVP at an appropriate level.	VF of CH0
8	Channel-to-Channel ΔVF too high	Lower OTP triggered but CHx < 4V	Any channel at below the target current will fault out after 6 PWM cycles. Remaining channels driven with normal current.		Highest VF of CH0 through CH5
9	Channel-to-Channel ΔVF too high	Upper OTP triggered but CHx < 4V	All channels go off until chip cooled and then comes back on with current reduced to 76%. Subsequent OTP triggers will reduce I_{OUT} further		Highest VF of CH0 through CH5
10	Output LED stack voltage too high	V_{OUT} > VOVP	Any channel that is below the target current will time-out after 6 PWM cycles, and V_{OUT} will return to the normal regulation voltage required for other channels.		Highest VF of CH0 through CH5
11	V_{OUT}/LX shorted to GND at start-up or V_{OUT} shorted in operation	LX current and timing are monitored. OVP pins monitored for excursions below 20% of OVP threshold.	The chip is permanently shutdown 31mS after power-up if V_{OUT}/Lx is shorted to GND.		

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On time is equal to the change of inductor current during the switching regulator Off time. Since the voltage across an inductor is:

$$V_L = L \times \Delta I_L / \Delta t \quad \text{(EQ. 6)}$$

and ΔI_L @ On = ΔI_L @ Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \quad \text{(EQ. 7)}$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as Equations 8 and 9:

$$V_O/V_I = 1/(1 - D) \quad \text{(EQ. 8)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 9)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

In boost mode, input current flows continuously into the inductor, with an AC ripple component proportional to the rate of inductor charging only and smaller value input capacitors may be used. It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability.

Its maximum current capability must be adequate to handle the peak current at the worst case condition. If an inductor core is chosen with too low a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the fact that the voltage across the inductor during the Off period can be shown as Equation 10:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_S)] \quad \text{(EQ. 10)}$$

The choice of 85% is just an average term for the efficiency approximation. The first term is average current that is inversely proportional to the input voltage. The second term is inductor current change that is inversely proportional to L and f_S. As a result, for a given switching frequency and minimum input voltage the system operates, the inductor I_{SAT} must be chosen carefully. At a given inductor size, usually the larger the inductance, the higher the series resistance because of the extra winding of the coil. Thus the higher the inductance, the lower the peak current capability. The ISL97672 current limit may also have to be taken into account.

Output Capacitors

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor for I_{LPEAK} during FET On and the voltage drop due to flowing through the ESR of the output capacitor. The ripple voltage can be shown as Equation 11:

$$\Delta V_{CO} = (I_O/C_O \times D/f_S) + ((I_O \times ESR) \quad \text{(EQ. 11)}$$

The conservation of charge principle in Equation 9 also brings up a fact that during the boost switch Off period, the output capacitor is charged with the inductor ripple current minus a relatively small output current in boost topology. As a result, the user needs to select an output capacitor with low ESR and with a enough input ripple current capability.

Output Ripple

ΔV_{Co} can be reduced by increasing C_O or f_S, or using small ESR capacitors. In general, ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

A larger output capacitor will also ease the driver response during PWM dimming Off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost harder in the next On period that minimizes transient current. The output capacitor is also needed for compensation, and in general, 2x4.7µF/50V ceramic capacitors are suitable for the notebook display backlight applications.

Schottky Diode

A high speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current will minimize losses, making Schottky diodes the preferred choice. Although the Schottky diode turns on only during the boost switch Off period, it carries the same peak current as the inductor's, and therefore, a suitable current rated Schottky diode must be used.

Applications

High Current Applications

Each channel of the ISL97672 can support up to 30mA. For applications that need higher current, multiple channels can be grouped to achieve the desirable current. For example, the cathode of the last LED can be connected to CH0 to CH2; this configuration can be treated as a single string with 90mA current driving capability.

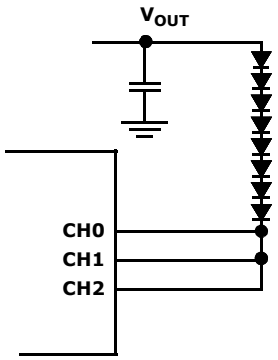


FIGURE 21. GROUPING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

Compensation

The ISL97672 has two main elements in the system; the Current Mode Boost Regulator and the op amp based multi-channel current sources. The ISL97672 incorporates a transconductance amplifier in its feedback path to allow the user some levels of adjustment on the transient response and better regulation. The ISL97672 uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The compensation network is a series Rc, Cc1 network from COMP pin to ground and an optional Cc2 capacitor connected to the COMP pin. The Rc sets the high frequency integrator gain for fast transient response and the Cc1 sets the integrator zero to ensure loop stability. For most applications, Rc is in the range of 15kΩ and Cc1 is in the range of 2.2nF. Depends on the PCB layout, a Cc2, in range of 47pF, may be needed to create a pole to cancel the output capacitor ESR's zero effect for stability.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
11/1/10	FN7632.1	Corrected part marking in "Ordering Information" on page 3 from "97672" to "7672" In "Thermal Information" on page 4 changed: "Maximum Continuous Junction Temperature . . . . . +125°C To: Absolute Maximum Junction Temperature . . . . . +150°C Recommended Max Operating Junction Temperature. . +125°C Added "Related Literature*(see page 16)" on page 1. Added "Latch Up (Tested per JESD-78B; Class 2, Level A) 100mA" on page 4
6/24/10	FN7632.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL97672

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

For additional products, see www.intersil.com/product_tree

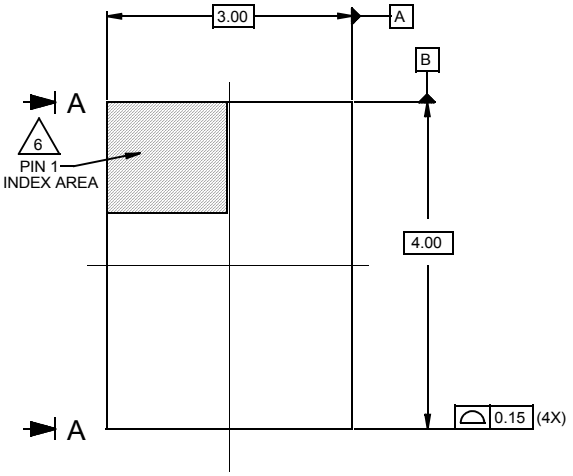
Intersil products are manufactured, assembled and tested utilizing ISO9000 quality systems as noted in the quality certifications found at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com

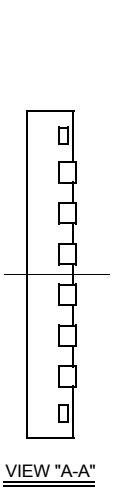
Package Outline Drawing

L20.3x4

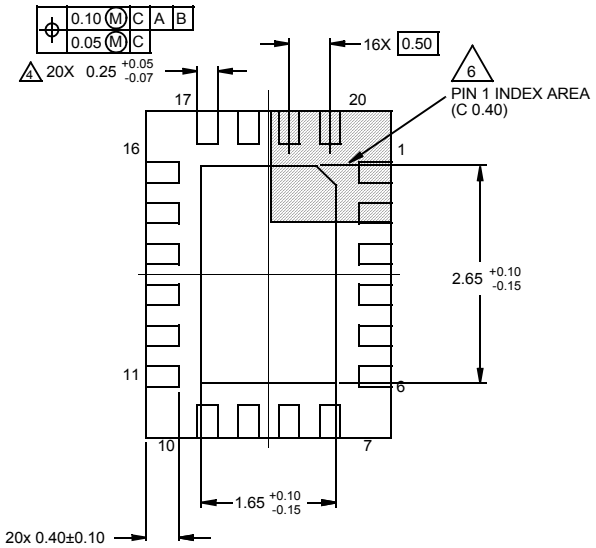
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/10



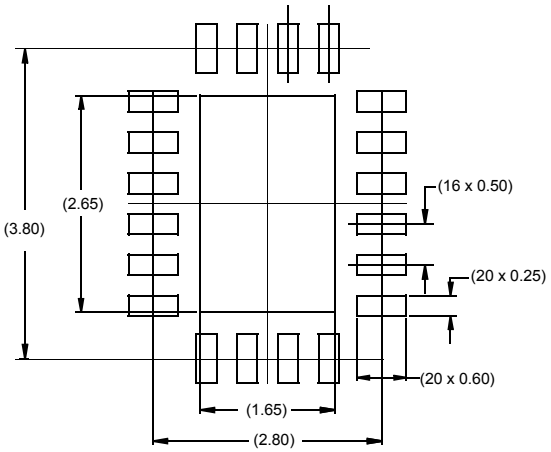
TOP VIEW



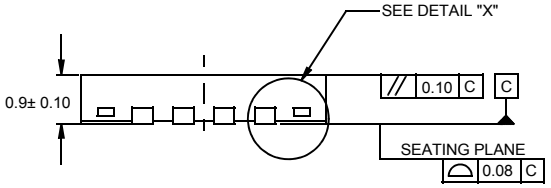
VIEW "A-A"



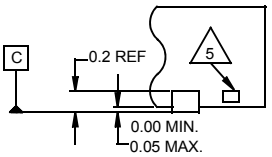
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.