19-1054; Rev 0; 1/08

EVALUATION KIT AVAILABLE

Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

General Description

The MAX16816 is a current-mode, high-brightness LED (HB LED) driver designed to control two external n-channel MOSFETs for single-string LED current regulation. The MAX16816 integrates all the building blocks necessary to implement fixed-frequency HB LED drivers with wide-range dimming control and EEPROM-programmable LED current binning with a factor of up to 1.6. This device is configurable to operate as a step-down (buck), step-up (boost), or step-up/step-down (buck-boost) current regulator.

Current-mode control with adjustable leading-edge blanking simplifies control-loop design. Adjustable slope compensation stabilizes the current loop when operating at duty cycles above 50%. The MAX16816 operates over a wide input voltage range and is capable of withstanding automotive load-dump events. Multiple MAX16816 devices can be synchronized to each other or to an external clock. The MAX16816 includes a floating dimming driver for brightness control with an external n-channel MOSFET in series with the LED string.

HB LEDs using the MAX16816 can achieve efficiencies of over 90% in automotive applications. The MAX16816 also includes a 1.4A source and 2A sink gate driver for driving switching MOSFETs in high-power LED driver applications, such as front light assemblies. Dimming control allows for wide PWM dimming range at frequencies up to 5kHz. Higher dimming ratios (up to 1000:1) are achievable at lower dimming frequencies.

The MAX16816 provides user-programmable features through on-chip nonvolatile EEPROM registers. Adjustable features include a programmable soft-start, LED current (binning), external MOSFET gate driver supply voltage, slope compensation, leading-edge blanking time, and disabling/enabling of the RT oscillator.

The MAX16816 is available in a 32-pin TQFN package with exposed pad and operates over the -40°C to +125°C automotive temperature range.

Applications

Automotive Exterior: Rear Combination Lights (RCL), Daytime Running Lights (DRL), Fog and Front Lighting, High-Beam/Low-Beam/Turn Lights

General Illumination

Navigation and Marine Indicators

Neon Replacement, Emergency Lighting

Signage and Beacons

Features

- **EEPROM-Programmable LED Current Binning**
- **Wide Input Range: 5.9V to 76V with Cold Start Operation to 5.4V**
- **Integrated Floating Differential LED Current-Sense Amplifier**
- **Floating Dimming Driver Capable of Driving an n-Channel MOSFET**
- **5% or Better LED Current Accuracy**
- **Multiple Topologies: Buck, Boost, Buck-Boost, SEPIC**
- **Resistor-Programmable Switching Frequency (125kHz to 500kHz) and Synchronization Capability**
- **200Hz On-Board Ramp Allows Analog-Controlled PWM Dimming and External PWM Dimming**
- **Output Overvoltage, Overcurrent, and LED Short Protection**
- **Enable/Shutdown Input with Shutdown Current Below 45µA**

Ordering Information

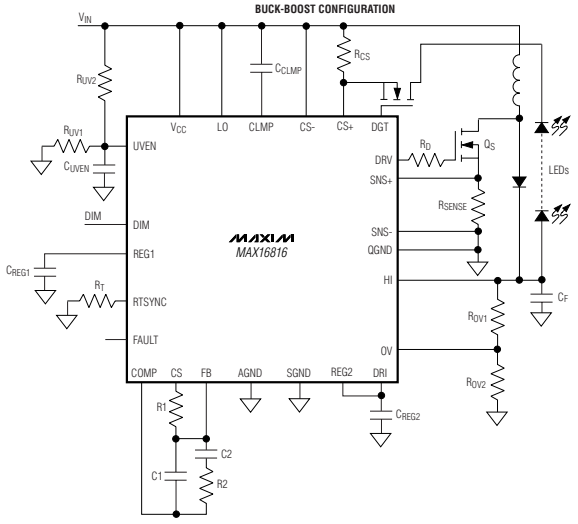
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX16816ATJ+	-40°C to +125°C	32 TQFN-EP*	T3255M-4

+Denotes a lead-free package.

***EP = Exposed pad.*

Pin Configuration appears at end of data sheet.

Typical Operating Circuits



Typical Operating Circuits continued at end of data sheet.

For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

ABSOLUTE MAXIMUM RATINGS

V_{CC}, HI, LO, CLMP to QGND .....-0.3V to +80V
CS+, CS-, DGT, UVEN, $\overline{FAULT}$ to QGND.....-0.3V to +80V
UVEN to QGND .....-0.3V to (V_{CC} + 0.3V)
DRV to SGND .....-0.3V to +18V
DRI, REG2, DIM to AGND .....-0.3V to +18V
QGND, SGND to AGND .....-0.3V to +0.3V
SNS+ to SNS- .....-0.3V to +6V
CS, FB, COMP, SNS+, SNS-, OV, REF, RTSYNC to AGND .....-0.3V to +6V
REG1, CLKOUT to AGND .....-0.3V to +6V
CS+ to CS- .....-0.3V to +12V
HI to LO .....-0.3V to +36V
CS+, CS-, DGT, CLMP to LO .....-0.3V to +12V
CS+, CS-, DGT, CLMP to LO .....-0.3V to (HI + 0.3V)
HI to CLMP .....-0.3V to +28V
Continuous Power Dissipation* (T_A = +70°C)
32-Pin TQFN (derate 34.5mW/°C above +70°C) 2758mW
Thermal Resistance
θ_{JA}.....29°C/W
θ_{JC}.....1.7°C/W
Operating Temperature Range .....-40°C to +125°C
Maximum Junction Temperature .....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

**As per JEDEC 51 standard, Multilayer Board (PCB).*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 1µF, C_{CLMP} = 0.1µF, R_T = 25kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{CC}		5.5		76	V
Supply Current to V_{CC}	I_{Q_VCC}	Exclude current to the gate driver, I_{REG2}		2.7	4.5	mA
Supply Current to HI	I_{Q_HI}	V_{HI} = 14V		0.5	1.0	mA
Shutdown Current to V_{CC}	I_{SHDN_VCC}	V_{UVEN} ≤ 300mV		25	45	µA
Shutdown Current to HI	I_{SHDN_HI}	V_{UVEN} ≤ 300mV		1	10	µA
UVEN						
V_{CC} UVLO Threshold	V_{CC_R}	V_{CC} rising	5.5		6.0	V
	V_{CC_F}	V_{CC} falling	5.0		5.5	
V_{CC} Threshold Hysteresis	V_{CC_HYS}			0.4		V
UVEN Threshold	V_{UVR}	V_{UVEN} rising	1.10	1.244	1.36	V
	V_{UVF}	V_{UVEN} falling	1.00	1.145	1.26	
UVEN Input Current	I_{UVEN}	(V_{UVEN} = 0V and V_{CC} = 14V) (V_{UVEN} = 76V and V_{CC} = 77V)	-0.2		+0.2	µA
REGULATORS						
REG1 Regulator Output	V_{REG1}	0 < I_{REG1} < 2mA, 7.5V < V_{CC} < 76V	4.75	5.00	5.25	V
		I_{REG1} = 2mA, V_{CC} = 5.7V	4.00	4.50	5.25	
REG1 Dropout Voltage		I_{REG1} = 2mA (Note 1)		0.5	1.0	V
REG1 Load Regulation	ΔV/ΔI	V_{CC} = 7.5V, I_{REG1} = 0 to 2mA			25	Ω
REG2 Dropout Voltage		V_{CC} ≥ 9.5V, REG2 control register is '0011', I_{REG2} = 20mA (Note 1)		0.5	1.0	V
REG2 Load Regulation	ΔV/ΔI	V_{CC} ≥ 9.5V, REG2 control register is '0011', I_{REG2} = 0 to 20mA			25	Ω

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 1µF, C_{CLMP} = 0.1µF, R_T = 25kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
REG2 Regulation Voltage		REG2 control register is '0000', V_{CC} ≥ 7.5V, I_{REG2} = 1mA	4.75	5	5.25	V
		REG2 control register is '0011', V_{CC} ≥ 9.5V, I_{REG2} = 1mA	6.65	7.0	7.35	
		REG2 control register is '1111', V_{CC} ≥ 17.5V, I_{REG2} = 1mA	13.5	15	16.5	
		REG2 control register is '0000', V_{CC} = 5.7V, 0 ≤ I_{REG2} ≤ 20mA	4	4.5	5.25	
		REG2 control register is '0000', V_{CC} = 7.5V, 0 ≤ I_{REG2} ≤ 20mA	4.75	5	5.25	
		REG2 control register is '1111', V_{CC} = 17.5V, 0 ≤ I_{REG2} ≤ 20mA	13.5	15	16.5	
HIGH-SIDE REGULATOR (CLMP) (All voltages referred to V_{LO}) (Note 2)						
CLMP UVLO Threshold	V_{CLMP_TH}	V_{CLMP} rising	2.0	2.5	3.0	V
CLMP UVLO Threshold Hysteresis	V_{CLMP_HYS}			0.22		V
CLMP Regulator Output Voltage	V_{CLMP}	8.7V ≤ (V_{HI} - V_{LO}) ≤ 36V, I_{CLMP} = 1mA	5.5	8.0	10.0	V
		5.0V ≤ (V_{HI} - V_{LO}) ≤ 8.7V, I_{CLMP} = 250µA		(V_{HI} - V_{LO}) - 0.7		
CURRENT-SENSE AMPLIFIER (CSA)						
Differential Input Voltage Range	V_{CS+} - V_{CS-}		0		0.3	V
Common-Mode Range		V_{CC} ≤ 68V	0		V_{CC}	V
CS+ Input Bias Current	I_{CS+}	V_{CS+} = 0.3V, V_{CS-} = 0V	-250		+250	nA
CS- Input Bias Current	I_{CS-}	V_{CS+} = 0.3V, V_{CS-} = 0V			400	µA
Unity-Gain Bandwidth		From (CS+ to CS-) to CS		1.0		MHz
REF OUTPUT BUFFER						
REF Output Voltage	V_{REF}	-100µA ≤ I_L ≤ +100µA	2.85	3.0	3.15	V
DIM DRIVER						
Minimal Pulse Width		f_{DIM} = 200Hz (Note 3)		20	40	µs
Source Current		V_{CLMP} - V_{LO} = 4V	5	20		mA
		V_{CLMP} - V_{LO} = 8V	30	67		
Sink Current		V_{CLMP} - V_{LO} = 4V	10	22		mA
		V_{CLMP} - V_{LO} = 8V	40	76		
GATE DRIVER						
DRI Voltage Range	V_{DRI}	V_{CC} ≥ 2.5V above V_{DRI}	5		15	V
DRI UVLO Threshold	V_{UVLO_TH}		4.0	4.2	4.4	V
DRI UVLO Threshold Hysteresis	V_{UVLO_HYST}			0.3		V

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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 1µF, C_{CLMP} = 0.1µF, R_T = 25kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Output Impedance	Z_{OUT_L}	V_{DRI} = 7.0V, DRV sinking 250mA		2.8	4	Ω
	Z_{OUT_H}	V_{DRI} = 7.0V, DRV sourcing 250mA		5.0	8	
Peak Sink Current	I_{SK}	V_{DRI} = 7.0V		2.5		A
Peak Source Current	I_{SR}	V_{DRI} = 7.0V		1.4		A
PWM, ILIM, AND HICCUP COMPARATOR						
PWM Comparator Offset Voltage		V_{COMP} - (V_{SNS+} -V_{SNS-})		0.8		V
Peak Current-Limit Comparator Trip Threshold			160	200	245	mV
Peak Current-Limit Comparator Propagation Delay (Excluding Blanking Time)		50mV overdrive		40		ns
HICCUP Comparator Trip Threshold			235	300	385	mV
SNS+ Input Bias Current		V_{SNS+} = 0V, V_{SNS-} = 0V	-100	-65		µA
SNS- Input Bias Current		V_{SNS+} = 0V, V_{SNS-} = 0V	-100	-65		µA
BLANKING TIME						
Blanking Time		Blanking Time Control Register is '00'		150		ns
		Blanking Time Control Register is '01'		125		
		Blanking Time Control Register is '10'		100		
		Blanking Time Control Register is '11'		75		
ERROR AMPLIFIER						
FB Input Bias Current		V_{FB} = 1V	-100		+100	nA
EAMP Output Sink Current		V_{FB} = 1.735V, V_{COMP} = 1V	3	7		mA
EAMP Output Source Current		V_{FB} = 0.735V, V_{COMP} = 1V	2	7		mA
EAMP Input Common-Mode Voltage	V_{COM}	(Note 5)	0		1.6	V
EAMP Output Clamp Voltage			1.3	2.0	2.7	V
Voltage Gain	A_V	R_{COMP} = 100kΩ to AGND		80		dB
Unity-Gain Bandwidth	GBW	R_{COMP} = 100kΩ to AGND, C_{COMP} = 100pF to AGND		0.5		MHz
OSCILLATOR, OSC SYNC, CLK, AND CLKOUT						
SYNC Frequency Range	f_{SW_MIN}				125	kHz
	f_{SW_MAX}		500			
RTSYNC Oscillator Frequency		RTOF bit set to '0', R_T = 100kΩ	106	125	143	kHz
		RTOF bit set to '0', R_T = 25kΩ	475	500	525	
SYNC High-Level Voltage	V_{SIHL}		2.8			V
SYNC Low-Level Voltage	V_{SILL}				0.4	V

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 1µF, C_{CLMP} = 0.1µF, R_T = 25kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLKOUT High Level		I_{SINK} = 0.8mA	2.8			V
CLKOUT Low Level		I_{SOURCE} = 1.6mA			0.4	V
CLKOUT Maximum Load Capacitance	C_{CLK_CAP}	f_{SW} = 500kHz			500	pF
DIM SYNC, DIM RAMP, AND DIM PWM GEN						
Internal RAMP Frequency	f_{RAMP}		160	200	240	Hz
External Sync Frequency Range	f_{DIM}		80		2000	Hz
External Sync Low-Level Voltage	V_{LTH}				0.4	V
External Sync High-Level Voltage	V_{HTH}		3.2			V
DIM Comparator Offset	V_{DIMOS}		170	200	300	mV
DIGITAL SOFT-START AND BINNING						
Soft-Start Duration	t_{SS}	Digital Soft-Start Duration register is ‘000’		4096		µs
		Digital Soft-Start Duration register is ‘001’		2048		
		Digital Soft-Start Duration register is ‘010’		1536		
		Digital Soft-Start Duration register is ‘011’		1024		
		Digital Soft-Start Duration register is ‘100’		768		
		Digital Soft-Start Duration register is ‘101’		512		
		Digital Soft-Start Duration register is ‘110’		256		
		Digital Soft-Start Duration register is ‘111’		0		
Binning Range		Binning Adjustment register is ‘0000’		100.00		mV
		Binning Adjustment register is ‘0001’		106.67		
		Binning Adjustment register is ‘0010’		113.33		
		Binning Adjustment register is ‘0011’		120.00		
		Binning Adjustment register is ‘0100’		126.67		
		Binning Adjustment register is ‘0101’		133.33		
		Binning Adjustment register is ‘0110’		140.00		
		Binning Adjustment register is ‘0111’		146.67		
		Binning Adjustment register is ‘1000’		153.33		
		Binning Adjustment register is ‘1001’		160.00		
		Binning Adjustment register is ‘1010’		166.67		
OVERVOLTAGE COMPARATOR, LOAD OVERCURRENT COMPARATOR						
OVP Overvoltage Comparator Threshold	V_{OV}	V_{OV} rising	1.20	1.235	1.27	V
OVP Overvoltage Comparator Hysteresis	V_{OV_HYST}			63.5		mV

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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 1µF, C_{CLMP} = 0.1µF, R_T = 25kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SLOPE COMPENSATION						
Slope Compensation Peak-to-Peak Voltage Per Cycle		Slope Compensation register is '0000', clock generated by R_T		0		mV/cycle
		Slope Compensation register is '0001', clock generated by R_T		20		
		Slope Compensation register is '0010', clock generated by R_T		40		
		Slope Compensation register is '0011', clock generated by R_T		60		
		Slope Compensation register is '0100', clock generated by R_T		80		
		Slope Compensation register is '0101', clock generated by R_T		100		
		Slope Compensation register is '0110', clock generated by R_T		120		
		Slope Compensation register is '0111', clock generated by R_T		140		
		Slope Compensation register is '1000', clock generated by R_T		160		
		Slope Compensation register is '1001', clock generated by R_T		180		
		Slope Compensation register is '1010', clock generated by R_T		200		
		Slope Compensation register is '1011', clock generated by R_T		220		
		Slope Compensation register is '1100', clock generated by R_T		240		
		Slope Compensation register is '1101', clock generated by R_T		260		
		Slope Compensation register is '1110', clock generated by R_T		280		
		Slope Compensation register is '1111', clock generated by R_T		300		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 1µF, C_{CLMP} = 0.1µF, R_T = 25kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Slope Compensation		Slope Compensation register is '0000', external clock applied to RTSYNC		0		mV/µs
		Slope Compensation register is '0001', external clock applied to RTSYNC		2		
		Slope Compensation register is '0010', external clock applied to RTSYNC		4		
		Slope Compensation register is '0011', external clock applied to RTSYNC		6		
		Slope Compensation register is '0100', external clock applied to RTSYNC		8		
		Slope Compensation register is '0101', external clock applied to RTSYNC		10		
		Slope Compensation register is '0110', external clock applied to RTSYNC		12		
		Slope Compensation register is '0111', external clock applied to RTSYNC		14		
		Slope Compensation register is '1000', external clock applied to RTSYNC		16		
		Slope Compensation register is '1001', external clock applied to RTSYNC		18		
		Slope Compensation register is '1010', external clock applied to RTSYNC		20		
		Slope Compensation register is '1011', external clock applied to RTSYNC		22		
		Slope Compensation register is '1100', external clock applied to RTSYNC		24		
		Slope Compensation register is '1101', external clock applied to RTSYNC		26		
		Slope Compensation register is '1110', external clock applied to RTSYNC		28		
		Slope Compensation register is '1111', external clock applied to RTSYNC		30		

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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 1µF, C_{CLMP} = 0.1µF, R_T = 25kΩ, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{FAULT}$ I/O						
$\overline{FAULT}$ Leakage Current		5.5V < $V_{\overline{FAULT}}$ < 76V	-1		+1	µA
$\overline{FAULT}$ Input Low Current		$V_{\overline{FAULT}}$ = 0V		500		µA
$\overline{FAULT}$ Pulldown Current		$V_{\overline{FAULT}}$ = 2V	0.7	1.2	1.8	mA
$\overline{FAULT}$ Pulldown Input Logic-Low	V_{IL}				0.4	V
$\overline{FAULT}$ Output Logic-High		Sourcing 10µA	2.8			V
$\overline{FAULT}$ Output Logic-Low		Sinking 10µA			0.4	V
Programming Slot at Power-Up		V_{UVEN} > 1.244V and V_{CC} > 5.9V (Note 4)	6.4	8.0		ms
THERMAL SHUTDOWN						
Thermal Shutdown Temperature	T_{J_SHDN}			+165		°C
Thermal Shutdown Hysteresis	ΔT_{J_SHDN}			20		°C
EEPROM						
Data Retention	t_{DR}	T_A = +125°C (Note 5)	10			years
EEPROM Write Time	t_{WRA}	(Note 5)			14	ms
Endurance		T_A = +85°C, read and write (Note 5)	50k			cycles

ELECTRICAL CHARACTERISTICS – 1-Wire® System

(C_{REG1} = 1µF, C_{REG2} = 1µF, T_A = T_J = -40°C to +125°C, unless otherwise noted. Typical specifications are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
I/O GENERAL DATA						
1-Wire Time Slot Duration	t_{SLOT}		65			µs
Recovery Time	t_{REC}	(Note 6)	5			µs
I/O, 1-Wire RESET, PRESENCE DETECT CYCLE						
Reset Low Time	t_{RSTL}		480		640	µs
Presence Detect Sample Time	t_{MSP}		65		75	µs
I/O, 1-Wire WRITE						
Write-0 Low Time	t_{W0L}		60			µs
Write-1 Low Time	t_{W1L}		5		15	µs
I/O, 1-Wire READ						
Read Low Time	t_{RL}		5		10	µs
Read Sample Time	t_{MSR}		12		15	µs

1-Wire is a registered trademark of Dallas Semiconductor Corp., a wholly owned subsidiary of Maxim Integrated Products, Inc.

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ELECTRICAL CHARACTERISTICS

Note 1: Dropout voltage is defined as the input to output differential voltage at which the output voltage drops 100mV below its nominal value measured at output.

Note 2: V_{CLMP_TH} determines the voltage necessary to operate the current-sense amplifier. The DIM driver requires 2.5V for (V_{CLMP} - V_{LO}) to drive a FET. V_{HI} is typically one diode drop above V_{CLMP}. A large capacitor connected to V_{CLMP} slows the response of the LED current-sense circuitry, resulting in current overshoot. To ensure proper operation, connect a 0.1µF capacitor from CLMP to LO.

Note 3: Minimum pulse width required to guarantee proper dimming operation.

Note 4: $\overline{FAULT}$ multiplexes a programming interface and fault indication functionality. At power-up initialization, an internal timer enables $\overline{FAULT}$ and two programming passcodes must be entered within the programming slot to enter programming mode. If the programming passcodes are not received correctly within the programming slot, $\overline{FAULT}$ goes back towards fault indication. Cycling power to the device is required to re-attempt entry into programming mode.

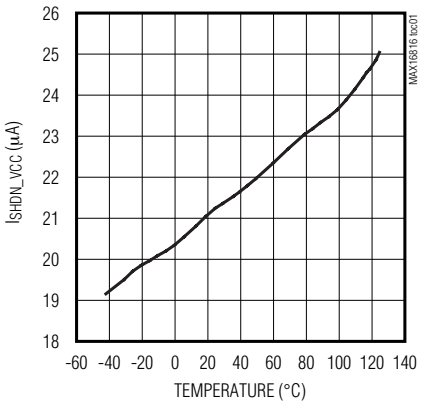
Note 5: Not production tested. Guaranteed by design.

Note 6: Recovery time is the time required for $\overline{FAULT}$ to be pulled high by the internal 10kΩ resistor.

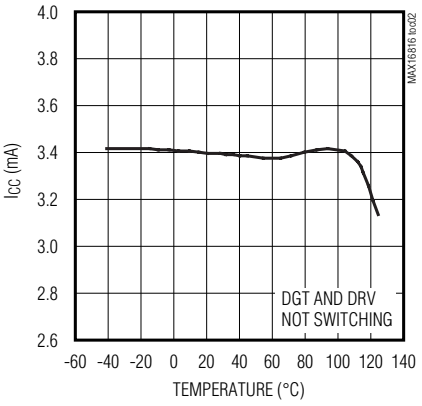
Typical Operating Characteristics

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 10µF, C_{CLMP} = 0.1µF, R_{CS} = 0.1Ω, Binning adjustment register is '0000', T_A = +25°C, unless otherwise noted.)

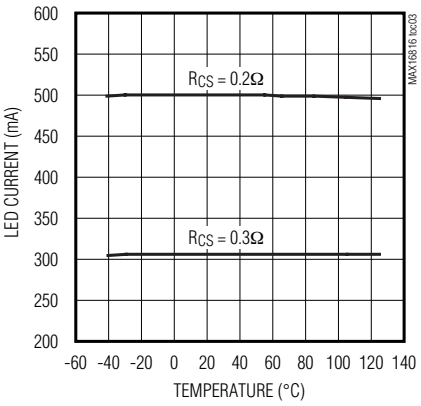
SHUTDOWN CURRENT vs. TEMPERATURE



OPERATING CURRENT vs. TEMPERATURE



OUTPUT CURRENT vs. TEMPERATURE



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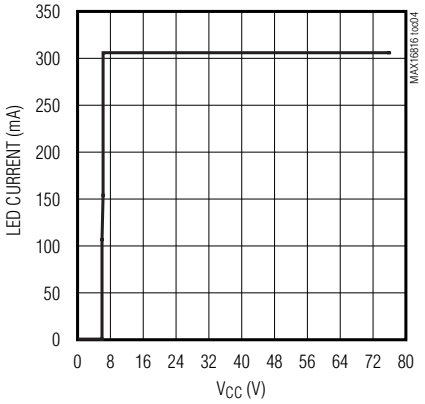
Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

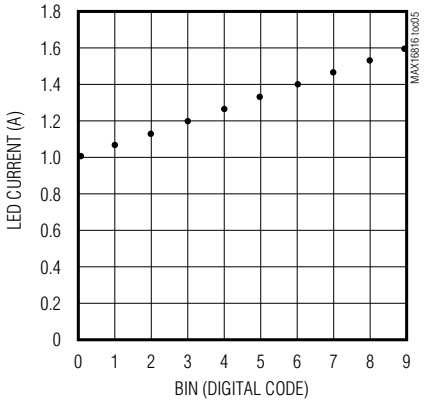
Typical Operating Characteristics (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 10µF, C_{CLMP} = 0.1µF, R_{CS} = 0.1Ω, Binning adjustment register is '0000', T_A = +25°C, unless otherwise noted.)

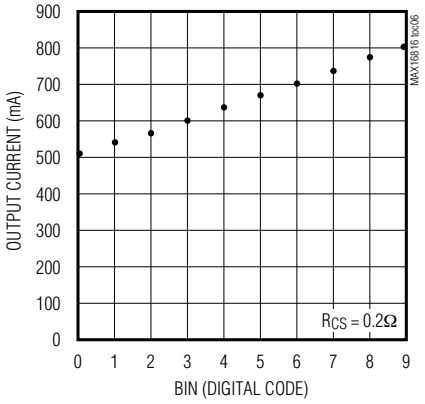
OUTPUT CURRENT vs. SUPPLY VOLTAGE



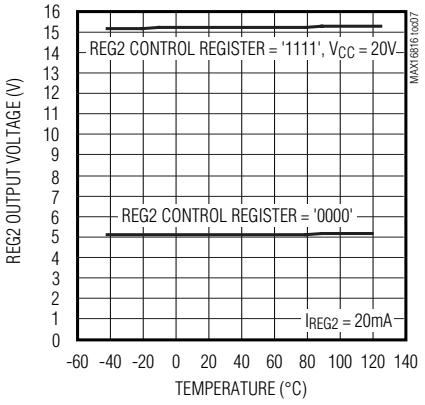
OUTPUT CURRENT vs. BINNING CODES



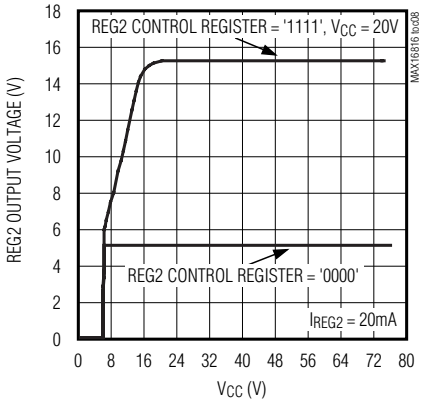
OUTPUT CURRENT vs. BINNING CODES



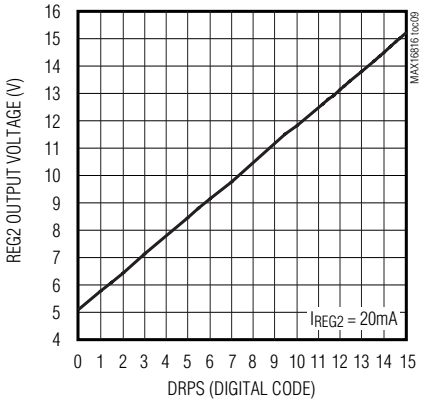
REG2 OUTPUT VOLTAGE vs. TEMPERATURE



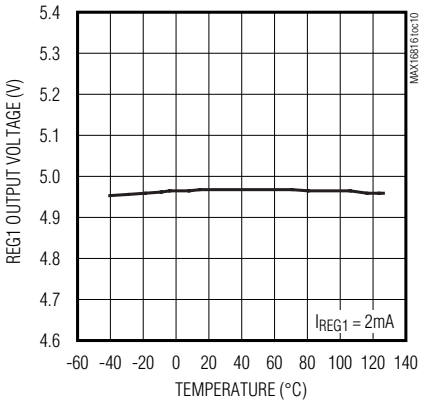
REG2 OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



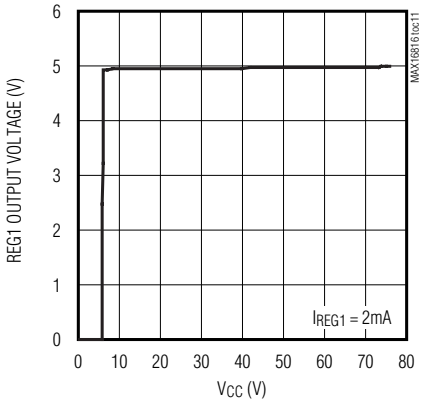
REG2 OUTPUT VOLTAGE vs. REG2 CONTROL REGISTER



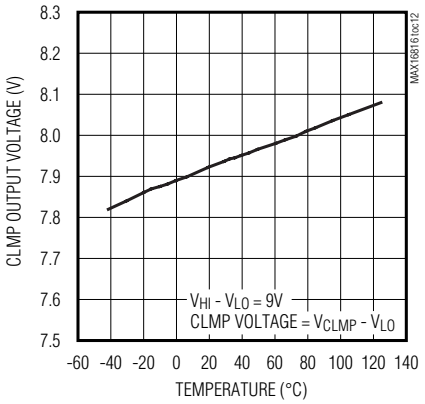
REG1 OUTPUT VOLTAGE vs. TEMPERATURE



REG1 OUTPUT VOLTAGE vs. SUPPLY VOLTAGE



CLMP OUTPUT VOLTAGE vs. TEMPERATURE



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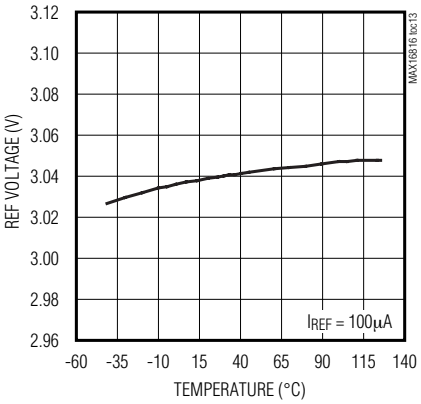
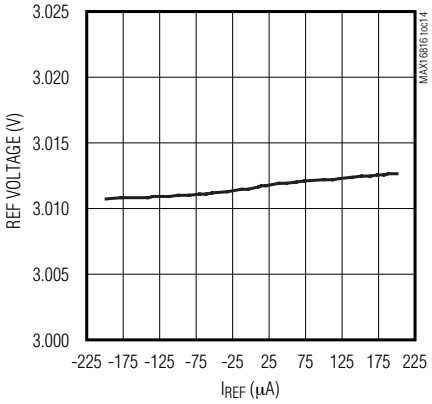
Typical Operating Characteristics (continued)

(V_{CC} = V_{UVEN} = 14V, C_{REG1} = 1µF, C_{REG2} = 10µF, C_{CLMP} = 0.1µF, R_{CS} = 0.1Ω, Binning adjustment register is '0000', T_A = +25°C, unless otherwise noted.)

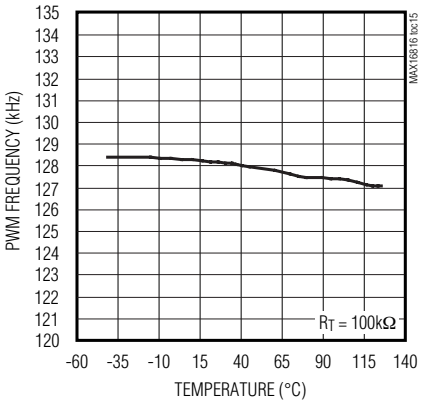
REF VOLTAGE vs. TEMPERATURE



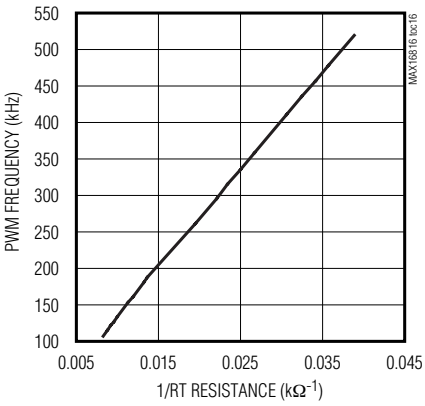
REF VOLTAGE vs. SINK CURRENT



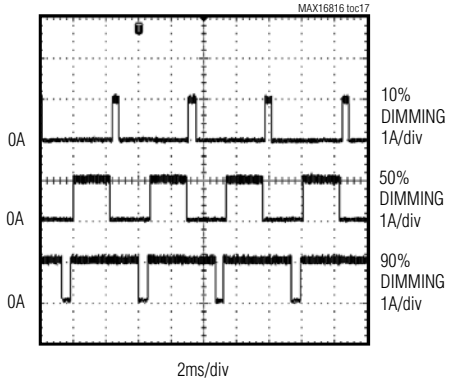
PWM OSCILLATION FREQUENCY vs. TEMPERATURE



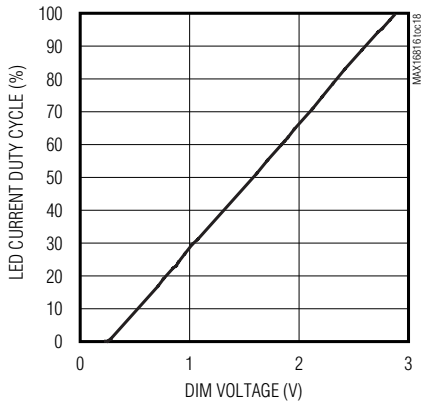
RT RESISTANCE vs. PWM FREQUENCY



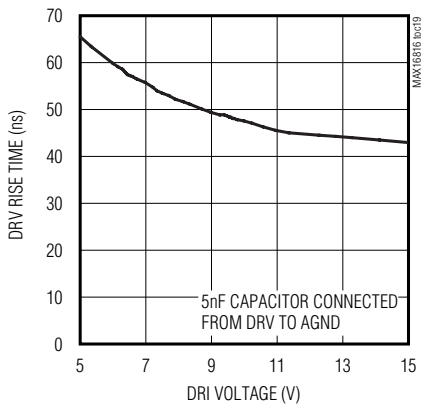
200Hz DIMMING OPERATION



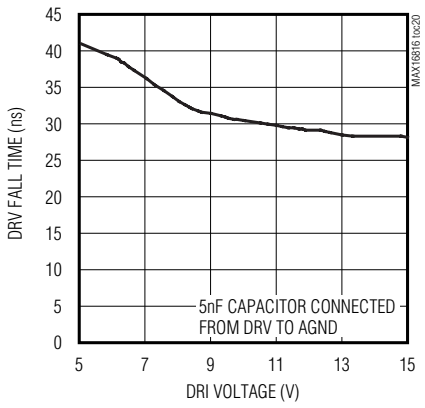
LED CURRENT DUTY CYCLE vs. DIM VOLTAGE



DRIVER DRV RISE TIME vs. DRI VOLTAGE



DRIVER DRI FALL TIME vs. DRI VOLTAGE



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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

Pin Description

PIN	NAME	FUNCTION
1, 24	N.C.	No Connection. Not internally connected.
2	UVEN	Undervoltage Lockout (UVLO) Threshold/Enable Input. UVEN is a dual-function adjustable UVLO threshold input with an enable feature. Connect UVEN to V_{CC} through a resistive voltage-divider to program the UVLO threshold. Connect UVEN directly to V_{CC} to use the 5.9V (max) default UVLO threshold. Apply a voltage greater than 1.244V to UVEN to enable the device.
3	REG1	5V Regulator Output. REG1 is an internal low-dropout voltage regulator that generates a 5V (V_{CC} > 6V) output voltage and supplies power to internal circuitry. Bypass REG1 to AGND through a 1µF ceramic capacitor.
4	AGND	Analog Ground. Use proper single-point ground design and decoupling to avoid ground impedance loop errors.
5	REF	Accurate 3V Buffered Reference Output. Connect REF to DIM through a resistive voltage-divider to apply a DC voltage for analog-controlled dimming functionality. Leave REF unconnected if unused.
6	DIM	Dimming Control Input. Connect DIM to an external PWM signal for PWM dimming. For analog-controlled dimming, connect DIM to REF through a resistive voltage-divider. The dimming frequency is 200Hz under these conditions. Connect DIM to AGND to turn off the LEDs.
7	RTSYNC	Sync Input/Output. The internal PWM clock is selectable through the RTOF EEPROM bit. Connect an external resistor to RTSYNC and set the RTOF register to '0' to select a clock frequency between 125kHz and 500kHz. Set RTOF register to '0' and connect RTSYNC to an external clock to synchronize the device with external clock. Set RTOF register to '1' to use the fixed 125kHz oscillator. Under these conditions, RTSYNC is powered off and may be left in any state. See the *Oscillator, Clock, and Synchronization* section.
8	CLKOUT	Clock Output. CLKOUT buffers the oscillator/clock. Connect CLKOUT to the SYNC input of another device to operate the MAX16816 in a multichannel configuration. CLKOUT is a logic output.
9, 10, 11	I.C.	Internally Connected. Must be connected to AGND.
12	COMP	Error-Amplifier Output. Connect the compensation network from COMP to FB for stable closed-loop control. Use low-leakage ceramic capacitors in the feedback network.
13	CS	Current-Sense Voltage Output. CS outputs a voltage proportional to the current sensed through the current-sense amplifier. Connect CS through a passive network to FB as dictated by the chosen compensation scheme.
14	FB	Error-Amplifier Inverting Input
15	OV	Overvoltage Protection Input. Connect OV to HI through a resistive voltage-divider to set the overvoltage limit for the load. When the voltage at OV exceeds the 1.235V (typ) threshold, an overvoltage fault is generated and the switching MOSFET turns off. The MOSFET is turned on again when the voltage at OV drops below 1.17V (typ).
16, 17	SGND	Switching Ground. SGND is the ground for non-analog and high-current gate-driver circuitry.
18	DRV	Gate-Driver Output. Connect DRV through a series resistor to the gate of an external n-channel MOSFET to reduce EMI. DRV can sink 1A or source 0.5A.
19	DRI	Gate-Driver Supply Input. Connect DRI to REG2 to power the primary switching MOSFET driver.
20	SNS+	Positive Peak Current-Sense Input. Connect SNS+ to the positive side of the switch current-sense resistor, R_{SENSE}.

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Pin Description (continued)

PIN	NAME	FUNCTION
21	SNS-	Negative Peak Current-Sense Input. Connect SNS- to the negative side of the switch current-sense resistor, R_{SENSE}.
22	QGND	Analog Ground. Ensure a low-impedance connection between QGND and AGND.
23	DGT	Dimming Gate-Driver Output. Connect DGT to the gate of an external n-channel MOSFET for dimming. DGT is powered by the internal regulator, CLAMP, and is referenced to LO.
25	LO	Low-Voltage Input. LO is the return point for the LED current. When using the MAX16816 in a buck-boost configuration, connect LO to V_{CC}. When using the device in a boost configuration only, connect LO to AGND. Connect LO to the junction of the inductor and LED current-sense resistor, R_{CS}, when using a buck configuration.
26	CS+	Noninverting Current-Sense Amplifier Input. Connect CS+ to the positive side of an external sense resistor, R_{CS}, connected in series with the load (LEDs).
27	CS-	Inverting Current-Sense Amplifier Input. Connect CS- to the negative side of an external sense resistor, R_{CS}, connected in series with the load (LEDs).
28	CLMP	Internal CLAMP Regulator Bypass. CLAMP supplies an 8V (typ) output when $V_{HI} \geq 9V$. If V_{HI} is lower than 9V, V_{CLMP} is one diode drop below V_{HI}. The CLAMP regulator powers the current-sense amplifier and provides the high reference for the dimming driver. V_{CLMP} must be at least 2.5V higher than V_{LO} to enable the current-sense amplifier and dimming MOSFET driver. Bypass CLMP to LO with a 0.1µF ceramic capacitor.
29	HI	High-Voltage Input. HI is referred to LO. HI supplies power to the current-sense amplifier and dimming MOSFET gate driver through the CLMP regulator.
30	REG2	Internal Regulator Output. REG2 is an internal voltage regulator that generates EEPROM-programmable (5V to 15V) output and supplies power to internal circuitry. Connect REG2 to DRI to power the switching MOSFET driver during normal operation. Bypass REG2 to AGND with a 10µF ceramic capacitor.
31	V_{CC}	Supply Voltage Input
32	$\overline{FAULT}$	$\overline{FAULT}$ Input/Output. $\overline{FAULT}$ is a bidirectional high-voltage logic input/output. $\overline{FAULT}$ multiplexes a 1-Wire programming interface with a fault indicator. $\overline{FAULT}$ is internally pulled up to 5V through a 10kΩ resistor and a 1.8mA (max) current pulldown to ground.
EP	EP	Exposed Pad. Connect EP to AGND. EP also functions as a heatsink to maximize thermal dissipation. Do not use as the main ground connection.

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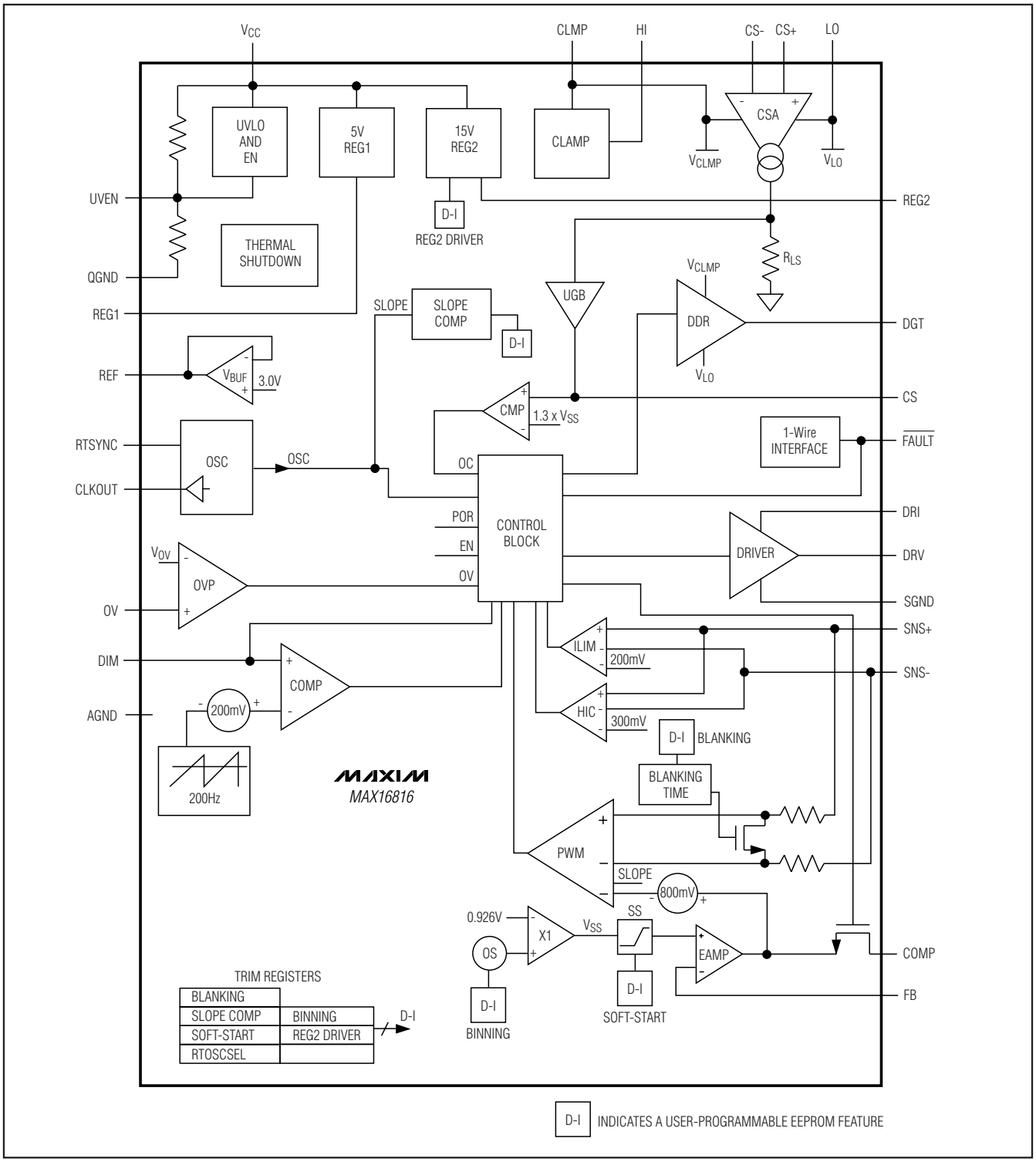
Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

Functional Diagram



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Detailed Description

The MAX16816 is a current-mode PWM LED driver for use in driving HB LEDs. An output current accuracy of 5% is achievable using two current regulation loops: one current regulation loop controls the external switching MOSFET peak current through a sense resistor, R_{SENSE}, from SNS+ to SNS- while the other current regulation loop controls the average LED string current through the sense resistor, R_{CS}, in series with the LEDs. The wide operating supply range of 5.9V/5.4V (ON/OFF) to 76V makes the MAX16816 ideal in automotive applications.

The MAX16816 provides LED binning through one programmable on-chip nonvolatile EEPROM. The LED current can be scaled up to a factor of 1.6. This feature is used to offset factory LED luminance variations and allows the system to achieve overall luminance accuracy.

A programmable undervoltage lockout (UVEN) ensures predictable operation during brownout conditions. The UVEN input circuitry monitors the supply voltage, V_{CC}, and turns the driver off when V_{CC} drops below the UVLO threshold. Connect UVEN to V_{CC} to use the 5.7V (typ) default UVLO threshold. The MAX16816 includes a cycle-by-cycle current limit that turns off the gate drive to the external switching MOSFET (Q_S) during an overcurrent condition and a programmable oscillator that simplifies and optimizes the design of external magnetics.

The MAX16816 is capable of synchronizing to an external clock or operating in a stand-alone mode. A single resistor, R_T, can be used to adjust the switching frequency from 125kHz to 500kHz for stand-alone operation. To synchronize the device with an external clock, apply a clock signal directly to the RTSYNC input. A buffered clock output, CLKOUT, is available to configure the MAX16816 for multichannel applications. The external RT oscillator can be disabled by setting EEPROM register RTOF to '1'.

The MAX16816 provides wide contrast pulsed dimming (up to 1000:1) utilizing a separate dimming input. Apply either a DC level voltage or low-frequency PWM signal to the dimming input. DC level input results in a 200Hz fixed dimming frequency.

The MAX16816 provides configurable on-chip nonvolatile EEPROM features including a programmable soft-start, load current, external MOSFET gate-driver supply voltage, blanking time, and slope compensation.

Protection features include peak current limiting, HICCUP mode current limiting, output overvoltage protection, short-circuit protection, and thermal shutdown. The HICCUP current-limit circuitry reduces the power delivered to the load during severe fault conditions. A nonlatching overvoltage protection limits the voltage on the external switching MOSFET (Q_S) under open-circuit conditions in the LED string. During continuous operation at high input voltages, the power dissipation of the MAX16816 could exceed the maximum rating and the internal thermal shutdown circuitry safely turns off the MAX16816 when the device junction temperature exceeds +165°C. When the junction temperature drops below the hysteresis temperature, the MAX16816 automatically reinitiates startup.

Undervoltage Lockout/Enable (UVEN)

The MAX16816 features a dual-purpose adjustable undervoltage lockout input and enable function (UVEN). Connect UVEN to V_{CC} through a resistive voltage-divider to set the undervoltage lockout (UVLO) threshold. The device is enabled when the voltage at UVEN exceeds the 1.244V (typ) threshold. Drive UVEN to ground to disable the output.

Setting the UVLO Threshold

Connect UVEN directly to V_{CC} to select the default 5.7V (typ) UVLO threshold. Connect UVEN to V_{CC} through a resistive voltage-divider to select a UVLO threshold (Figure 1). Select the desired UVLO threshold voltage, V_{UVLO}, and calculate resistor values using the following equation:

$$R_{UV1} = R_{UV2} \times \left(\frac{V_{UVEN}}{V_{UVLO} - V_{UVEN}} \right)$$

where $R_{UV1} + R_{UV2} \le 270k\Omega$. V_{UVEN} is the 1.244V (typ) UVEN threshold voltage.

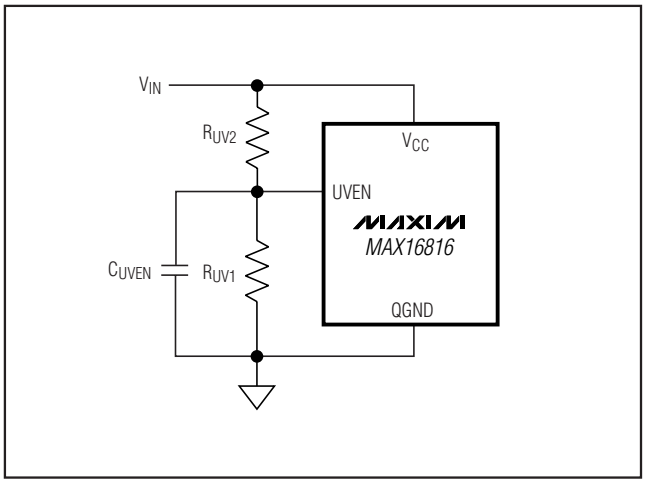

Figure 1. Setting the UVLO Threshold

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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

The capacitor C_{UVEN} is required to prevent chattering at the UVLO threshold due to line impedance drops during power-up and dimming. If the undervoltage setting is very close to the required minimum operating voltage, there can be large jumps in the voltage at V_{CC} during dimming, which may cause the MAX16816 to turn on and off when the dimming signal transitions from low to high. The capacitor C_{UVEN} should be large enough to limit the ripple on UVEN to less than the 100mV (min) UVEN hysteresis so that the device does not turn off under these circumstances.

Soft-Start

The MAX16816 features a digitally programmable soft-start delay that allows the load current to ramp up in a controlled manner, minimizing output overshoot. Soft-start begins once the device is enabled and V_{CC} exceeds the UVLO threshold. Soft-start circuitry slowly increases the internal soft-start voltage, V_{SS}, resulting in a controlled rise of the load current. Signals applied to DIM are ignored until the soft-start duration is complete and a successive delay of 200µs has elapsed. Use the Digital Soft-Start Duration register in the EEPROM to select a soft-start duration from 0 (no delay) to 4.096ms. See the *EEPROM and Programming* section for more information on using the Digital Soft-Start Duration register.

Regulators (REG1, REG2, CLAMP)

The MAX16816 includes a fixed 5V voltage regulator, REG1; an EEPROM-adjustable regulator, REG2; and an internal 8V regulator, CLAMP. REG1 and REG2 power up when V_{CC} exceeds the UVLO threshold. REG1 supplies power to internal circuitry and remains on during PWM dimming. REG1 is capable of driving external loads up to 2mA.

Use the REG2 Control Register in the EEPROM to select an output voltage from 5V to 15V for REG2. Connect REG2 to DRI to generate the supply voltage for the primary switching MOSFET driver, DRV. REG2 is capable of delivering up to 20mA of current. See the *EEPROM and Programming* section for more information on configuring the REG2 output voltage.

CLAMP is powered by HI and supplies power to the current-sense amplifier (CSA). CSA is enabled when V_{CLMP} goes 2.5V above V_{LO} and is disabled when (V_{CLMP} - V_{LO}) falls below 2.28V. The CLAMP regulator also provides power to the dimming MOSFET control circuitry. CLMP is the output of the CLAMP regulator. Do not use CLMP to power external circuitry. Bypass CLMP to LO with a 0.1µF ceramic capacitor. A larger capacitor will result in overshoot of the load current.

Reference Voltage Output (REF)

The MAX16816 includes a 5% accurate, 3V (typ) buffered reference output, REF. REF is a push-pull output capable of sourcing/sinking up to 200µA of current and can drive a maximum load capacitance of 100pF. Connect REF to DIM through a resistive voltage-divider to supply an analog signal for dimming. See the *Dimming Input (DIM)* section for more information.

Dimming MOSFET Driver (DDR)

The MAX16816 requires an external n-channel MOSFET for PWM dimming. Connect the MOSFET to the output of the DDR dimming driver, DGT, for normal operation. V_{DGT} swings between V_{LO} and V_{CLMP}. The DDR dimming driver is capable of sinking or sourcing up to 20mA of current. The average current required to drive the dimming MOSFET (I_{DRIVE_DIM}) depends on the MOSFET's total gate charge (Q_{G_DIM}) and the dimming frequency of the converter, f_{DIM}. Use the following equation to calculate the supply current for the n-channel dimming FET driver.

$$I_{DRIVE\_DIM} = Q_{G\_DIM} \times f_{DIM}$$

n-Channel MOSFET Switch Driver (DRV)

The MAX16816 drives an external n-channel MOSFET for switching. Use an external supply or connect REG2 to DRI to power the MOSFET driver. The driver output, V_{DRV}, swings between ground and V_{DRI}. Ensure that V_{DRI} remains below the absolute maximum V_{GS} rating of the external MOSFET. DRV is capable of sinking 2A or sourcing 1.4A of peak current, allowing the MAX16816 to switch MOSFETs in high-power applications. The average current sourced to drive the external MOSFET depends on the total gate charge (Q_G) and operating frequency of the converter, f_{SW}. The power dissipation in the MAX16816 is a function of the average output drive current (I_{DRIVE}). Use the following equations to calculate the power dissipation in the gate-driver section of the MAX16816 due to I_{DRIVE}:

$$I_{DRIVE} = Q_G \times f_{SW}$$

$$P_D = I_{DRIVE} \times V_{DRI}$$

where V_{DRI} is the supply voltage to the gate driver.

Dimming Input (DIM)

The dimming input, DIM, functions with either analog or PWM control signals. Once the internal pulse detector detects three successive edges of a PWM signal with a frequency between 80Hz and 2kHz, the MAX16816 synchronizes to the external signal and pulse-width modulates the LED current at the external DIM input frequency with the same duty cycle as the DIM input. If

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an analog control signal is applied to DIM, the MAX16816 compares the DC input to an internally generated 200Hz ramp to pulse-width modulate the LED current (f_{DIM} = 200Hz). The output current duty cycle is linearly adjustable from 0 to 100% (0.2V < V_{DIM} < 2.8V).

Use the following formula to calculate voltage, V_{DIM}, necessary for a given output current duty cycle, D:

$$V_{DIM} = (D \times 2.6) + 0.2V$$

where V_{DIM} is the voltage applied to DIM in volts.

Connect DIM to REF through a resistive voltage-divider to apply a DC DIM control signal (Figure 2). Use the required dimming input voltage, V_{DIM}, calculated above and select appropriate resistor values using the following equation:

$$R_4 = R_3 \times V_{DIM} / (V_{REF} - V_{DIM})$$

where V_{REF} is the 3V reference output voltage and $15k\Omega \le R_3 + R_4 \le 150k\Omega$.

A minimum 20µs pulse width is necessary for proper operation during dimming.

Oscillator, Clock, and Synchronization

The MAX16816 is capable of stand-alone operation, of synchronizing to an external clock, and of driving external devices in SYNC mode. For stand-alone operation, set the EEPROM Oscillator Enable/Disable (RTOF) bit to '1' to use the fixed internal 125kHz oscillator or set RTOF to '0' and program the switching frequency by connecting a single external resistor, R_T, between RTSYNC and ground. Select a switching frequency, f_{SW}, between 125kHz and 500kHz and calculate R_T using the following formula:

$$R_T = \frac{500kHz}{f_{SW}} \times 25k\Omega$$

where the switching frequency is in kHz and R_T is in kΩ.

To synchronize the MAX16816 with an external clock signal ranging from 125kHz to 500kHz, set the RTOF bit to '0' and connect the clock signal to the RTSYNC input. The MAX16816 synchronizes to the clock signal after the detection of 5 successive clock edges at RTSYNC.

A buffered clock output, CLKOUT, can drive the RTSYNC input of an external PWM controller for multichannel applications. CLKOUT can drive capacitive loads up to 500pF.

If the PWM switching frequency is set to 125kHz, the RTSYNC oscillator can be temporarily disabled by setting the EEPROM RTOF bit to '1'. In this case, the internal 125kHz frequency-fixed oscillator drives the PWM. See the *EEPROM and Programming* section for more information on setting the Oscillator Enable/Disable bit in the EEPROM.

Multichannel Configuration

The MAX16816 is capable of multichannel operation and is configurable as a master or slave in a Master-Slave configuration, or in a Peer-to-Peer configuration. Connect CLKOUT to the SYNC input of an external device to use the MAX16816 as a master clock signal. Connect an external clock signal to RTSYNC to configure the MAX16816 as a slave. To setup two MAX16816 devices in a daisy-chain configuration, drive the RTSYNC input of one MAX16816 with the CLKOUT buffer of another (Figure 3).

ILIM and HICCUP Comparator

R_{SENSE} sets the peak current through the inductor for switching. The differential voltage across R_{SENSE} is compared to the 200mV voltage-trip limit of the current-limit comparator, ILIM. Set the current limit 20% higher than the peak switch current at the rated output power and minimum voltage. Use the following equation to calculate R_{SENSE}:

$$R_{SENSE} = V_{SENSE} / (1.2 \times I_{PEAK})$$

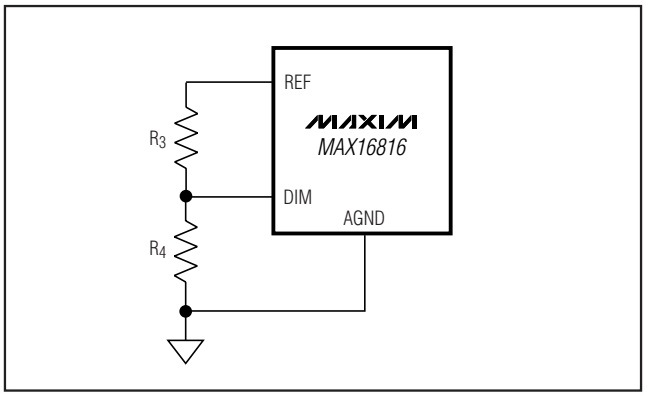

Figure 2. Creating DIM Input Signal from REF

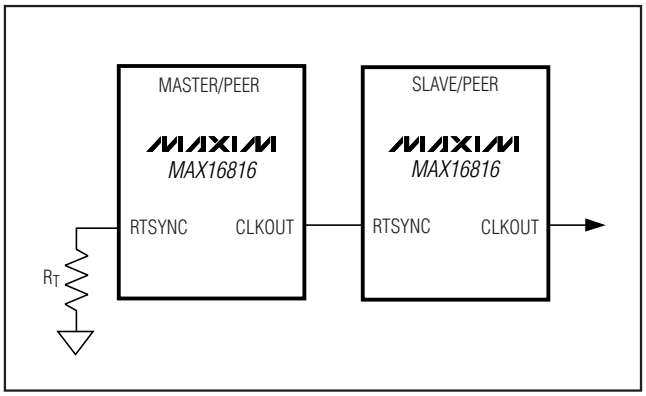

Figure 3. Master-Slave/Peer-Peer Clock Configuration

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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

where V_{SENSE} is the 200mV maximum differential voltage between SNS+ and SNS- and I_{PEAK} is the peak inductor current at full load and minimum input voltage.

When the voltage drop across R_{SENSE} exceeds the ILIM threshold, the MOSFET driver (DRV) terminates the on-cycle and turns the switch off, reducing the current through the inductor. The FET is turned back on at the beginning of the next switching cycle.

When the voltage across R_{SENSE} exceeds the 300mV (typ) HICCUP threshold, the HIC comparator terminates the on-cycle of the device, turning the switching MOSFET off. Following a startup delay of 8ms (typ), the MAX16816 reinitiates soft-start. The device will continue to operate in HICCUP mode until the overcurrent condition is removed.

A programmable built-in leading-edge blanking circuit of the current-sense signal prevents these comparators from prematurely terminating the on-cycle of the external switching MOSFET (Q_S). Select a blanking time from 75ns to 150ns by configuring the Blanking Time register in the EEPROM. In some cases, the maximum blanking time may not be adequate and an additional RC filter may be required to prevent spurious turn-off.

Load Current Sense

The load sense resistor, R_{CS}, monitors the current through the LEDs. The internal floating current-sense amplifier, CSA, measures the differential voltage across R_{CS}, and generates a voltage proportional to the load current through R_{CS} at CS. This voltage on CS is referred to AGND. The closed-loop regulates the load current to a value, I_{LED}, given by the following equation:

$$I_{LED} = V_{SS} / R_{CS}$$

where V_{SS} is the binning adjustment voltage. Set the value of V_{SS} in the Binning Adjustment register in the EEPROM between 100mV and 166mV. See the *EEPROM and Programming* section for more information on adjusting the binning voltage.

Slope Compensation

The amount of slope compensation required is largely dependent on the down-slope of the inductor current when the switching MOSFET, Q_S, is off. The inductor down-slope depends on the input-to-output voltage differential of the converter, the inductor value, and the switching frequency. For stability, the compensation slope should be equal to or greater than half of the inductor current down-slope multiplied by the current-sense resistance (R_{SENSE}).

See the *EEPROM and Programming* section for more information on the ESLP register.

Internal Voltage-Error Amplifier (EAMP)

The MAX16816 includes a built-in voltage amplifier, with three-state output, which can be used to close the feedback loop. The buffered output current-sense signal appears at CS, which is connected to the inverting input, FB, of the error amplifier through resistor R_1. The noninverting input is connected to an internally trimmed current reference.

The output of the error amplifier is controlled by the signal applied to DIM. When DIM is high, the output of the amplifier is connected to COMP. The amplifier output is open when DIM is low. This enables the integrating capacitor to hold the charge when the DIM signal has turned off the gate drive. When DIM is high again, the voltage on the compensation capacitors, C_1 and C_2, forces the converter into steady state almost instantaneously.

PWM Dimming

PWM dimming is achieved by driving DIM with either a PWM signal or a DC signal. The PWM signal is connected internally to the error amplifier, the dimming MOSFET gate driver, and the switching MOSFET gate driver. When the DIM signal is high, the dimming MOSFET and the switching MOSFET drivers are enabled and the output of the voltage-error amplifier is connected to the external compensation network. Also, the buffered current-sense signal is connected to CS. Preventing discharge of the compensation capacitor when the DIM signal is low allows the control loop to return the LED current to its original value almost instantaneously.

When the DIM signal goes low, the output of the error amplifier is disconnected from the compensation network and the compensation capacitors, C_1 and C_2, voltage is preserved. Choose low-leakage capacitors for C_1 and C_2. The drivers for the external dimming and switching MOSFETs are disabled, and the converter stops switching. The inductor energy is now transferred to the output capacitors.

When the DIM signal goes high and the gate drivers are enabled, the additional voltage on the output capacitor may cause a current spike on the LED string. A larger output capacitor will result in a smaller current spike. If the overcurrent spike exceeds 30% of the programmed LED current, the dimming is turned off and the MAX16816 reinitiates soft-start.

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FAULT 1-Wire Interface

The MAX16816 features a FAULT output multiplexed with a 1-Wire programming interface. Once the voltage at UVEN exceeds the UVLO threshold, the device is enabled and FAULT will pulse low once, indicating the beginning of the programming window. Two programming mode entry codes must be entered within 8ms after the pulse to enter programming mode (see Table 1). The MAX16816 will register the second entry code only after the first code has been received. Once the MAX16816 successfully enters programming mode, the data and clock for the 1-Wire interface are supplied through FAULT.

Once the programming window has passed, the EEPROM is no longer accessible without cycling power to the device. Under these conditions, FAULT will go low only when a fault (overvoltage, overcurrent, or HICCUP mode) occurs or when the supply voltage drops below the UVLO threshold.

EEPROM and Programming

Nonvolatile EEPROM is available to configure the MAX16816 through a 1-Wire serial interface. Registers are located in a linear address space as shown in Table 2. All other EEPROM locations are reserved. Configure the six control registers to adjust parameters including the REG2 voltage, soft-start durations, blanking time, LED load current (binning), slope compensation, and to enable/disable the RTOF oscillator. See the *1-Wire Interface* section for more information about 1-Wire programming.

Table 1. Programming Mode Entry Codes

PROGRAMMING MODE ENTRY CODE	D7	D6	D5	D4	D3	D2	D1	D0	HEX CODE
PASS_CODE_1	0	0	1	0	1	0	0	1	29h
PASS_CODE_2	0	0	0	0	1	0	0	1	09h

Table 2. EEPROM Memory Map

REGISTER	EEPROM ADDRESS RANGE	NO. OF BITS	TYPE	DESCRIPTION
Binning Adjustment (BIN)	24h–27h	4	R/W	Adjusts the LED current.
REG2 Control (DRPS)	28h–2Bh	4	R/W	Sets the output voltage for REG2. Connect REG2 to DRI to supply the high-side voltage for the gate driver, DRV.
Blanking Time Adjustment (BLNK)	32h–33h	2	R/W	Adjusts the blanking time for debouncing.
Digital Soft-Start Duration (SS)	34h–36h	2	R/W	Adjusts the soft-start duration to allow the load current to ramp up in a controlled manner, minimizing output overshoot.
Internal Oscillator Enable/Disable (RTOF)	37h	1	R/W	Enables/disables the internal oscillator for stand-alone operation or to synchronize with an external clock.
Slope Compensation (ESLP)	38h–3Bh	4	R/W	Adjusts the slope compensation for stability.

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Binning Adjustment Register (BIN)

The MAX16816 uses a feedback loop to control the load current. The differential voltage across the current-sense resistor, R_{CS}, is compared with an internal adjustable reference to regulate the LED current. The voltage across the sense resistor is measured differentially to achieve high immunity to common-mode noise. The MAX16816 includes a factory-set regulation voltage of 133mV ±3% across R_{CS}. Adjust the differential regulation voltage by programming the binning adjustment register (see Table 3). The reference voltage level may not necessarily be equal to the regulation voltage. There are offsets involved that are trimmed at the factory. Read the default register code and step up the code by one to increase the regulation voltage by 6.66mV. Step down the code by one to reduce the regulation voltage by 6.66mV.

REG2 Control Register (DRPS)

REG2 is EEPROM configurable to supply a voltage ranging from 5V to 15V and is capable of sourcing up to 20mA. Connect REG2 to the primary switching MOSFET gate-driver supply input, DRI, for normal operation. Adjust REG2 by programming the REG2 Control Register. See Table 4.

Blanking Time Adjustment Register (BLNK)

The MAX16816 features a programmable blanking time to mask out the current-sense signal for a short duration to avoid the ILIM and HICCUP comparators from prematurely terminating the on-cycle of the switching MOSFET. This blanking time allows for higher input current during startup without triggering a fault condition. The blanking time is adjustable in the range of 150ns to 75ns by configuring the EEPROM. See Table 5.

Table 3. Binning Adjustment Register

REFERENCE VOLTAGE LEVEL (mV)	EEPROM ADDRESS			
	27h	26h	25h	24h
100.00	0	0	0	0
106.67	0	0	0	1
113.33	0	0	1	0
120.00	0	0	1	1
126.67	0	1	0	0
133.33	0	1	0	1
140.00	0	1	1	0
146.67	0	1	1	1
153.33	1	0	0	0
160.00	1	0	0	1
166.67	1	0	1	0
173.33*	1	0	1	1
180.00*	1	1	0	0
186.67*	1	1	0	1
193.33*	1	1	1	0
200.00*	1	1	1	1

**Not recommended*

Table 4. REG2 Control Register

REG2 OUTPUT VOLTAGE (V)	EEPROM ADDRESS			
	2Bh	2Ah	29h	28h
5.000	0	0	0	0
5.667	0	0	0	1
6.333	0	0	1	0
7.000*	0	0	1	1
7.667	0	1	0	0
8.333	0	1	0	1
9.000	0	1	1	0
9.667	0	1	1	1
10.333	1	0	0	0
11.000	1	0	0	1
11.667	1	0	1	0
12.333	1	0	1	1
13.000	1	1	0	0
13.667	1	1	0	1
14.333	1	1	1	0
15.000	1	1	1	1

**Factory default*

Table 5. Blanking Time

BLANKING TIME (ns)	EEPROM ADDRESS	
	33h	32h
150*	0	0
125	0	1
100	1	0
75	1	1

**Factory default*

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Digital Soft-Start Duration Register (SS)

The MAX16816 programmable soft-start feature allows the load current to ramp up in a controlled manner, eliminating output overshoot during startup. Soft-start begins once the device is enabled and V_{CC} has exceeded the 5.5V (min) rising threshold voltage. Adjust the soft-start duration by configuring the EEPROM. Enter '111' to disable the soft-start feature. See Table 6.

Oscillator Enable/Disable Register (RTOF)

The MAX16816 features a programmable accurate RTSYNC oscillator and resistor synchronized to an external clock. Set the EEPROM bit RTOF to '1' to disable the external sync mode, and the RTSYNC oscillator, and to use the fixed internal frequency of 125kHz as the switching frequency. Set RTOF to '0' to synchronize with an external oscillator or to program the external oscillator frequency with an external resistor, R_T. See Table 7.

Slope Compensation Register (ESLP)

The MAX16816 uses an internally generated ramp to stabilize the current loop when operating at duty cycles above 50%. Set the compensating slope by adjusting the peak ramp voltage through the on-chip EEPROM. See Tables 8 and 9.

Table 6. Digital Soft-Start Duration

DURATION (µs)	EEPROM ADDRESS		
	36h	35h	34h
4096*	0	0	0
2048	0	0	1
1860	0	1	0
1024	0	1	1
768	1	0	0
512	1	0	1
256	1	1	0
No SS	1	1	1

**Factory default*

Table 7. Oscillator Enable/Disable

RT OSCILLATOR	EEPROM ADDRESS
	37h
RT Oscillator Off	1
RT Oscillator On*	0

**Factory default*

Table 8. Slope Compensation with Clock Generated by RT Oscillator

SLOPE COMPENSATION (mV/clock cycle)	EEPROM ADDRESS			
	3Bh	3Ah	39h	38h
0	0	0	0	0
20	0	0	0	1
40	0	0	1	0
60	0	0	1	1
80	0	1	0	0
100	0	1	0	1
120*	0	1	1	0
140	0	1	1	1
160	1	0	0	0
180	1	0	0	1
200	1	0	1	0
220	1	0	1	1
240	1	1	0	0
260	1	1	0	1
280	1	1	1	0
300	1	1	1	1

**Factory default*

Table 9. Slope Compensation with External Clock Applied to RTSYNC or RT Oscillator Off

SLOPE COMPENSATION (mV/µs)	EEPROM ADDRESS			
	3Bh	3Ah	39h	38h
0	0	0	0	0
2	0	0	0	1
4	0	0	1	0
6	0	0	1	1
8	0	1	0	0
10	0	1	0	1
12*	0	1	1	0
14	0	1	1	1
16	1	0	0	0
18	1	0	0	1
20	1	0	1	0
22	1	0	1	1
24	1	1	0	0
26	1	1	0	1
28	1	1	1	0
30	1	1	1	1

**Factory default*

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Fault Protection

The MAX16816 features built-in overvoltage protection, overcurrent protection, HICCUP mode current-limit protection, and thermal shutdown. Overvoltage protection is achieved by connecting OV to HI through a resistive voltage-divider. HICCUP mode limits the power dissipation in the external MOSFETs during severe fault conditions. Internal thermal shutdown protection safely turns off the converter when the IC junction temperature exceeds +165°C.

Overvoltage Protection

The overvoltage protection (OVP) comparator compares the voltage at OV with a 1.235V (typ) internal reference. When the voltage at OV exceeds the internal reference, the OVP comparator terminates PWM switching and no further energy is transferred to the load. The MAX16816 reinitiates soft-start once the overvoltage condition is removed. Connect OV to HI through a resistive voltage-divider to set the overvoltage threshold at the output.

Setting the Overvoltage Threshold

Connect OV to HI or to the high-side of the LEDs through a resistive voltage-divider to set the overvoltage threshold at the output (Figure 4). The overvoltage protection (OVP) comparator compares the voltage at OV with a 1.235V (typ) internal reference. Use the following equation to calculate resistor values:

$$R_{OV1} = R_{OV2} \times \left(\frac{V_{OV\_LIM} - V_{OV}}{V_{OV}} \right)$$

where V_{OV} is the 1.235V OV threshold. Choose R_{OV1} and R_{OV2} to be reasonably high value resistors to prevent discharge of filter capacitors. This will prevent unnecessary undervoltage and overvoltage conditions during dimming.

Load-Dump Protection

The MAX16816 features load-dump protection up to 76V. LED drivers using the MAX16816 can sustain single fault load dump events. Repeated load dump events within very short time intervals can cause damage to the dimming MOSFET due to excess power dissipation.

Thermal Shutdown

The MAX16816 contains an internal temperature sensor that turns off all outputs when the die temperature exceeds +165°C. Outputs are enabled again when the die temperature drops below +145°C.

Applications Information

Inductor Selection

The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the peak-to-peak inductor current (ΔI_L). Higher ΔI_L allows for a lower inductor value while a lower ΔI_L requires a higher inductor value. A lower inductor value minimizes size and cost, improves large-signal transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output ripple voltage for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current, ΔI_L. However, resistive losses due to extra turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. A good compromise is to choose ΔI_L equal to 30% of the full load current. The inductor saturating current is also important to avoid runaway current during the output overload and continuous short circuit. Select the I_{SAT} to be higher than the maximum peak current limit.

Buck configuration: In a buck configuration the average inductor current does not vary with the input. The worst-case peak current occurs at high input voltage. In this case the inductance, L, for continuous conduction mode is given by:

$$L = \frac{V_{OUT} \times (V_{INMAX} - V_{OUT})}{V_{INMAX} \times f_{SW} \times \Delta I_L}$$

where V_{INMAX} is the maximum input voltage, f_{SW} is the switching frequency, and V_{OUT} is the output voltage.

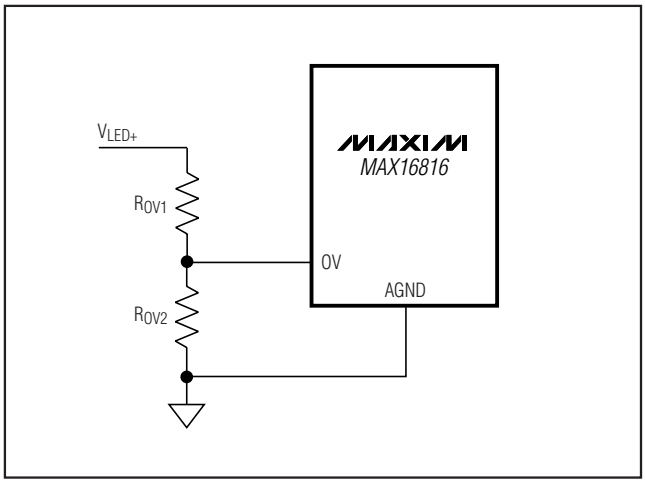

Figure 4. Setting the Overvoltage Threshold

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Boost configuration: In the boost converter, the average inductor current varies with line and the maximum average current occurs at low line. For the boost converter, the average inductor current is equal to the input current. In this case the inductance, L, is calculated as:

$$L = \frac{V_{INMIN} \times (V_{OUT} - V_{INMIN})}{V_{OUT} \times f_{SW} \times \Delta I_L}$$

where V_{INMIN} is the minimum input voltage, V_{OUT} is the output voltage, and f_{SW} is the switching frequency.

Buck-boost configuration: In a buck-boost converter the average inductor current is equal to the sum of the input current and the load current. In this case the inductance, L, is:

$$L = \frac{V_{OUT} \times V_{INMIN}}{(V_{OUT} + V_{INMIN}) \times f_{SW} \times \Delta I_L}$$

where V_{INMIN} is the minimum input voltage, V_{OUT} is the output voltage, and f_{SW} is the switching frequency.

Output Capacitor

The function of the output capacitor is to reduce the output ripple to acceptable levels. The ESR, ESL, and the bulk capacitance of the output capacitor contribute to the output ripple. In most of the applications, the output ESR and ESL effects can be dramatically reduced by using low-ESR ceramic capacitors. To reduce the ESL effects, connect multiple ceramic capacitors in parallel to achieve the required bulk capacitance.

In a buck configuration, the output capacitance, C_F, is calculated using the following equation:

$$C_F \geq \frac{(V_{INMAX} - V_{OUT}) \times V_{OUT}}{\Delta V_R \times 2 \times L \times V_{INMAX} \times f_{SW}^2}$$

where ΔV_R is the maximum allowable output ripple.

In a boost configuration, the output capacitance, C_F, is calculated as:

$$C_F \geq \frac{(V_{OUT} - V_{INMIN}) \times 2 \times I_{OUT}}{\Delta V_R \times V_{OUT} \times f_{SW}}$$

where I_{OUT} is the output current.

In a buck-boost configuration, the output capacitance, C_F, is calculated as:

$$C_F \geq \frac{2 \times V_{OUT} \times I_{OUT}}{\Delta V_R \times (V_{OUT} + V_{INMIN}) \times f_{SW}}$$

where V_{OUT} is the voltage across the load and I_{OUT} is the output current.

Input Capacitor

An input capacitor connected between V_{CC} and ground must be used when configuring the MAX16816 as a buck converter. Use a low-ESR input capacitor that can handle the maximum input RMS ripple current. Calculate the maximum allowable RMS ripple using the following equation:

$$I_{IN(RMS)} = \frac{I_{OUT} \times \sqrt{V_{OUT} \times (V_{INMIN} - V_{OUT})}}{V_{INMIN}}$$

In most of the cases, an additional electrolytic capacitor should be added to prevent input oscillations due to line impedances.

When using the MAX16816 in a boost or buck-boost configuration, the input RMS current is low and the input capacitance can be small (see the *Typical Operating Circuits*).

Operating the MAX16816 Without the Dimming Switch

The MAX16816 can also be used in the absence of the dimming MOSFET. In this case, the PWM dimming performance is compromised but in applications that do not require dimming the MAX16816 can still be used. A short circuit across the load will cause the MAX16816 to disable the gate drivers and they will remain off until the input power is recycled.

Switching Power MOSFET Losses

When selecting MOSFETs for switching, consider the total gate charge, power dissipation, the maximum drain-to-source voltage, and package thermal impedance. The product of the MOSFET gate charge and $R_{DS(ON)}$ is a figure of merit, with a lower number signifying better performance. Select MOSFETs optimized for high-frequency switching applications.

Layout Recommendations

Typically, there are two sources of noise emission in a switching power supply: high di/dt loops and high dv/dt surfaces. For example, traces that carry the drain current often form high di/dt loops. Similarly, the heatsink of the MOSFET connected to the device drain presents a high dv/dt source; therefore, minimize the surface area of the heatsink as much as possible. Keep all PCB traces carrying switching currents as short as possible to minimize current loops. Use ground planes for best results.

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Careful PCB layout is critical to achieve low switching losses and clean, stable operation. Use a multilayer board whenever possible for better noise performance and power dissipation. Follow these guidelines for good PCB layout:

- Use a large copper plane under the MAX16816 package. Ensure that all heat-dissipating components have adequate cooling. Connect the exposed pad of the device to the ground plane.
- Isolate the power components and high current paths from sensitive analog circuitry.
- Keep the high-current paths short, especially at the ground terminals. This practice is essential for stable, jitter-free operation. Keep switching loops short.
- Connect AGND, SGND, and QGND to a ground plane. Ensure a low-impedance connection between all ground points.
- Keep the power traces and load connections short. This practice is essential for high efficiency. Use thick copper PCBs (2oz vs. 1oz) to enhance full-load efficiency.
- Ensure that the feedback connection to FB is short and direct.
- Route high-speed switching nodes away from the sensitive analog areas.
- To prevent discharge of the compensation capacitors, C_1 and C_2, during the off-time of the dimming cycle, ensure that the PCB area close to these components has extremely low leakage. Discharge of these capacitors due to leakage may result in degraded dimming performance.

1-Wire Interface

EEPROM implementation uses a 1-Wire communication method. A 1-Wire net-based system consists of three main elements: a bus master with controlling software, the wiring and associated connectors, and 1-Wire devices. Data on the 1-Wire net is transferred with respect to time slots. For example, the master pulls the bus low and holds it for 15µs or less to write a logic '1', and holds the bus low for at least 60µs to write a logic '0'. During EEPROM programming the MAX16816 is a 1-Wire slave device only. Data and clock signals are supplied through $\overline{FAULT}$.

MAX16816 1-Wire Function Commands

Table 10 shows the list of 1-Wire function commands for the MAX16816. Use these commands to start the programming mode, write to the on-chip EEPROM, and read EEPROM through the 1-Wire interface.

PASS_CODE_ONE: The PASS_CODE_ONE sequence is the first code that the MAX16816 must receive from the master. PASS_CODE_ONE must be received within the initial 8ms programming window after startup.

PASS_CODE_TWO: The PASS_CODE_TWO sequence is the second code that the MAX16816 must receive during the 8ms programming window. The MAX16816 will start searching for PASS_CODE_TWO only after PASS_CODE_ONE has been received.

EXT_EEM_MODE: The EXT_EEM_MODE command clears the PASS_CODE_ONE and PASS_CODE_TWO verification register. Use this command to exit programming mode.

SET_WRITE_EE: The SET_WRITE_EE command is the write all command for the MAX16816. When the device detects the SET_WRITE_EE command the write

Table 10. MAX16816 1-Wire Function Commands

COMMAND	DATA BIT CODE								HEX CODE
	D7	D6	D5	D4	D3	D2	D1	D0	
PASS_CODE_ONE	0	0	1	0	1	0	0	1	29h
PASS_CODE_TWO	0	0	0	0	1	0	0	1	09h
EXT_EEM_MODE	0	0	0	0	0	0	0	1	01h
SET_WRITE_EE	0	0	0	0	0	1	0	0	04h
SET_WRITE_SCH	ADD	ADD	ADD	ADD	DATA	DATA	DATA	DATA	—
SET_READ_SCH	0	0	0	0	0	1	1	0	06h

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sequence begins. All EEPROM bits are copied to the EEPROM from the scratchpad with a single SET_WRITE_EE command. This command also sets an internal BUSY flag to mask all other incoming signals.

SET_WRITE_SCH: The SET_WRITE_SCH command transfers data to the scratchpad. The 4 MSBs contain the register address and the 4 LSBs contain the data to be written. The internal BUSY flag is not set by this command. Table 11 shows the MAX16816 EEPROM memory organization. Use the SET_WRITE_EE command to transfer data from the scratchpad to the EEPROM.

SET_READ_SCH: The SET_READ_SCH command is the command to read data in the scratch pad buffer. Once the MAX16816 receives the SET_READ_SCH command, data on the scratchpad register is shifted out. After 60 clock cycles, the MAX16816 completes the SET_READ_SCH sequence. The BUSY signal is not set by this command.

Programming

To program the MAX16816 on-chip EEPROM with a pulldown device, directly connect $\overline{FAULT}$ to the DATA IN input of a microcontroller (µC). Also, connect $\overline{FAULT}$ to the DATA OUT output of a µC using an external switch (Figure 5). Connect the EN of the µC directly to UVEN to control the internal timer of the MAX16816 for programming purposes. Ensure that V_{CC} is greater than the UVLO threshold because both UVEN and $\overline{FAULT}$ are pulled up to 5V. See the *Electrical Characteristic* tables for details.

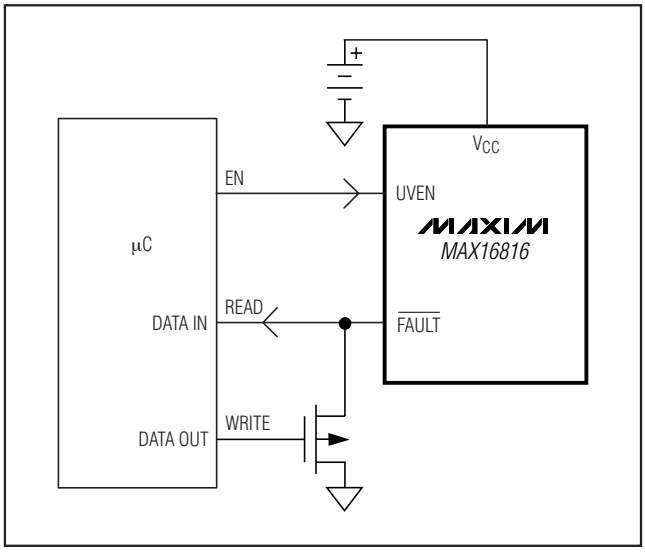

Figure 5. Programming Through a $\overline{FAULT}$ Pin

Table 11. MAX16816 Memory Map (Scratchpad)

SCRATCHPAD ADDRESS	EEPROM ADDRESS	REGISTER
1h	Reserved	Reserved
2h	Reserved	Reserved
3h	Reserved	Reserved
4h	Reserved	Reserved
5h	Reserved	Reserved
6h–9h	14h–23h	Reserved
Ah	24h–27h	Binning Adjustment Register
Bh	28h–2Bh	REG2 Control Register
Ch	2Ch–2Fh	Reserved
Dh	30h–33h	Blanking Time Adjustment Register
Eh	34h–37h	Digital Soft-Start Duration Register, Internal Oscillator Enable Bit
Fh	38h–3Bh	Slope Compensation Register

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Programming Sequences

The µC (master) starts the communication with the MAX16816 by pulling UVEN high. The MAX16816 then does the handshaking with the µC by pulling $\overline{FAULT}$ low. Once the µC receives the handshaking signal, it begins the initialization sequences to reset the 1-Wire interface. The sequence consists of a reset pulse from the µC followed by a presence pulse from the MAX16816. At this point the µC must send PASS_CODE_ONE and PASS_CODE_TWO. These pass codes must be received by the MAX16816 within the 8ms programming slot to allow the MAX16816 to enter the EE programming mode.

1-Wire Signaling

The MAX16816 requires strict protocols to ensure data integrity. The protocol consists of four types of signaling on one line: reset sequence with Reset Pulse and Presence Pulse, Write-Zero, Write-One, and Read-Data. Except for the Presence Pulse, the bus master initiates all falling edges.

Externally pull $\overline{FAULT}$ below V_{IL} to indicate a logic-input low. Release the pulldown device to indicate a logic-input high. The MAX16816 will pull $\overline{FAULT}$ low below V_{OL} to indicate a logic-output low. $\overline{FAULT}$ is pulled high with an internal 10kΩ resistor above V_{OH} to indicate a logic-output high.

Initialization Procedure (Reset and Presence Pulses)

All 1-Wire communication with the MAX16816 begins with an initialization sequence that consists of a Reset Pulse from the master followed by a Presence Pulse from the MAX16816 (Figure 6). When the MAX16816 sends the Presence Pulse in response to the Reset Pulse, it is indicating to the master that it is ready to receive and transmit data.

During the initialization sequence, the bus master transmits the reset pulse by pulling the 1-Wire bus low for a minimum of 480µs. The bus master then releases the bus and goes into receive mode. When the bus is released, the pullup resistor pulls the 1-Wire bus high. When the MAX16816 detects this rising edge, it waits 15µs to 60µs and then transmits a Presence Pulse by pulling the 1-Wire bus low for 60µs to 240µs.

Read and Write Time Slots

The bus master writes data to the MAX16816 during write time slots and reads data from the MAX16816 during read time slots. One bit of data is transmitted over the 1-Wire bus per time slot.

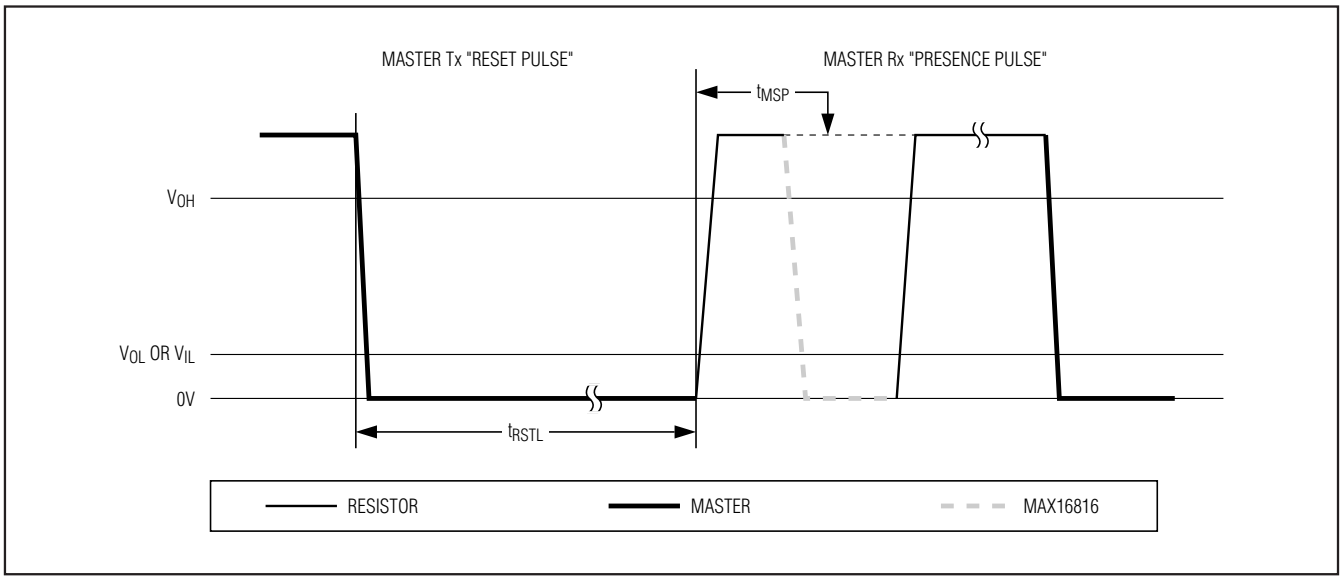

Figure 6. 1-Wire Initialization Timing

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Write Time Slots

There are two types of write time slots: Write-1 time slots and Write-0 time slots. The bus master uses a Write-1 time slot to write a logic '1' to the MAX16816 and a Write-0 time slot to write a logic '0'. All write time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between individual Write slots. Both types of write time slots are initiated by the master pulling the 1-Wire bus low (Figures 7 and 8).

To generate a Write-1 time slot, the bus master must release the 1-Wire bus within 15µs after pulling the bus low. When the bus is released, the pullup resistor will pull the bus high. To generate a Write-0 time slot, the bus master must continue to hold the bus low for the duration of the time slot (at least 60µs) after pulling the 1-Wire bus low. The MAX16816 samples the 1-Wire bus during a window that lasts from 15µs to 60µs after the master initiates the Write time slot. If the bus is high during the samples window, a '1' is written to the MAX16816. If the line is low, a '0' is written to the MAX16816.

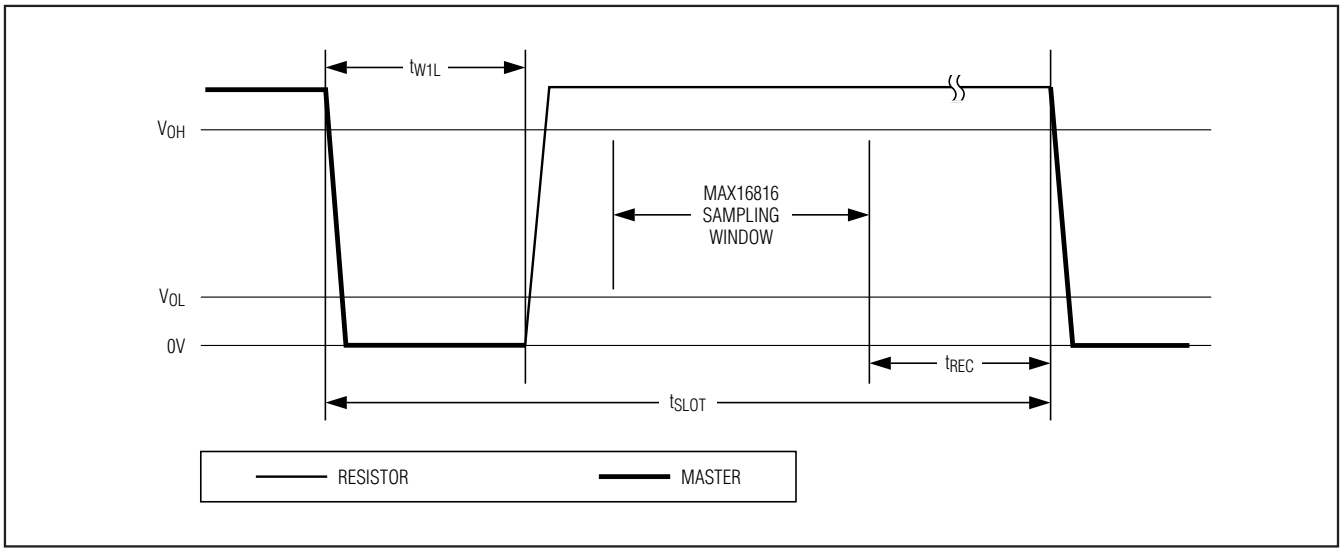

Figure 7. 1-Wire Write-1 Time Slot

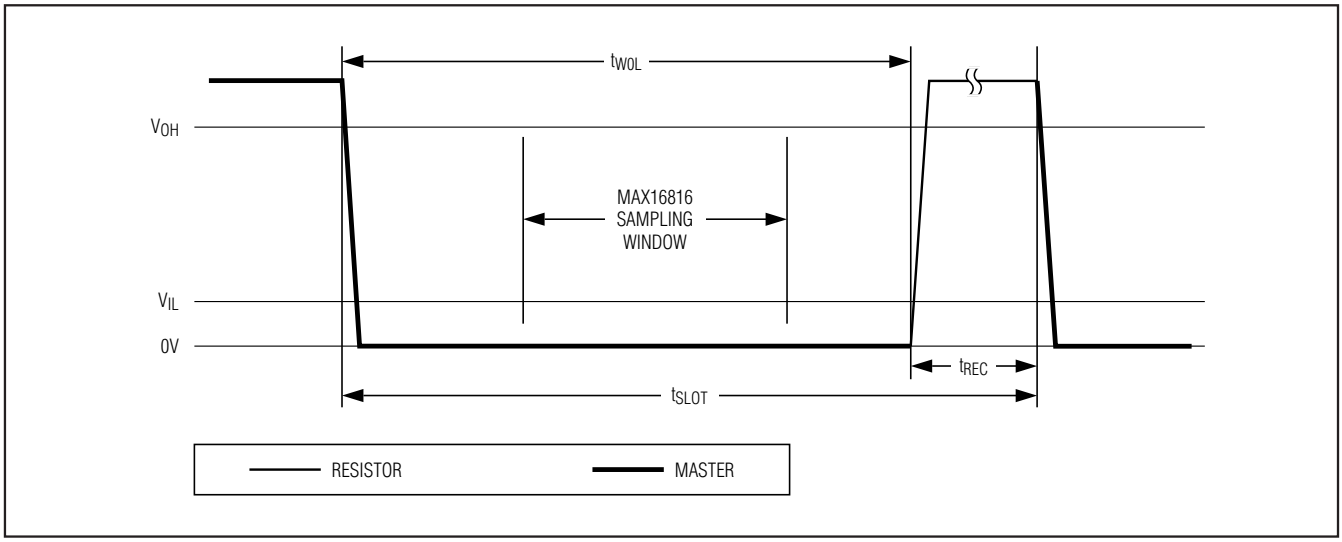

Figure 8. 1-Wire Write-0 Time Slot

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Read Time Slots

The MAX16816 can only transmit data to the master when the master issues read time slots.

All read time slots must be a minimum of 60µs in duration with a minimum of a 1µs recovery time between slots. A read time slot is initiated by the master device pulling the 1-Wire bus low for a minimum of 1µs and then releasing it (Figure 9). After the master initiates the read time slot, the MAX16816 will transmit a '1' or a '0' on the bus. The MAX16816 transmits a '1' by leaving the bus high and transmits a '0' by pulling the bus low. When transmitting a '0', the MAX16816 will release the bus before the end of the time slot, and the bus will be pulled back to its high idle state by the pullup resistor. Output data from the MAX16816 is valid for 15µs after the falling edge that initiated the read time slot. Therefore, the master must release the bus and then sample the bus state within 15µs from the start of the slot.

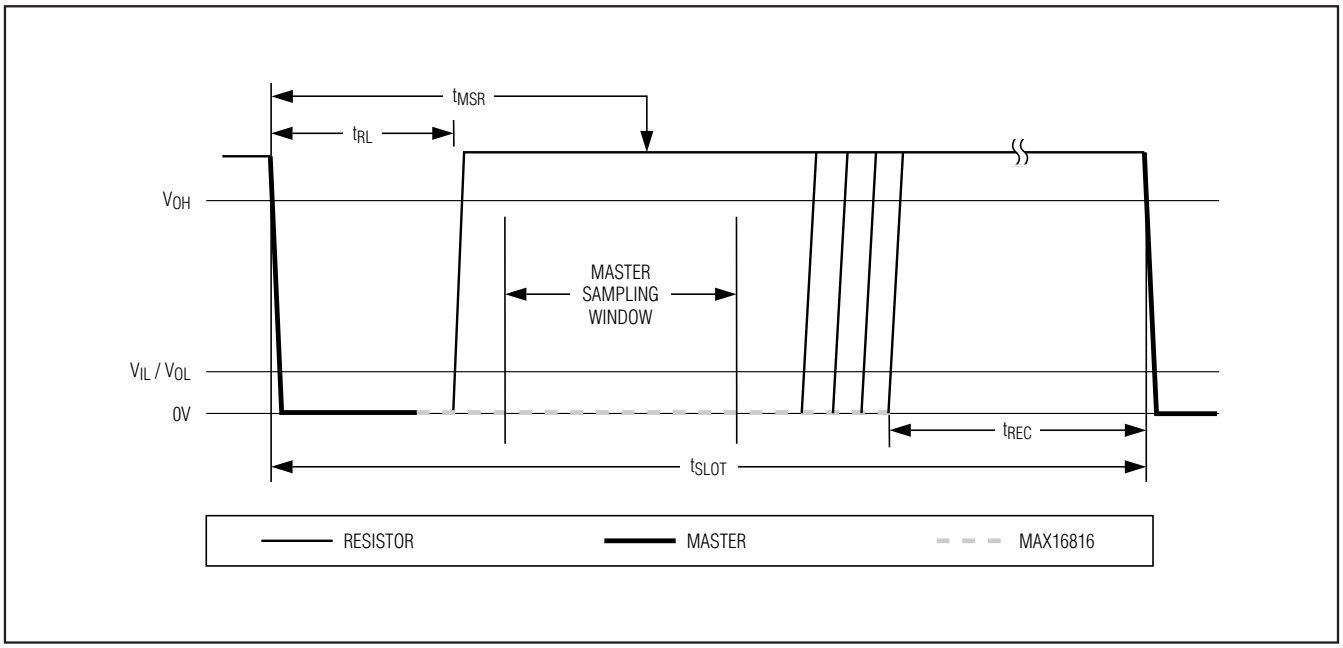

Figure 9. 1-Wire Read Time Slot

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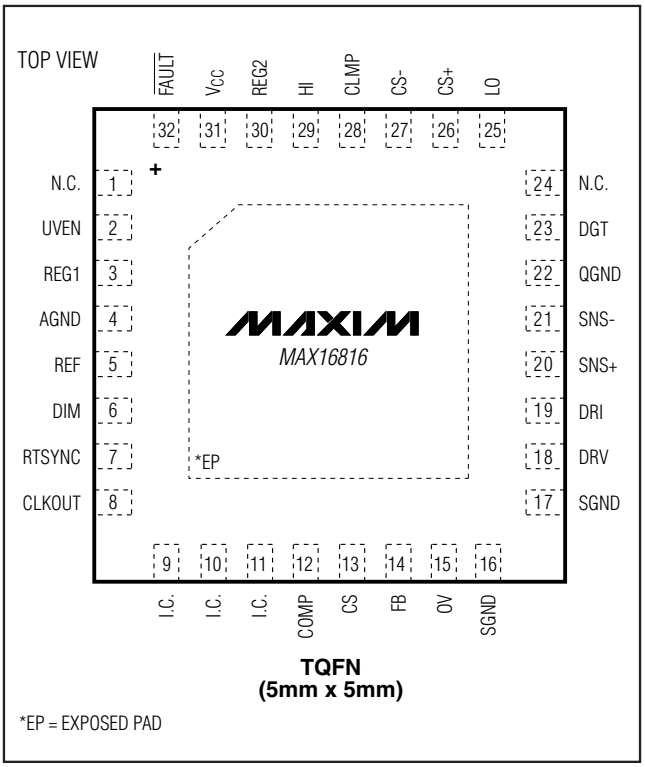
Chip Information

PROCESS: BiCMOS

Pin Configuration



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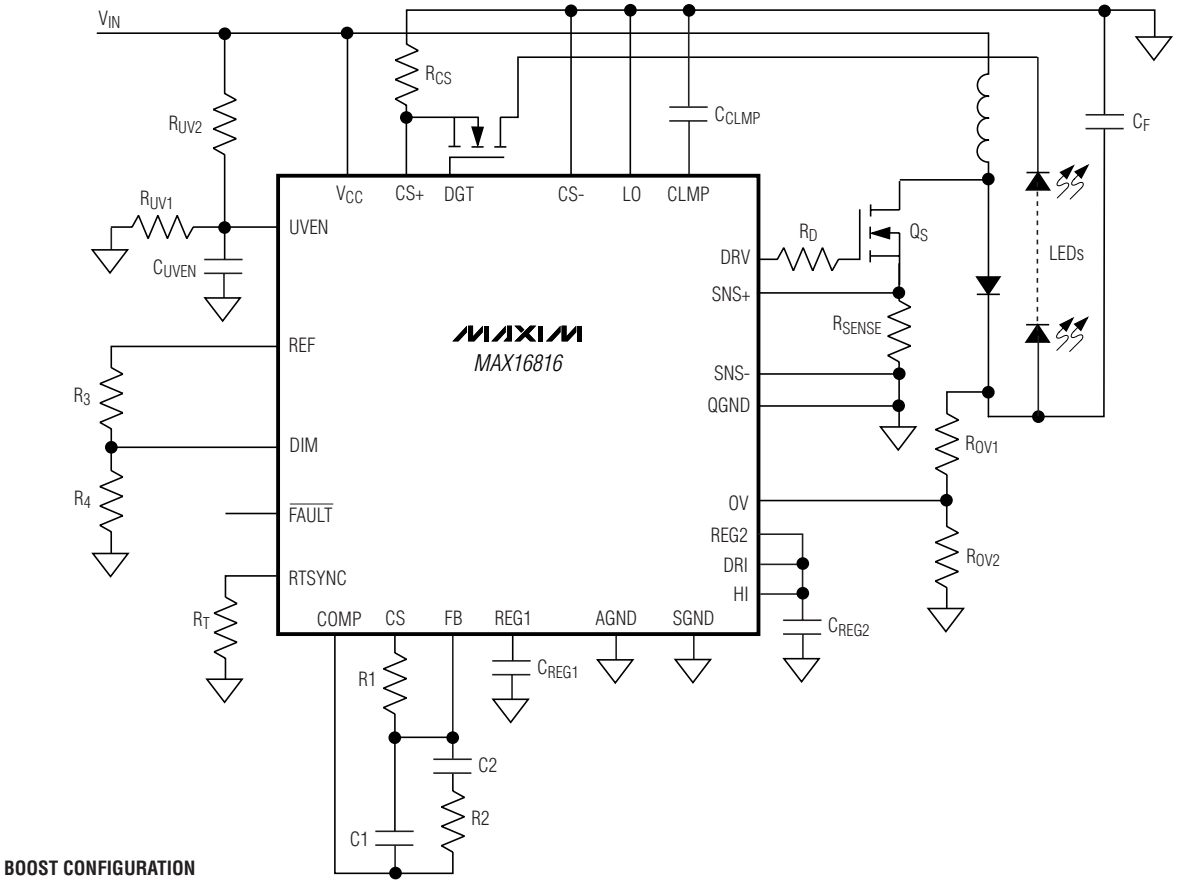
Typical Operating Circuits (continued)



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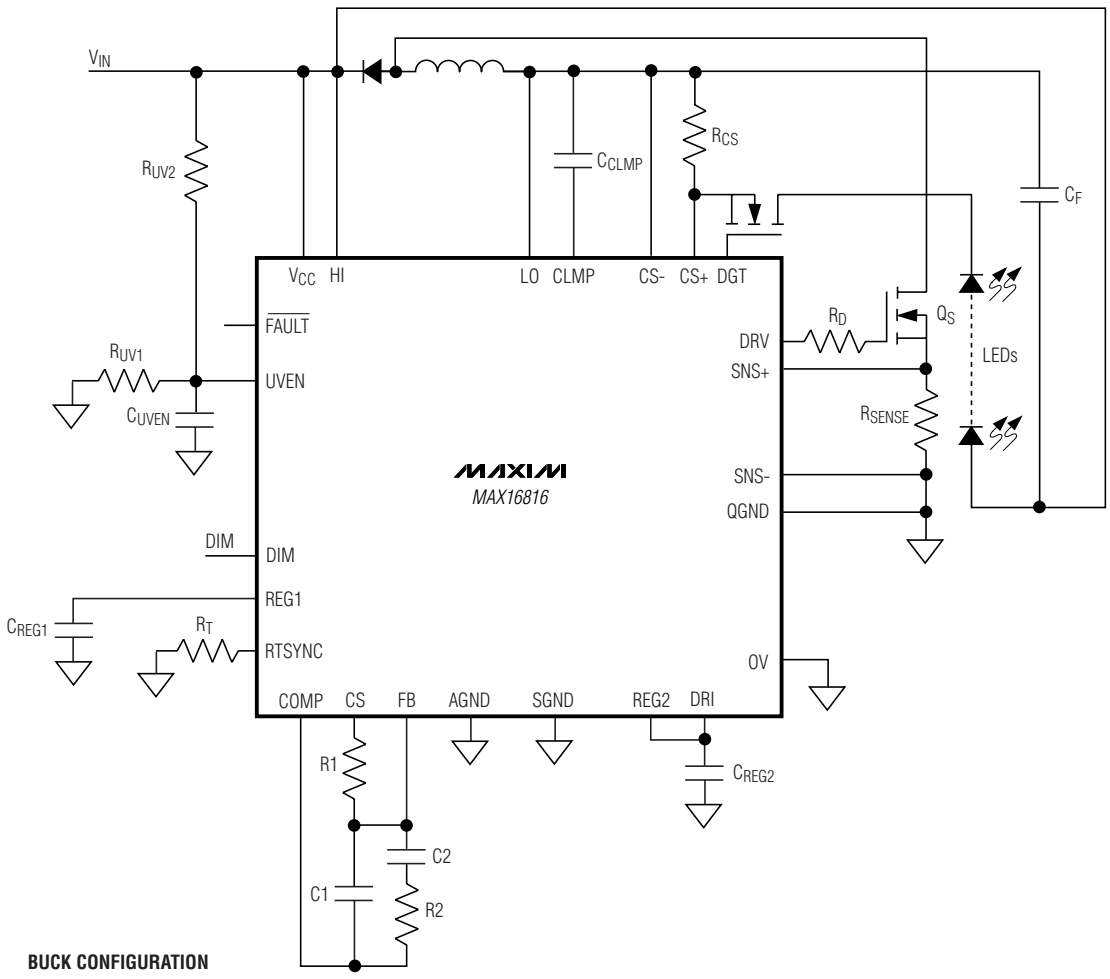
Typical Operating Circuits (continued)



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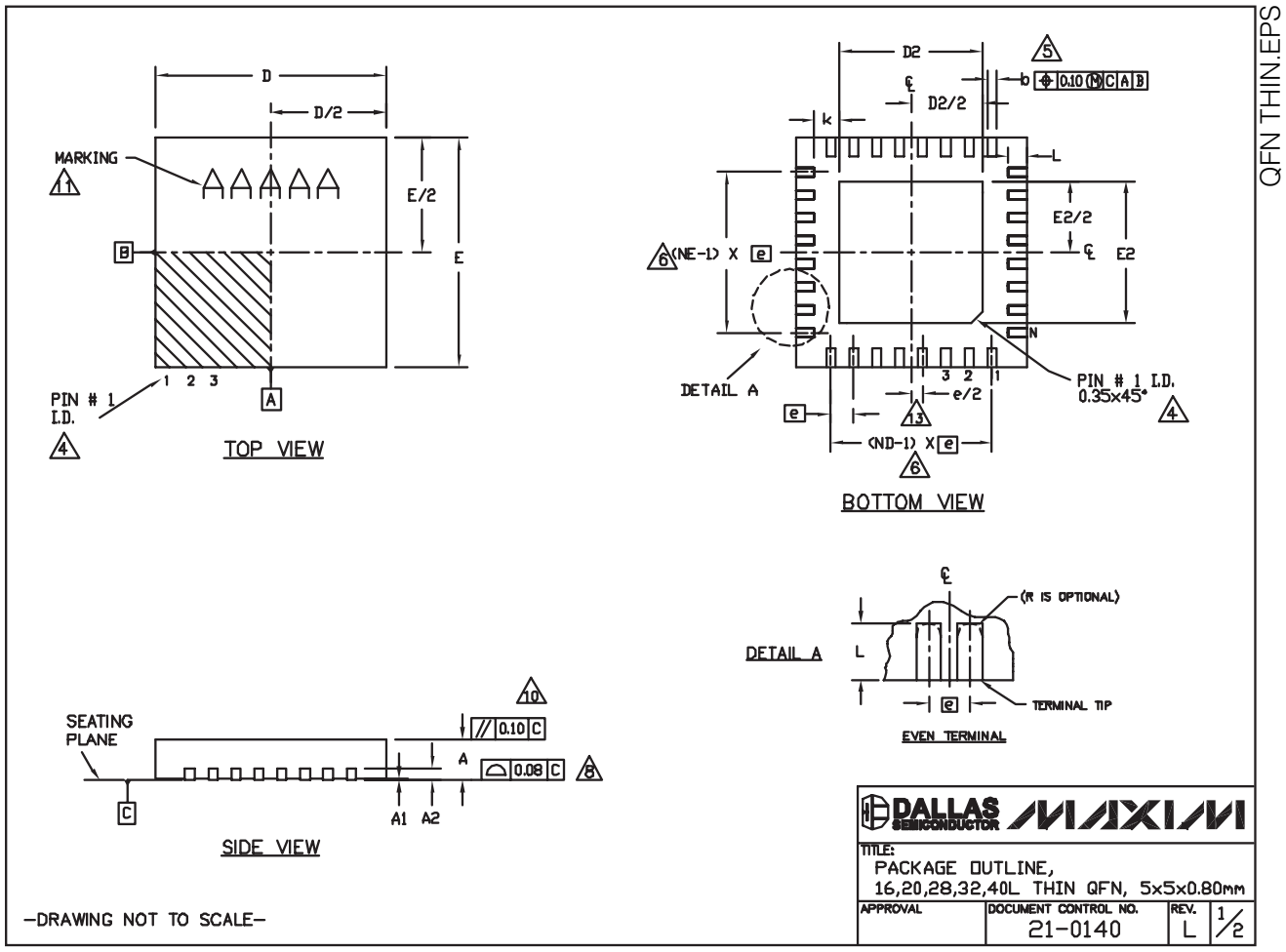
Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

QFN THIN.EPS



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Programmable Switch-Mode LED Driver with Analog-Controlled PWM Dimming

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS																
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5			
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25	
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.			
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50	
N	16			20			28			32			40			
ND	4			5			7			8			10			
NE	4			5			7			8			10			
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----			

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

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