National Semiconductor

June 2007

LP55281
Quad RGB Driver

General Description

LP55281 is a quad RGB LED driver for handheld devices. It can drive 4 RGB LED sets and a single fun light LED. The boost DC-DC converter drives high current loads with high efficiency. The RGB driver can drive individual color LEDs or RGB LEDs powered from boost output or external supply. Built-in audio synchronization feature allows user to synchronize the fun light LED to audio inputs. The flexible SPI/I²C interface allows easy control of LP55281. Small Micro SMD or Micro SMDxt package together with minimum number of external components is a best fit for handheld devices. LP55281 has also a LED test feature, which can be used for example in production for checking the LED connections.

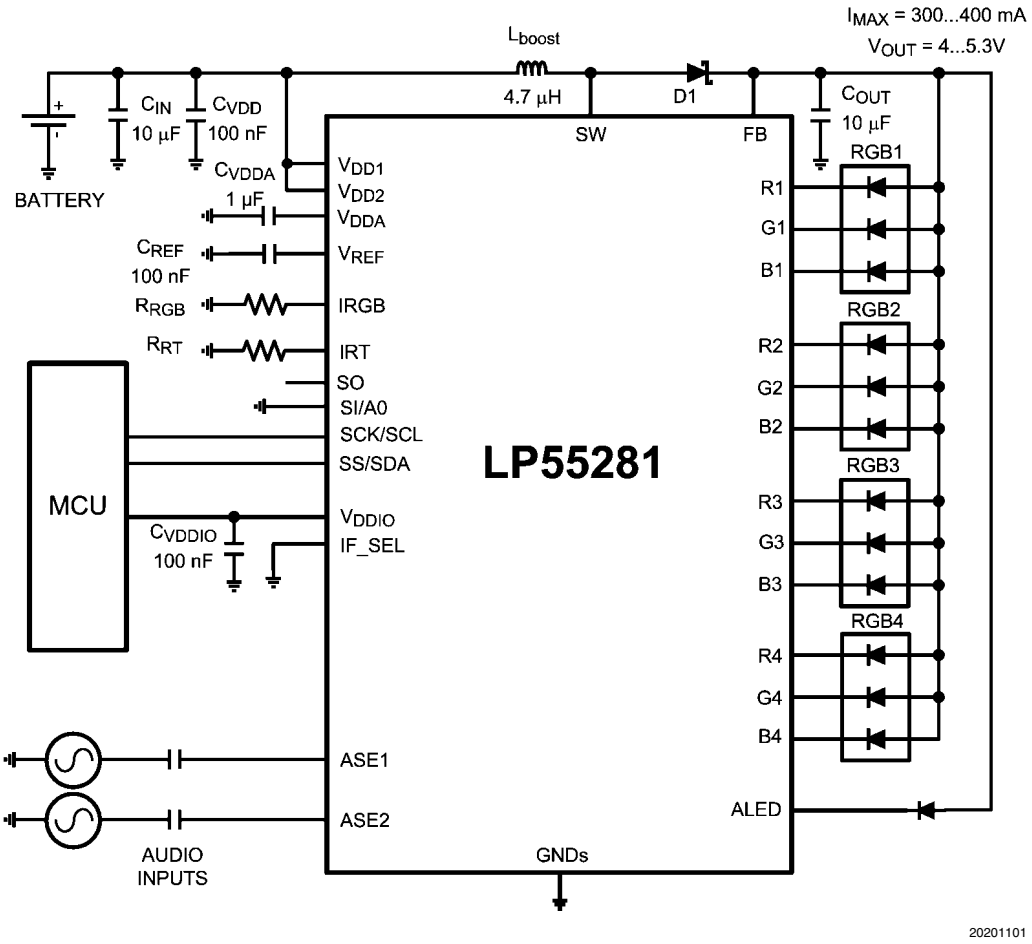
Features

- Audio synchronization for a single fun light LED
- 4 PWM controlled RGB LED drivers
- High efficiency Boost DC-DC converter
- SPI/I²C compatible interface
- 2 addresses in I²C compatible interface
- LED connectivity test through the serial interface
- Small 36-bump Micro SMD (3 mm x 3 mm x 0.6 mm) or 36-bump Micro SMDxt package (3 mm x 3 mm x 0.65 mm)

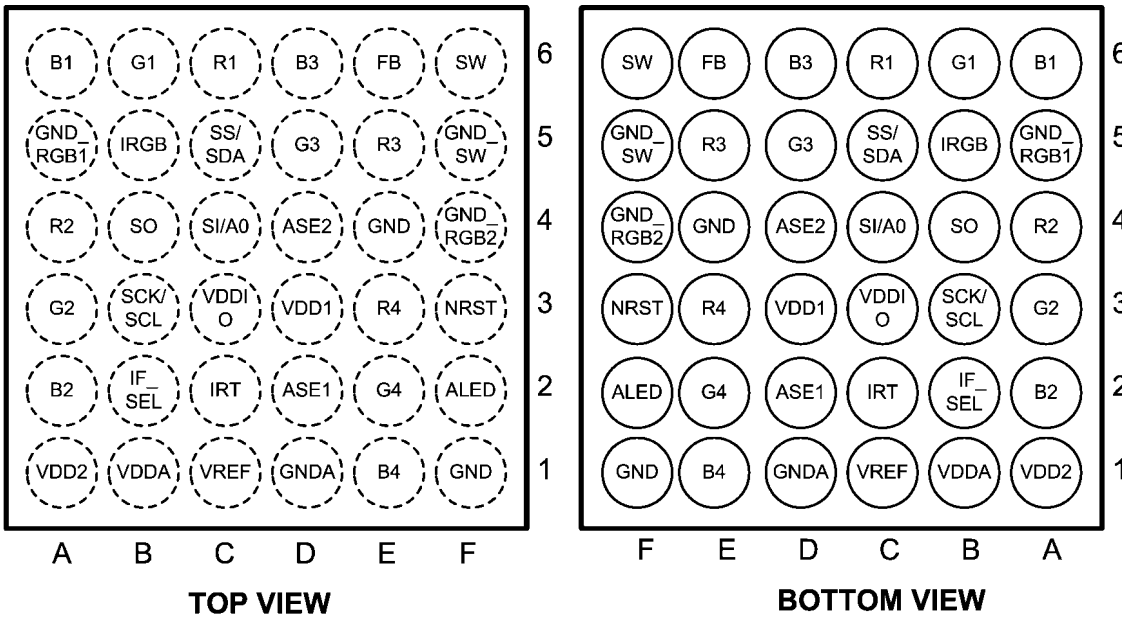
Applications

- Cellular Phones
- PDAs, MP3 players

Typical Application



Connection Diagram



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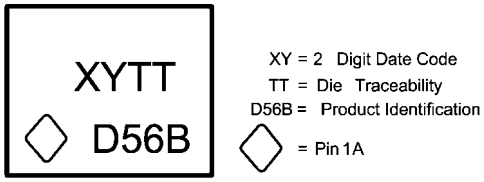
36-bump Micro SMD package, 3 * 3 * 0.6 mm body size, 0.5 mm pitch NS Package Number TLA36AAA
36-bump Micro SMDxt package, 3 * 3 * 0.65 mm body size, 0.5 mm pitch NS Package Number RLA36AAA

Package Mark



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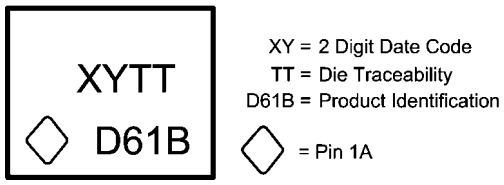
36-bump Micro SMD package, 3 * 3 * 0.6 mm body size, 0.5 mm pitch NS Package Number TLA36AAA



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36-bump Micro SMDxt package, 3 * 3 * 0.65 mm body size, 0.5 mm pitch NS Package Number RLA36AAA

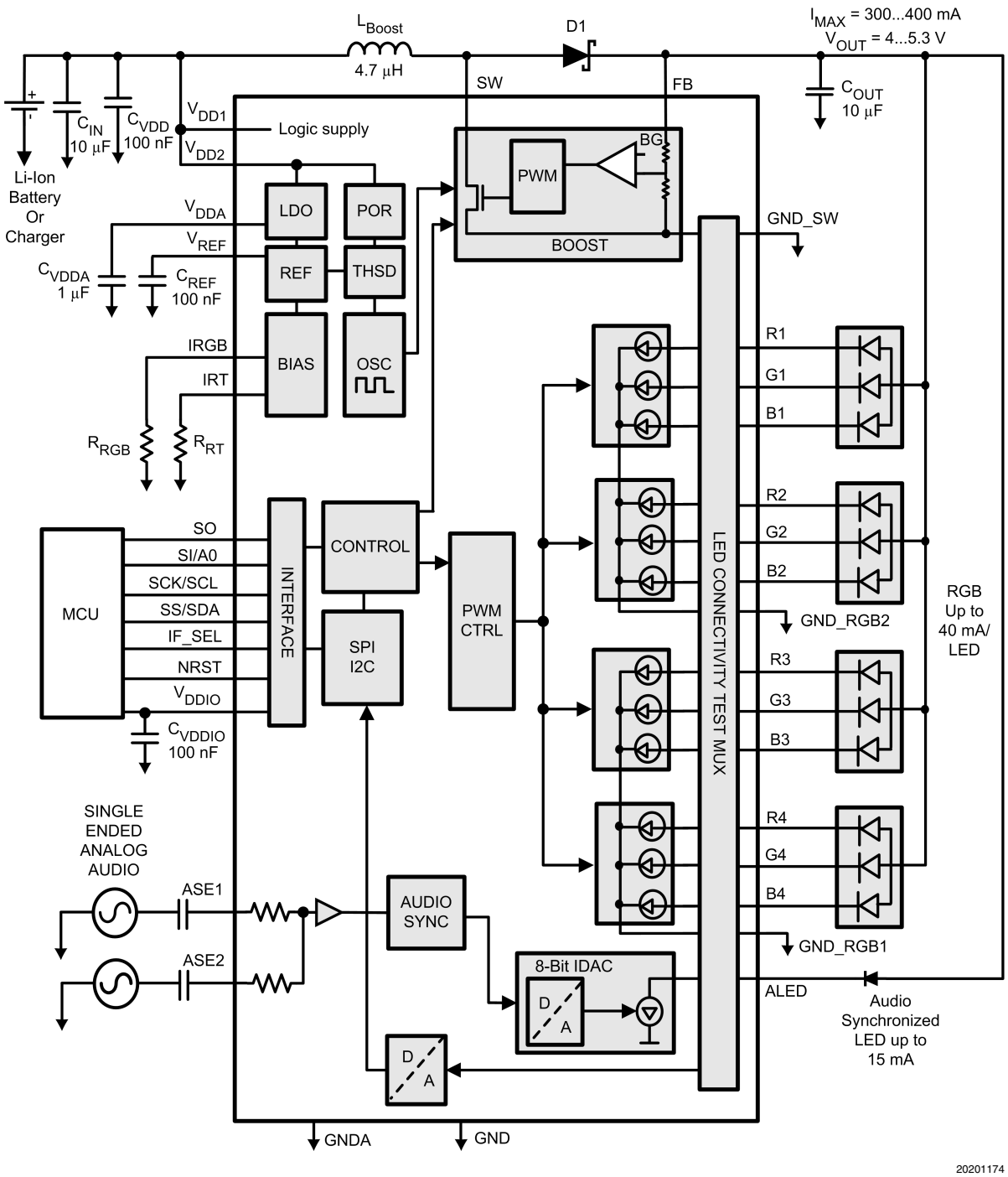
Ordering Information

Order Number	Package Marking	Supplied As	Spec/Flow
LP55281TL	D56B	TNR 250	NoPB
LP55281TLX	D56B	TNR 1000	NoPB
LP55281RL	D61B	TNR250	NoPB
LP55281RLX	D61B	TNR1000	NoPB

Pin Descriptions

Pin	Name	Type	Description
6F	SW	Output	Boost Converter Power Switch
6E	FB	Input	Boost Converter Feedback
6D	B3	Output	Blue LED 3 Output
6C	R1	Output	Red LED 1 Output
6B	G1	Output	Green LED 1 Output
6A	B1	Output	Blue LED 1 Output
5F	GND_SW	Ground	Power Switch Ground
5E	R3	Output	Red LED 3 Output
5D	G3	Output	Green LED 3 Output
5C	SS/SDA	Logic Input/Output	Slave Select (SPI), Serial Data In/Out (I^2C)
5B	IRGB	Input	Bias Current Set Resistor for RGB Drivers
5A	GND_RGB1	Ground	Ground for RGB1-2 Currents
4F	GND_RGB2	Ground	Ground for RGB3-4 Currents
4E	GND	Ground	Ground
4D	ASE2	Input	Audio Synchronization Input 2
4C	SI/A0	Logic Input	Serial Input (SPI), Address Select (I^2C)
4B	SO	Logic Output	Serial Data Out (SPI)
4A	R2	Output	Red LED 2 Output
3F	NRST	Input	Asynchronous Reset, Active Low
3E	R4	Output	Red LED 4 Output
3D	VDD1	Power	Supply Voltage
3C	VDDIO	Power	Supply Voltage for Input/Output Buffers and Drivers
3B	SCK/SCL	Logic Input	Clock (SPI/I^2C)
3A	G2	Output	Green LED 2 Output
2F	ALED	Output	Audio Synchronized LED Output
2E	G4	Output	Green LED 4 Output
2D	ASE1	Input	Audio Synchronization Input 1
2C	IRT	Input	Oscillator Frequency Resistor
2B	IF_SEL	Logic Input	Interface (SPI or I^2C compatible) Selection (IF_SEL = 1 for SPI)
2A	B2	Output	Blue LED 2 Output
1F	GND	Ground	Ground
1E	B4	Output	Blue LED 4 Output
1D	GNDA	Ground	Ground for Analog Circuitry
1C	VREF	Output	Reference Voltage
1B	VDDA	Power	Internal LDO Output
1A	VDD2	Power	Supply Voltage

Block Diagram



Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V (SW, FB, R1-4, G1-4, B1-4, ALED (Notes 3, 4))	-0.3V to +7.2V
V_{DD1}, V_{DD2}, V_{DDIO}, V_{DDA}	-0.3V to +6.0V
Voltage on ASE1-2, IRT, IRGB, VREF	-0.3V to V_{DD1} +0.3V with 6.0V max
Voltage on Logic Pins	-0.3V to V_{DDIO} + 0.3V with 6.0V max
V (all other pins): Voltage to GND	-0.3V to +6.0V
I (VREF)	10 µA
I (R1-4, G1-4, B1-4)	100 mA
Continuous Power Dissipation (Note 5)	Internally Limited
Junction Temperature (T_{J-MAX})	150°C
Storage Temperature Range	-65°C to +150°C
Maximum Lead Temperature (Reflow soldering, 3 times) (Note 6)	260°C

ESD Rating

Human Body Model (Note 7)	2 kV

Operating Ratings (Notes 1, 2)

V (SW, FB, R1-4, G1-4, B1-4, ALED)	0 to 6.0V
$V_{DD1,2}$ with external LDO	2.7V to 5.5V
$V_{DD1,2}$ with internal LDO	3.0V to 5.5V
V_{DDA}	2.7V to 2.9V
V_{DDIO}	1.65V to V_{DD1}
Voltage on ASE1-2	0.1V to V_{DDA} - 0.1V
Recommended Load Current	0 mA to 300 mA
Junction Temperature (T_J) Range	-30°C to +125°C
Ambient Temperature (T_A) Range (Note 8)	-30°C to +85°C

Thermal Properties

Junction-to-Ambient Thermal Resistance (θ_{JA}), TLA36AAA Package (Note 9)	60°C/W

Electrical Characteristics (Notes 2, 10)

Limits in standard typeface are for T_J = 25°C. Limits in **boldface** type apply over the operating ambient temperature range (-30°C < T_A < +85°C). Unless otherwise noted, specifications apply to the LP55281 Block Diagram with: V_{DD1} = V_{DD2} = 3.6V, V_{DDIO} = 2.8V, $C_{V_{DD}}$ = $C_{V_{DDIO}}$ = 100 nF, C_{OUT} = C_{IN} = 10 µF, $C_{V_{DDA}}$ = 1 µF, C_{REF} = 100 nF, L1 = 4.7 µH, R_{RGB} = 8.2 kΩ and R_{RT} = 82 kΩ (Note 11).

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{DD}	Standby supply current (V_{DD1} + V_{DD2} + leakage to SW, FB, RGB1-4, ALED)	NSTBY = L SCK = SS = SI = H NRST = L		1	**10**	µA
	No-Boost supply current (V_{DD1} + V_{DD2})	NSTBY = H, EN_BOOST = L SCK = SS = SI = H Audio synchronization and LEDs OFF		350		µA
	No-load supply current (V_{DD1} + V_{DD2})	NSTBY = H, EN_BOOST = H, SCK = SS = SI = H Audio synchronization and LEDs OFF Autoload OFF		0.6		mA
	Total RGB drivers quiescent current (V_{DD1} + V_{DD2})	EN_RGBx = H		250		µA
	ALED driver current (V_{DD1} + V_{DD2})	ALED[7:0] = FFh ALED[7:0] = 00h		180 0		µA µA
	Audio Synchronization current (V_{DD1} + V_{DD2})	Audio Synchronization ON $V_{DD1,2}$ = 2.8V $V_{DD1,2}$ = 3.6V		390 700		µA µA
I_{DDIO}	V_{DDIO} Standby Supply current	NSTBY = L SCK = SS = SI = H			**1**	µA
	V_{DDIO} supply current	1 MHz SCK frequency in SPI mode, C_L = 50 pF at SO pin		20		µA

V_{DDA}	Output voltage of internal LDO for analog parts	(Note 12)	-3%	2.80	+3%	V

MAGNETIC BOOST DC/DC CONVERTER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
I_{LOAD}	Recommended Load Current	3.0V ≤ V_{IN} V_{OUT} = 5V	0		300	mA
		3.0V ≤ V_{IN} V_{OUT} = 4V	0		400	mA
V_{OUT}	Output Voltage Accuracy (FB pin)	3.0V ≤ V_{IN} ≤ V_{OUT} - 0.5 V_{OUT} = 5V	**-5**		**+5**	%
	Output Voltage (FB pin)	1 mA ≤ I_{LOAD} ≤ 300 mA V_{IN} > V_{OUT} + $V_{SCHOTTKY}$ (Note 14)		V_{IN} - $V_{schottky}$		V
RDS_{ON}	Switch ON resistance	$V_{DD1,2}$ = 3.0V, I_{SW} = 0.5 A		0.4	**0.8**	Ω
f_{Boost}	PWM mode switching frequency	RT = 82 kΩ freq_sel[2:0] = 1XX		2		MHz
	Frequency Accuracy	2.7V ≤ V_{DDA} ≤ 2.9V RT = 82 kΩ ± 1%	-7 **-10**	± 3	+7 **+10**	%
t_{PULSE}	Switch pulse minimum width	no load		30		ns
$t_{STARTUP}$	Startup time	Boost startup from STANDBY (Note 13)		10		ms
I_{SW_MAX}	SW pin current limit		700 **550**	800	900 **950**	mA

RGB DRIVER ELECTRICAL CHARACTERISTICS (R1-4, G1-4, B1-4)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{LEAKAGE}$	R1-4, G1-4, B1-4 pin leakage current	5.5V at measured pin		0.1	**1**	µA
I_{RGB}	Maximum Recommended Sink Current	Limited with external resistor R_{RGB}			**40**	mA
	Accuracy @ 15 mA	R_{RGB} = 8.2 kΩ ± 1 %		± 5		%
	Current mirror ratio	(Note 13)		1 : 100		
	RGB1-4 current mismatch	I_{RGB} = 15 mA		± 5		%
f_{PWM}	RGB switching frequency	Accuracy defined by internal oscillator, frequency value selectable		f_{PWM}		

AUDIO SYNCHRONIZATION INPUT ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
Z_{IN}	Input Impedance of ASE1, ASE2	(Note 13)	10	15		kΩ
A_{IN}	ASE1, ASE2 Audio Input Level Range (peak-to-peak)	Min input level needs maximum gain; Max input level for minimum gain	0		1600	mV

ALED DRIVER ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Condition	Min	Typ	Max	Units
$I_{leakage}$	Leakage current	V_{ALED} = 5.5V		0.03	**1**	µA

I_{ALED}	ALED current tolerance	I_{ALED} set to 13.2 mA	**11.9** **-10**	13.2	**14.5** **+10**	mA %
LOGIC INTERFACE CHARACTERISTICS						
Symbol	**Parameter**	**Condition**	**Min**	**Typ**	**Max**	**Units**
Logic Input SS/SDA, SI/A0, SCK/SCL, IF_SEL						
V_{IL}	Input Low Level				**0.2*V_{DDIO}**	V
V_{IH}	Input High Level		**0.8*V_{DDIO}**			V
I_I	Logic Input Current		**-1.0**		**1.0**	µA
$f_{SCK/SCL}$	Clock Frequency	I²C			**400**	kHz
		SPI Mode, $V_{DDIO > 1.8V}$ (Note 13)			**13**	MHz
		SPI Mode, 1.65V ≤ V_{DDIO} < 1.8V			**5**	MHz
Logic Input NRST						
V_{IL}	Input Low Level				**0.5**	V
V_{IH}	Input High Level		**1.2**			V
I_I	Logic Input Current		**-1.0**		**1.0**	µA
t_{NRST}	Reset Pulse Width		**10**			µs
Logic Output SO						
V_{OL}	Output Low Level	I_{SO} = 3 mA V_{DDIO} > 1.8V		0.3	**0.5**	V
		I_{SO} = 2 mA 1.65V ≤ V_{DDIO} < 1.8V		0.3	**0.5**	
V_{OH}	Output High Level	I_{SO} = -3 mA V_{DDIO} > 1.8V	**V_{DDIO} -** **0.5**	V_{DDIO} - 0.3		V
		I_{SO} = -2 mA 1.65V ≤ V_{DDIO} < 1.8V	**V_{DDIO} -** **0.5**	V_{DDIO} - 0.3		
I_L	Output Leakage Current	V_{SO} = 2.8V			**1.0**	µA
Logic Output SDA						
V_{OL}	Output Low Level	I_{SDA} = 3 mA		0.3	**0.5**	V

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the component may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pins.

Note 3: Battery/Charger voltage should be above 6V no more than 10% of the operational lifetime.

Note 4: Voltage tolerance of LP55281 above 6.0V relies on fact that V_{DD1} and V_{DD2} (2.8V) are available (ON) at all conditions. If V_{DD1} and V_{DD2} are not available (ON) at all conditions, National Semiconductor® does not guarantee any parameters or reliability for this device.

Note 5: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 160°C (typ.) and disengages at T_J = 140°C (typ.)

Note 6: For detailed soldering specifications and information, please refer to National Semiconductor Application Note AN1112 : Micro SMD Wafer Level Chip Scale Package or National Semiconductor Application Note AN1412 : Micro SMDxt Wafer Level Chip Scale Package.

Note 7: The Human Body Model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. MIL-STD-883 3015.7

Note 8: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to-ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 9: Junction-to-Ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

Note 10: Min and Max limits are guaranteed by design, test or statistical analysis. Typical numbers are not guaranteed, but do represent the most likely norm.

Note 11: Low-ESR Surface-Mount Ceramic Capacitors (MLCCs) used in setting electrical characteristics.

Note 12: V_{DDA} output is not recommended for external use.

Note 13: Data guaranteed by design

Note 14: When V_{IN} rises above V_{OUT} + $V_{SCHOTTKY}$, V_{OUT} starts to follow the V_{IN} voltage rise so that $V_{OUT} = V_{IN} - V_{SCHOTTKY}$

Modes of Operation

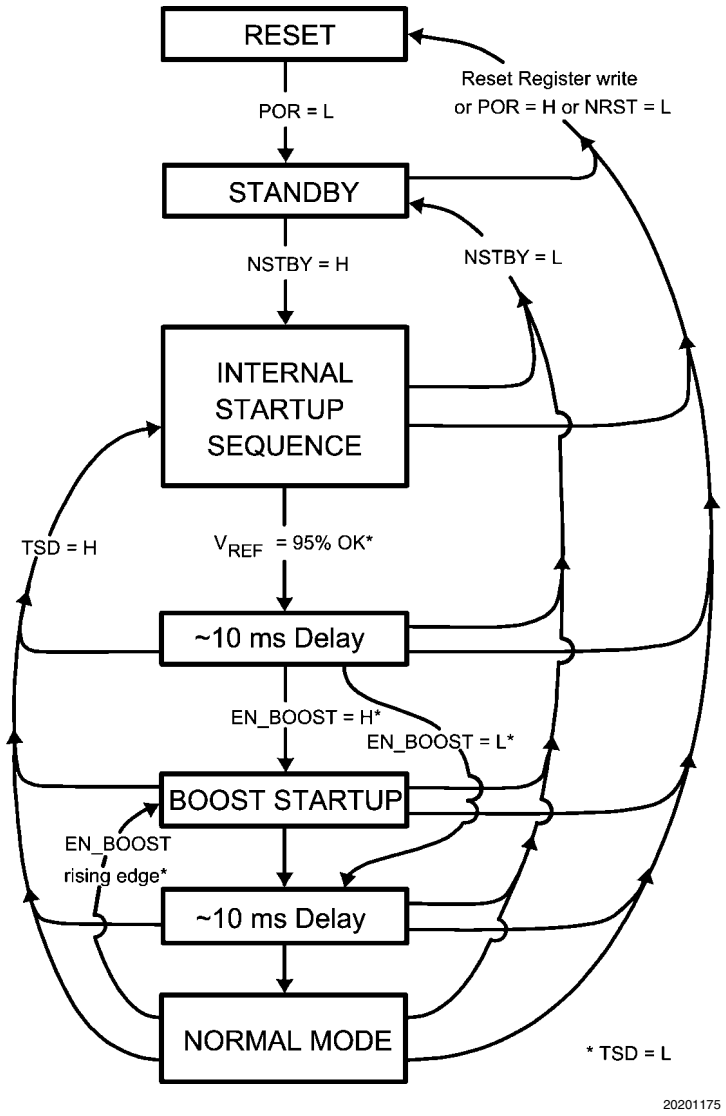
RESET: In the RESET mode all the internal registers are reset to the default values and the device goes to STANDBY mode after reset. NSTBY control bit is low after reset by default. Reset is entered always if Reset Register is written, internal Power On Reset is active, or NRST pin is pulled down externally. The LP55281 can be reset by writing any data to the Reset Register (address 60H). Power On Reset (POR) will activate during the device startup or when the supply voltage V_{DD2} falls below 1.5V. Once V_{DD2} rises above 1.5V, POR will inactivate and the device will continue to the STANDBY mode.

STANDBY: The STANDBY mode is entered if the register bit NSTBY is LOW. This is the low power consumption mode, when all circuit functions are disabled. Registers can be written in this mode and the control bits are effective immediately after startup.

STARTUP: When NSTBY bit is written high, the INTERNAL STARTUP SEQUENCE powers up all the needed internal blocks (VREF, Oscillator, etc.). To ensure the correct oscillator initialization, a 10 ms delay is generated by the internal state-machine. If the device temperature rises too high, the Thermal Shutdown (TSD) disables the device operation and STARTUP mode is entered until no thermal shutdown is present.

BOOST STARTUP: Soft start for boost output is generated in the BOOST STARTUP mode. The boost output is raised in PWM mode during the 10 ms delay generated by the state-machine. The Boost startup is entered from Internal Startup Sequence if EN_BOOST is HIGH or from Normal mode when EN_BOOST is written HIGH. During the 10 ms Boost Startup time all LED outputs are switched off to ensure smooth startup.

NORMAL: During NORMAL mode the user controls the device using the Control Registers. The registers can be written in any sequence and any number of bits can be altered in a register in one write.



Magnetic Boost DC/DC Converter

The LP55281 Boost DC/DC Converter generates a 4.0 - 5.3V supply voltage for the LEDs from single Li-Ion battery (3V... 4.5V). The output voltage is controlled with an 8-bit register in 9 steps. The converter is a magnetic switching PWM mode DC/DC converter with a current limit. The converter has three options for switching frequency, 1 MHz, 1.67 MHz and 2 MHz (default), when timing resistor RT is 82 kΩ. Timing resistor defines the internal oscillator frequency and thus directly affects boost frequency and all circuit's internally generated timing (RGB, ALED).

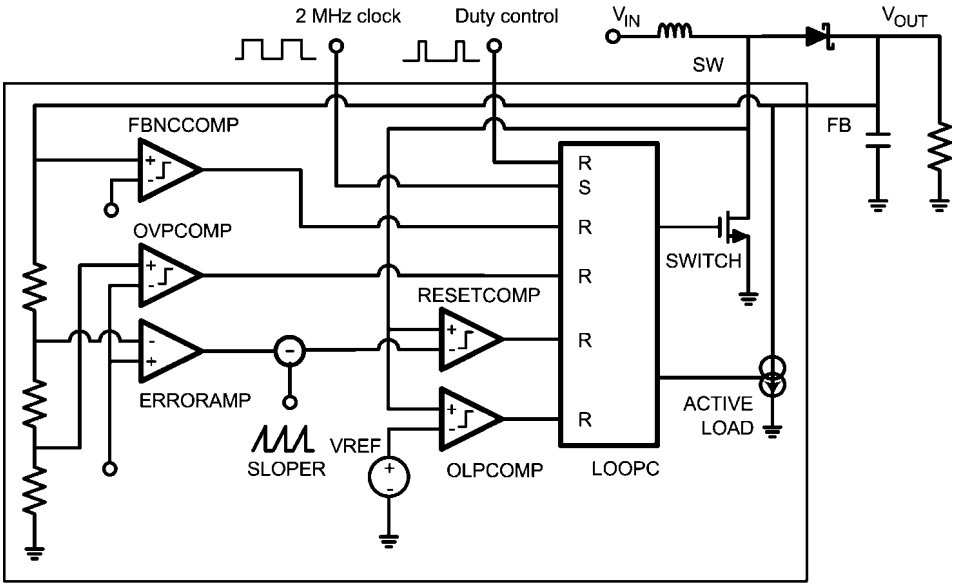
The LP55281 Boost Converter uses pulse-skipping elimination to stabilize the noise spectrum. Even with light load or no load a minimum length current pulse is fed to the inductor. An active load is used to remove the excess charge from the output capacitor at very light loads. At very light load and when input and output voltages are very close to each other, the pulse skipping is not completely eliminated. Output voltage should be at least 0.5V higher than input voltage to avoid pulse skipping. Reducing the switching frequency will also reduce the required voltage difference.

Active load can be disabled with the EN_AUTOLOAD bit. Disabling will increase the efficiency at light loads, but the downside is that pulse skipping will occur. The Boost Converter should be stopped when there is no load to minimise the current consumption.

The topology of the magnetic boost converter is called CPM control, current programmed mode, where the inductor current is measured and controlled with the feedback. The user can program the output voltage of the boost converter. The output voltage control changes the resistor divider in the feedback loop.

The following figure shows the boost topology with the protection circuitry. Four different protection schemes are implemented:

1. Over voltage protection, limits the maximum output voltage
   - — Keeps the output below breakdown voltage.
   - — Prevents boost operation if battery voltage is much higher than desired output.
2. Over current protection, limits the maximum inductor current
   - — Voltage over switching NMOS is monitored; too high voltages turn the switch off.
3. Feedback break protection. Prevents uncontrolled operation if FB pin gets disconnected.
4. Duty cycle limiting, done with digital control.



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Boost Converter Topology

BOOST STANDBY MODE

User can stop the Boost Converter operation by writing the Enables register bit EN_BOOST low. When EN_BOOST is written high, the converter starts for 10 ms in PFM mode and then goes to PWM mode.

BOOST OUTPUT VOLTAGE CONTROL

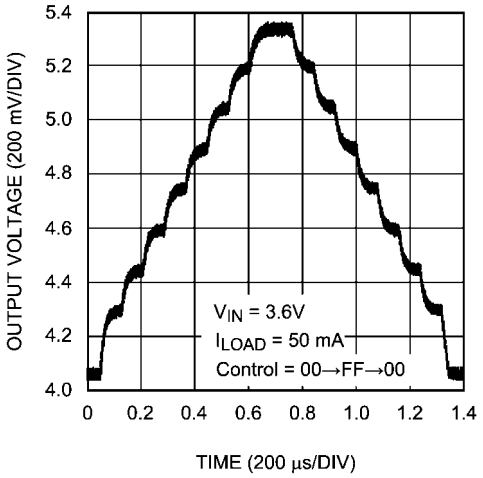
User can control the Boost output voltage by boost output 8-bit register.

Boost Output [7:0] Register 0Fh		Boost Output Voltage (typical)
Bin	Hex	
0000 0000	00	4.00
0000 0001	01	4.25
0000 0011	03	4.40
0000 0111	07	4.55
0000 1111	0F	4.70
0001 1111	1F	4.85
0011 1111	**3F**	**5.00 (default)**
0111 1111	7F	5.15
1111 1111	FF	5.30

BOOST FREQUENCY CONTROL

Register 'Frequency selections' (address 10h). Register default value after reset is 07h.

FRQ_SEL[2:0]	frequency
1XX	2.00 MHz
01X	1.67 MHz
001	1.00 MHz



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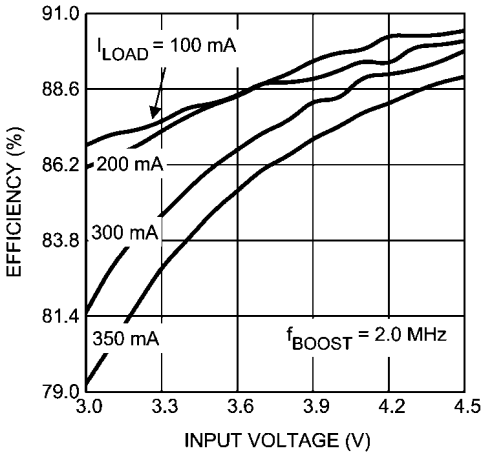
Boost Output Voltage Control

BOOST CONVERTER TYPICAL PERFORMANCE CHARACTERISTICS



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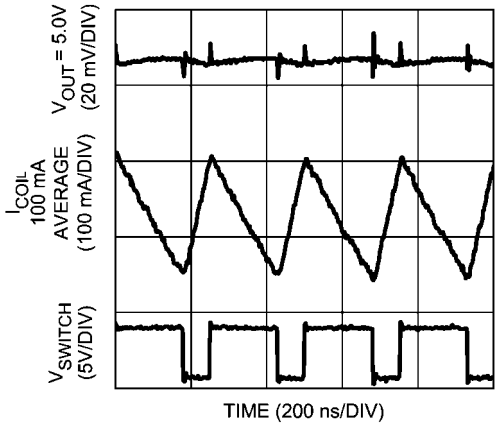
Boost Converter Efficiency



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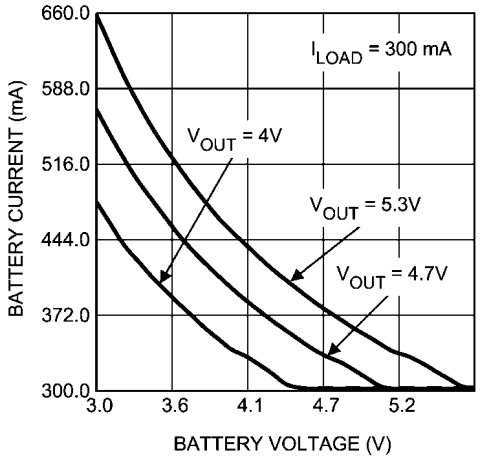
Boost Typical Waveforms with 100 mA Load



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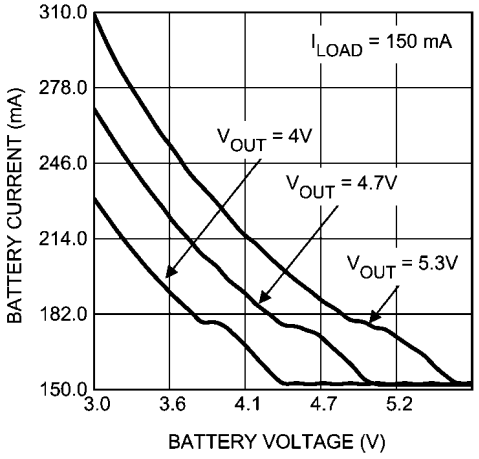
Battery Current vs Voltage



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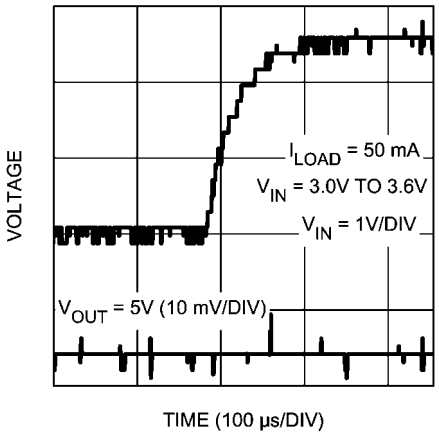
Battery Current vs Voltage



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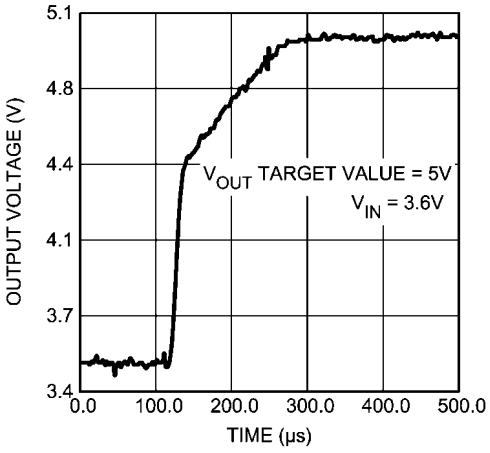
Boost Line Regulation



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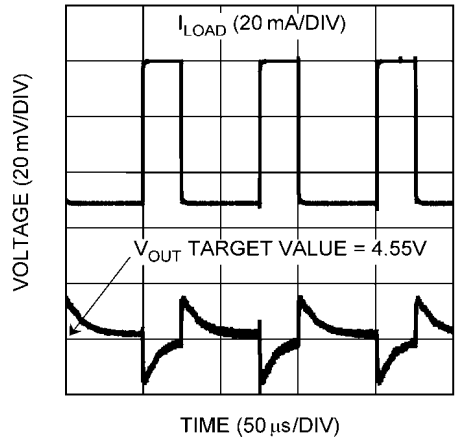
Boost Startup with No Load



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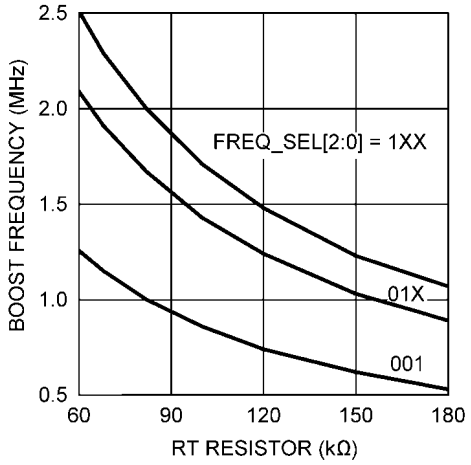
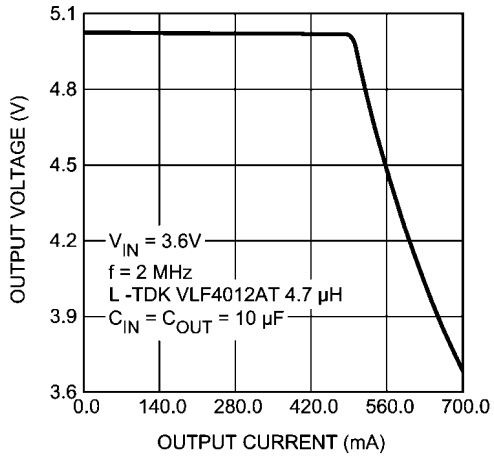
Boost Load Regulation, 50 - 100 mA

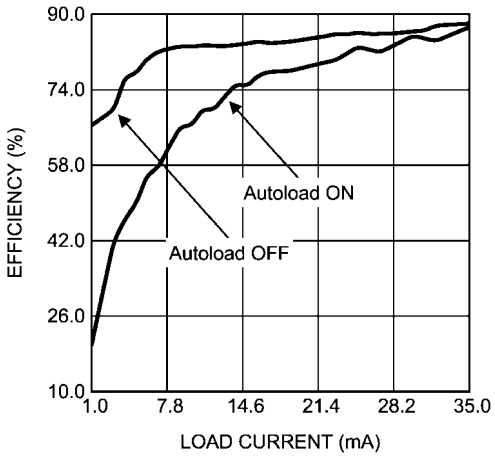


20201114



20201115

Output Voltage vs Load Current



20201116

Efficiency at Low Load vs Autoload

Functionality of RGB LED Outputs (R1-4, G1-4, B1-4)

LP55281 has 4 sets of RGB/color LED outputs. Each set has 3 outputs, which can be controlled individually with a 6-bit PWM control register. The pulsed current level for each LED output is set with a single external resistor R_{RGB} and a 2-bit coarse adjustment bit for each LED output (see tables below).

Rx_IPLS[7:6] / Gx_IPLS[7:6] / Bx_IPLS[7:6]	Sink Current Pulse (I_{MAX} = 100*1.23/R_{RGB}) I_{PLS}
00	0.25*I_{MAX}
01	0.50*I_{MAX}
10	0.75*I_{MAX}
11	1.00*I_{MAX}

Rx_PWM[5:0] / Gx_PWM[5:0] / Bx_PWM[5:0]	Awerage Sink Current	Pulse Ratio, %
000 000	0	0
000 001	1/63*I_{PLS}	1.6
000 010	2/63*I_{PLS}	3.2
...	...	...
111 110	62/63*I_{PLS}	98.4
111 111	63/63*I_{PLS}	100

Each RGB set must be enabled separately by setting EN_RGBx bit to '1'. Note, that the device must be enabled (NSTBY = '1') before the RGB outputs can be activated.

When any of EN_RGBx bits are set to '1' and NSTBY = '1', the RGB driver takes a certain quiescent current from battery even if all PWM control bits are '0'. The quiescent current is dependent on R_{RGB} resistor, and can be calculated from formula I_{R_RGB} = 1.23V/R_{RGB}.

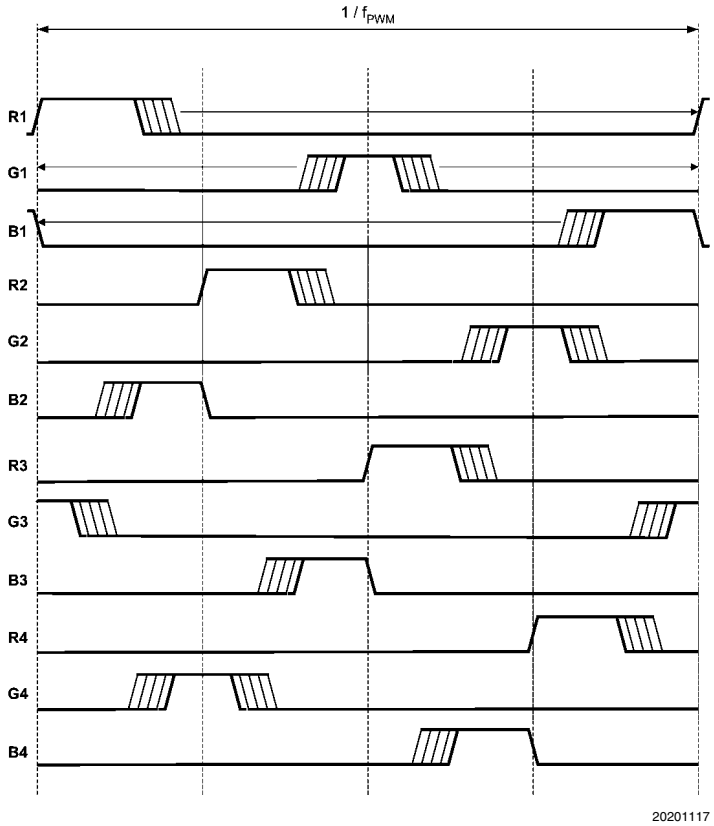
PWM CONTROL TIMING

PWM frequency can be selected from 3 predefined values: 10 kHz, 20 kHz and 40 kHz. The frequency is selected with FPWM1 and FPWM0 bits, see following table:

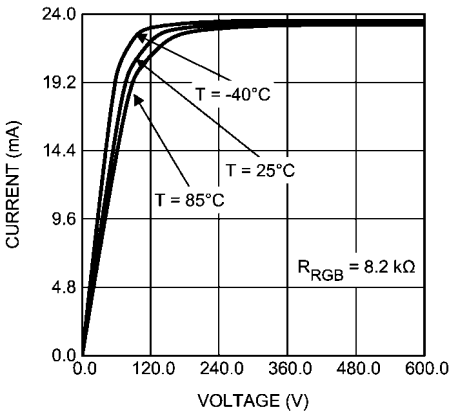
FPWM1	FPWM0	PWM Frequency (f_{PWM})
0	0	9.92 kHz
0	1	19.84 kHz
1	0	39.68 kHz
1	1	39.68 kHz

Each RGB set has equivalent internal PWM timing between R, G and B: R has a fixed start time, G has a fixed midpulse time and B has a fixed pulse end time. PWM start time for each RGB set is different in order to minimize the instantaneous current loading due to the current sink switch on transition. See following timing diagram for details.

Timing Diagram

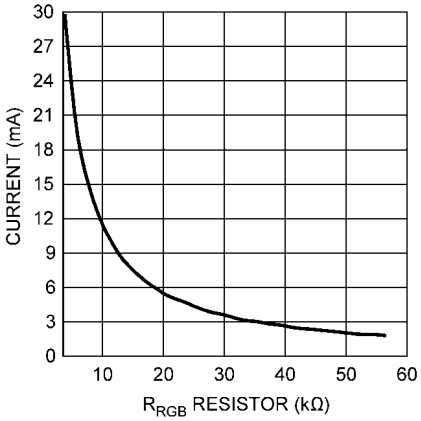


RGB DRIVER TYPICAL PERFORMANCE CHARACTERISTICS



20201126

Output Current vs Pin Voltage (Current Sink Mode)



20201127

Output Current vs R_{RGB} (Current Sink Mode)

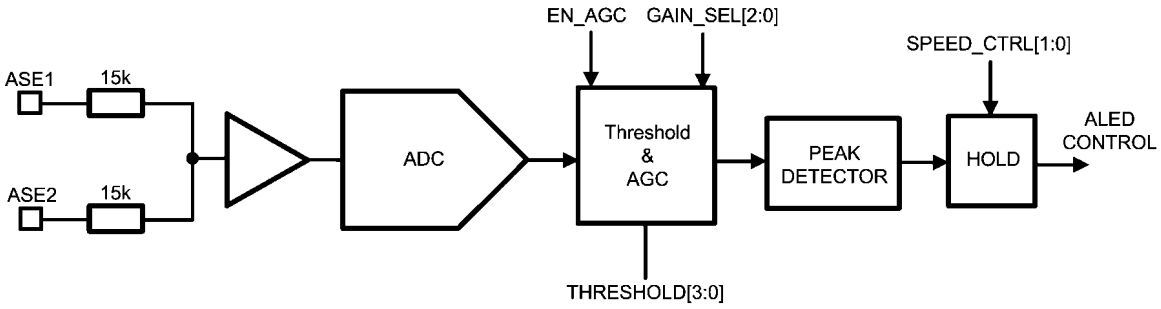
Audio Synchronization

The ALED output can be synchronized to incoming audio with Audio Synchronization feature. Audio Synch synchronizes ALED based on input signal's peak amplitude. Programmable gain and automatic gain control function are also available for adjustment of input signal amplitude to light response. Control of ALED brightness refreshing frequency is done with four different frequency configurations. The digitized input signal has DC component that is removed by a digital dc-remover (-3 dB @ 500 Hz). LP55281 has a 2-channel audio (stereo) input for audio synchronization, as shown in the figure below.

The inputs accept signals in the range of 0V to 1.6V peak-to-peak and these signals are mixed into a single wave so that they can be filtered simultaneously.

LP55281 audio synchronization is mainly realized digitally and it consists following signal path blocks (see figure below)

- Input buffer
- AD converter
- Automatic Gain Control (AGC) and manually programmable gain
- Peak detector



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CONTROL OF AUDIO SYNCHRONIZATION

The following table describes the controls required for audio synchronization. ALED brightness control through serial interface is not available when audio synchronization is enabled.

Audio Synchronization Control (Registers 0Dh and 0Eh)

GAIN_SEL [2:0]	Register 0Dh Bits 7-5	Input signal gain control. Gain has a range from 0 dB to -46 dB. [000] = 0 dB, [001] = -6 dB, [010] = -12 dB, [011] = -18 dB, [100] = -24 dB, [101] = -31 dB, [110] = -37 dB, [111] = -46 dB
DC_FREQ	Register 0Dh Bit 4	Control of the high-pass filter's corner frequency: 0 = 80 Hz 1 = 510 Hz
EN_AGC	Register 0Dh Bits 3	Automatic gain control. Set EN_AGC = 1 to enable automatic control or 0 to disable. When EN_AGC is disabled, the audio input signal gain value is defined by GAIN_SEL.
EN_SYNC	Register 0Dh Bits 2	Audio synchronization enabled. Set EN_SYNC = 1 to enable audio synchronization or 0 to disable.
SPEED_CTRL [1:0]	Register 0Dh Bits 1-0	Control for refreshing frequency. Sets the typical refreshing rate for the ALED output [00] = FASTEST, [01] = 15 Hz, [10] = 7.6 Hz, [11] = 3.8 Hz
THRESHOLD [3:0]	Register 0Eh Bits 3-0	Control for the audio input threshold. Sets the typical threshold for the audio inputs signals. May be needed if there is noise on the audio lines.

Audio Input Threshold Setting (Register 0Eh)

THRESHOLD[3:0]	Threshold Level, mV (typical)
0000	Disabled
0001	0.2
0010	0.4
...	...
1110	2.5
1111	2.7

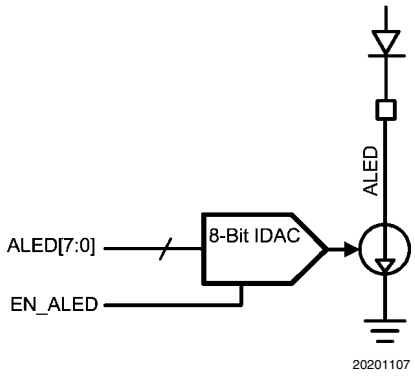
Typical Gain Values vs Audio Input Amplitude

Audio Input Amplitude mV_{P-P}	Gain Value dB
0 to 10	0
0 to 20	-6
0 to 40	-12
1 to 85	-18
3 to 170	-24
5 to 400	-31
10 to 800	-37
20 to 1600	-46

ALED Driver

LP55281 has a single ALED driver. It is a constant current sink with an 8-bit control. ALED driver can be used as a DC current sink or an audio synchronized current sink. Note, that when the audio synchronization function is enabled, the 8-bit current control register has no effect.

ALED driver is enabled when audio synchronization is enabled (EN_SYNC = 1) or when ALED[7:0] control byte has other than 00h value.



ADJUSTMENT OF ALED DRIVER

Adjustment of the ALED driver current (Register 0Ch) is described in table below:

ALED[7:0]	Driver Current, mA (typical)
0000 0000	0
0000 0001	0.06
0000 0010	0.1
...	...
1111 1101	14.8
1111 1110	14.9
1111 1111	15

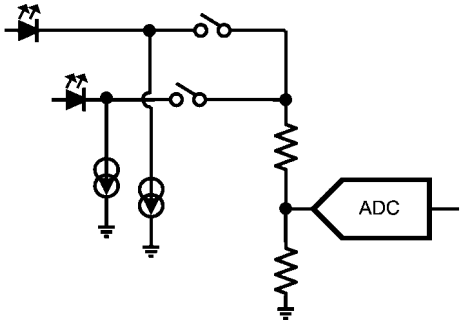
With other than values on the table, the current value can be calculated to be (15.0 mA / 255) * ALED[7:0], where ALED [7:0] is value in decimals.

LED Test Interface

All LED pin voltages and boost output voltage in LP55281 can be measured and value can be read through the SPI/I²C compatible interface. MUX_LED[3:0] bits in the LED test register (address 12h) are used to select one of the LED outputs or boost output for measurement. The selected output is connected to the internal ADC through a 55 kΩ resistor divider. The AD conversion is activated by setting the EN_LTEST bit to '1'. The first conversion is ready after 128 µs from this. The result can be read from the ADC output register (address 13h). The device executes the AD conversions automatically once in every 128 µs period, as long as the EN_LTEST bit is '1'.

User can set the preferred DC current level with the LED driver controls. The RGB drivers' PWM must be set to 100%, or otherwise there can appear random variation on results. Note, that the 55 kΩ resistor divider causes small additional current through the LED under measurement.

ADC result can be converted into a voltage value (of the selected pin) by multiplying the ADC result (in decimals) with **27.345 mV** (value of LSB). The calculated voltage value is the voltage between the selected pin and ground. The internal LDO voltage is used as a reference voltage for the conversion. The accuracy of LDO is ± 3%, which is defining the overall accuracy. The non-linearity and offset figures are both better than 2LSB.



Principle of LED Connection to ADC

LED Multiplexing (Register 12h)

MUX_LED[3:0]	Connection
0000	R1
0001	G1
0010	B1
0011	R2
0100	G2
0101	B2
0110	R3
0111	G3
1000	B3
1001	R4
1010	G4
1011	B4
1100	ALED
1101	-
1110	-
1111	Boost Output

LED TEST PROCEDURE

An example of LED test sequence is presented here. Note, that user can use incremental write sequence on I²C. The test sequence consists of the basic setup and measurement phases for all RGB LEDs and Boost voltage.

Basic setup phase for the device:

1. Give reset to LP55281 (by power on, NRST pin or write any data to register 60h)
2. Set the preferred value for RED1 (write 3Fh, 7Fh, BFh or FFh to register 00h)
3. Set the preferred value for GREEN1 (write 3Fh, 7Fh, BFh or FFh to register 01h)
4. Set the preferred value for BLUE1 (write 3Fh, 7Fh, BFh or FFh to register 02h)
5. Set the preferred value for RED2 (write 3Fh, 7Fh, BFh or FFh to register 03h)
6. Set the preferred value for GREEN2 (write 3Fh, 7Fh, BFh or FFh to register 04h)
7. Set the preferred value for BLUE2 (write 3Fh, 7Fh, BFh or FFh to register 05h)
8. Set the preferred value for RED3 (write 3Fh, 7Fh, BFh or FFh to register 06h)
9. Set the preferred value for GREEN3 (write 3Fh, 7Fh, BFh or FFh to register 07h)
10. Set the preferred value for BLUE3 (write 3Fh, 7Fh, BFh or FFh to register 08h)
11. Set the preferred value for RED4 (write 3Fh, 7Fh, BFh or FFh to register 09h)
12. Set the preferred value for GREEN4 (write 3Fh, 7Fh, BFh or FFh to register 0Ah)
13. Set the preferred value for BLUE4 (write 3Fh, 7Fh, BFh or FFh to register 0Bh)
14. Set the preferred value for ALED (write 01h - FFh to register 0Ch)
15. Dummy write: 00h to register 0Dh (Only if the incremental write sequence is used)
16. Dummy write: 00h to register 0Eh (Only if the incremental write sequence is used)
17. Set preferred boost voltage (write 00h - FFh to register 0Fh)
18. Set preferred boost frequency (write 00h - 07h to register 10h, PWM frequency can be anything)
19. Enable boost and RGB drivers (write CFh to register 11h)
20. Wait 20 ms for the device and boost startup

Measurement phase:

1. Enable LED test and select output (write 1xh to register 12h)
2. Wait for 128 µs
3. Read ADC output (read register 13h)
4. Go to step 1 of measurement phase and define next output to be measured as many times as needed
5. Disable LED test (write 00h to register 12h) or give reset to the device (see step 1 in basic setup phase)

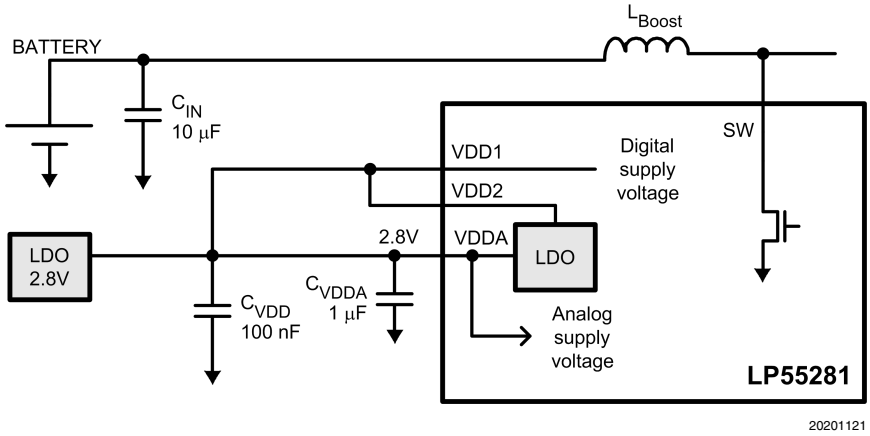
LED TEST TIME ESTIMATION

Assuming the maximum clock frequencies used in SPI or I²C compatible interfaces, the following table predicts the overall test sequence time for the test procedure shown above. This estimation gives the shortest time possible. Incremental write is assumed with I²C. Reset and LED test disable are not included.

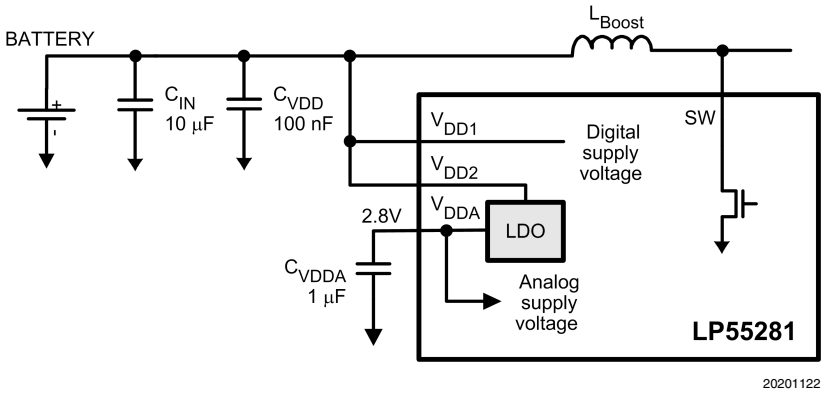
Test Phase	Time (ms)	
	I²C	**SPI**
Setup	0.528	0.024
Boost startup	20	20
14 measurements	4.137	1.831
Total Time	**24.7**	**21.9**

7V Shielding

To shield LP55281 from high input voltages (6 to 7.2V), the use of external 2.8V LDO is required. This 2.8V voltage protects internally the device against high voltage condition. The recommended connection is shown in the picture below. Internally both logic and analog circuitry works at 2.8V supply voltage. Both supply voltage pins should have separate filtering capacitors. Note that it is recommended to pull down the external LDO voltage when it is disabled in order to minimize the leakage current of the LED outputs.



In cases where high voltage is not an issue, the alternative connection is shown below.



Control Interface

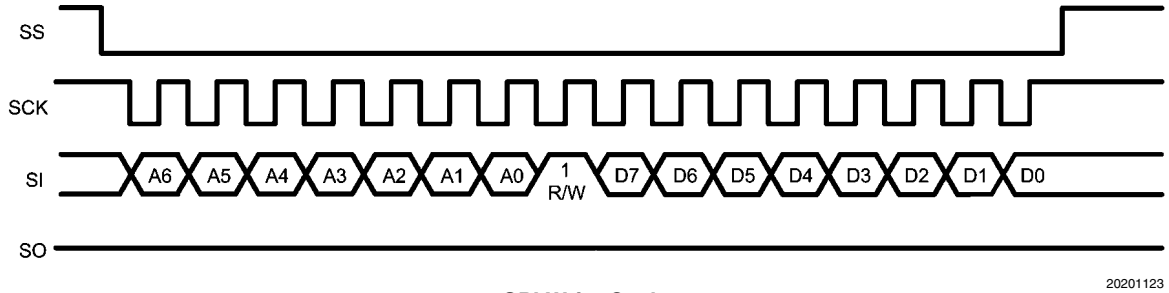
The LP55281 supports two different interface modes:

- SPI interface (4 wire, serial)
- I²C compatible (2 wire, serial)

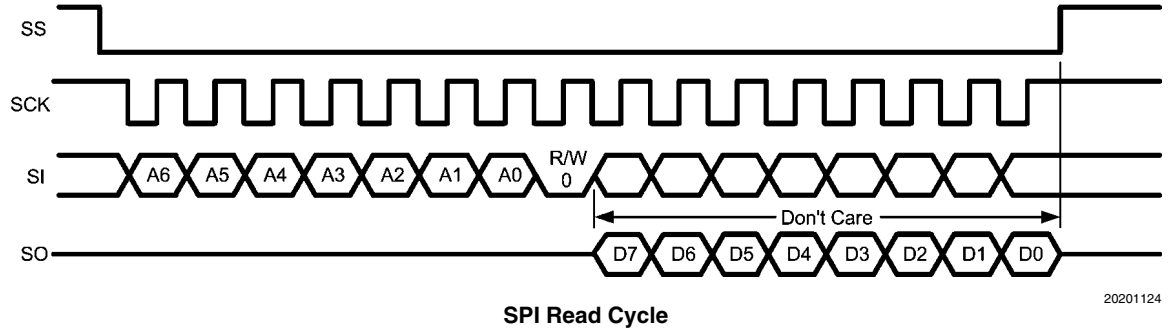
User can define the serial interface by IF_SEL pin. If IF_SEL = 0, I²C mode is selected.

SPI INTERFACE

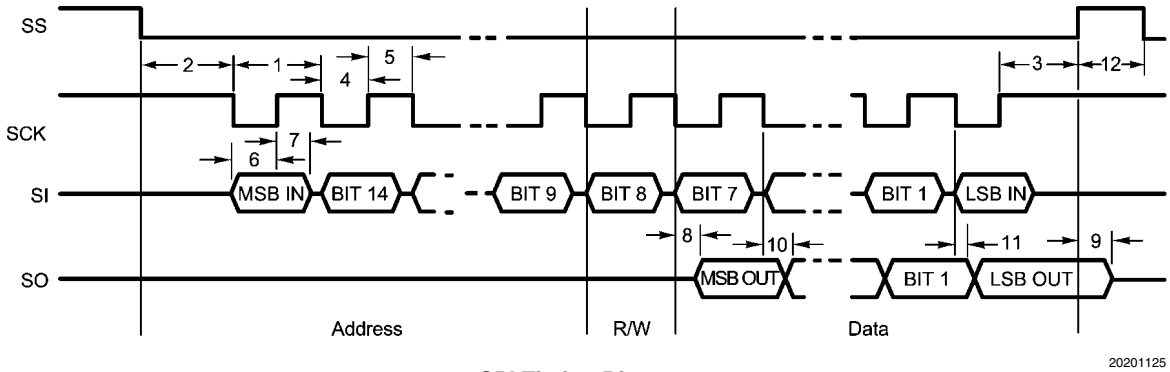
LP55281 is compatible with SPI serial bus specification and it operates as a slave. The transmission consists of 16-bit Write and Read Cycles. One cycle consists of a 7 Address bits, 1 Read/Write (RW) bit and 8 Data bits. RW bit high state defines a Write Cycle and low a Read Cycle. SO output is normally in high-impedance state and it is active only when Data is sent out during a Read Cycle. A pull-up resistor may be needed in SO line if a floating logic signal can cause unintended current consumption in the input circuits where SO is connected. The Address and Data are transmitted MSB first. The Slave Select signal (SS) must be low during the Cycle transmission. SS resets the interface when high and it has to be taken high between successive Cycles. Data is clocked in on the rising edge of the clock signal (SCK), while data is clocked out on the falling edge of SCK.



SPI Write Cycle



SPI Read Cycle



SPI Timing Diagram

SPI Timing Parameters

$V_{DD} = V_{DDIO} = 2.8V$

Symbol	Parameter	Limit		Units
		Min	Max	
1	Cycle Time	70		ns
2	Enable Lead Time	35		ns
3	Enable Lag Time	35		ns
4	Clock Low Time	35		ns
5	Clock High Time	35		ns
6	Data Setup Time	20		ns
7	Data Hold Time	0		ns
8	Data Acces Time		20	ns
9	Disble Time		10	ns
10	Data Valid		20	ns
11	Data Hold Time	0		ns

Note: Data guaranteed by design

I²C COMPATIBLE SERIAL BUS INTERFACE

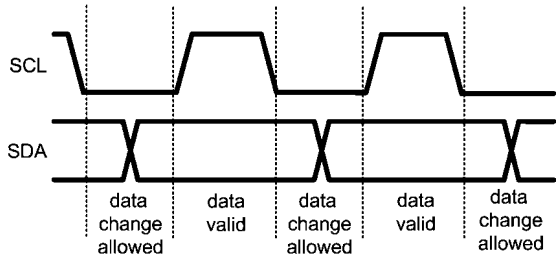
Interface Bus Overview

The I²C compatible synchronous serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the IC's connected to the bus. The two interface lines are the Serial Data Line (SDA) and the Serial Clock Line (SCL). These lines should be connected to a positive supply, via a pull-up resistor and remain HIGH even when the bus is idle.

For every device on the bus is assigned a unique address and it acts as a Master or a Slave, depending on whether it generates or receives the serial clock (SCL). When LP55281 is connected in parallel with other I²C compatible devices, the LP55281 supply voltages V_{DD1}, V_{DD2} and V_{DDIO} must be active. Supplies are required to make sure that the LP55281 does not disturb the SDA and SCL lines.

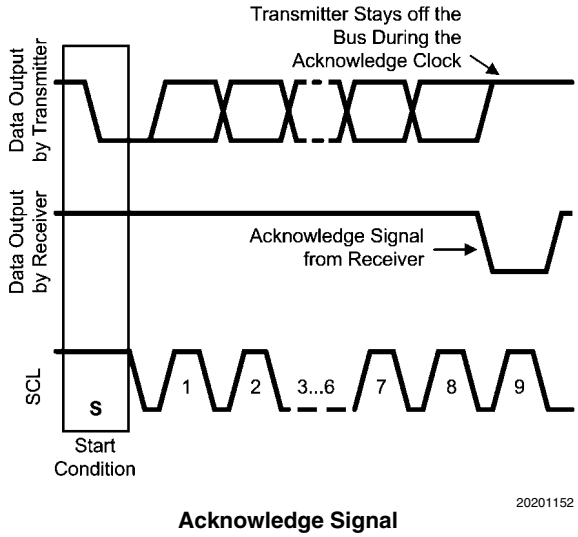
Data Transactions

One data bit is transferred during each clock pulse. Data is sampled during the high state of the serial clock (SCL). Consequently, throughout the clock's high period, the data should remain stable. Any changes on the SDA line during the high states of the SCL and in the middle of the transaction, aborts the current transaction. New data should be sent during the low SCL state. This protocol permits a single data line to transfer both command/control information and data using the synchronous serial clock.



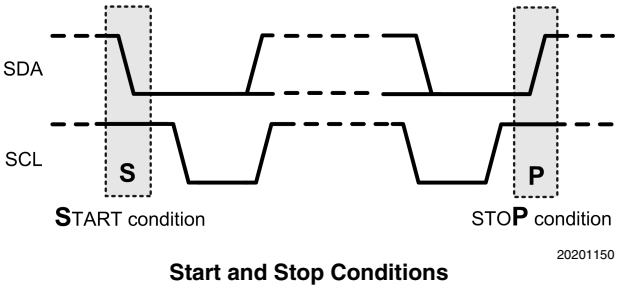
Data Validity

Each data transaction is composed of a Start Condition, a number of byte transfers (set by the software) and a Stop Condition to terminate the transaction. Every byte written to the SDA bus must be 8 bits long and is transferred with the most significant bit first. After each byte, an Acknowledge signal must follow. The following sections provide further details of this process.



Acknowledge Signal

The Master device on the bus always generates the Start and Stop Conditions (control codes). After a Start Condition is generated, the bus is considered busy and it retains this status until a certain time after a Stop Condition is generated. A high-to-low transition of the data line (SDA), while the clock (SCL) is high, indicates a Start Condition. A low-to-high transition of the SDA line, while the SCL is high, indicates a Stop Condition



Start and Stop Conditions

In addition to the first Start Condition, a repeated Start Condition can be generated in the middle of a transaction. This allows another device to be accessed or a register read cycle.

Acknowledge Cycle

The Acknowledge Cycle consists of two signals: the acknowledge clock pulse the master sends with each byte transferred, and the acknowledge signal sent by the receiving device.

The master generates the acknowledge clock pulse on the ninth clock pulse of the byte transfer. The transmitter releases the SDA line (permits it to go high) to allow the receiver to send the acknowledge signal. The receiver must pull down the SDA line during the acknowledge clock pulse and ensure that SDA remains low during the high period of the clock pulse, thus signaling the correct reception of the last data byte and its readiness to receive the next byte.

"ACKNOWLEDGE AFTER EVERY BYTE" Rule

The Master generates an acknowledge clock pulse after each byte transfer. The receiver sends an acknowledge signal after every byte received.

There is one exception to the "acknowledge after every byte" rule. When the master is the receiver, it must indicate to the transmitter an end of data by not-acknowledging ("negative acknowledge") the last byte clocked out of the slave. This

"negative acknowledge" still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

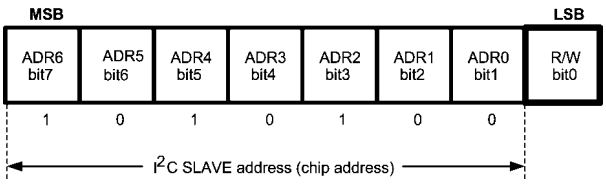
Addressing Transfer Formats

Each device on the bus has a unique slave address. The LP55281 operates as a slave device with 7-bit address. LP55281 I²C address is pin selectable from two different choices. **The LP55281 address is 4Ch (SI/A0 = 0) or 4Dh (SI/A0 = 1) as selected with SI/A0 pin.** If eighth bit is used for programming, the 8th bit is 1 for read and 0 for write.

Before any data is transmitted, the master transmits the address of the slave being addressed. The slave device should send an acknowledge signal on the SDA line, once it recognizes its address.

The slave address is the first seven bits after a Start Condition. The direction of the data transfer (R/W) depends on the bit sent after the slave address (the eighth bit).

When the slave address is sent, each device in the system compares this slave address with its own. If there is a match, the device considers itself addressed and sends an acknowledge signal. Depending upon the state of the R/W bit (1 for read, 0 for write), the device acts as a transmitter or a receiver.



I²C Device Address

Control Register Write Cycle

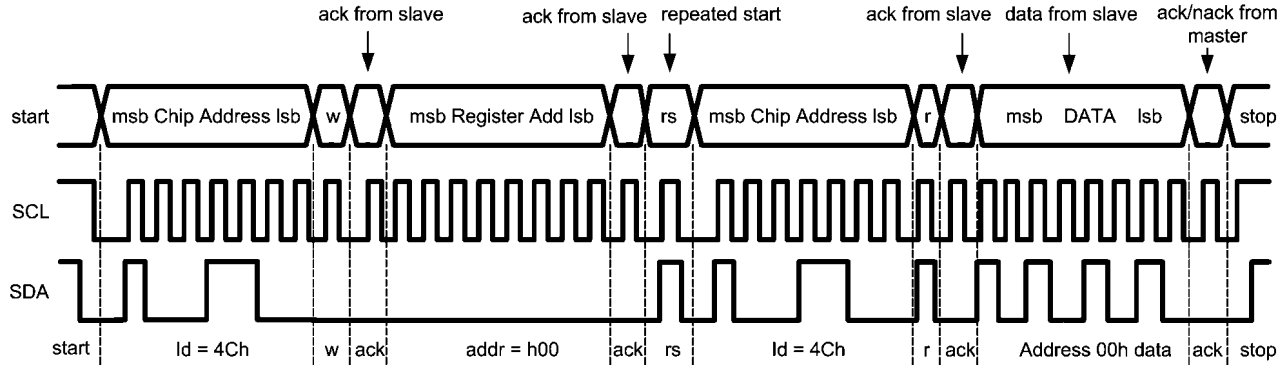
- Master device generates start condition
- Master device sends slave address (7 bits) and the data direction bit (r/w=0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master sends data byte to be written to the addressed register.
- Slave sends acknowledge signal.
- If master will send further data bytes, the control register address will be incremented by one after acknowledge signal
- Write cycle ends when the master creates stop condition.

Control Register Read Cycle

- Master device generates a start condition.
- Master device sends slave address (7 bits) and the data direction bit (r/w=0).
- Slave device sends acknowledge signal if the slave address is correct.
- Master sends control register address (8 bits).
- Slave sends acknowledge signal.
- Master device generates repeated start condition.
- Master sends the slave address (7 bits) and the data direction bit (r/w=1).
- Slave sends acknowledge signal if the slave address is correct.
- Slave sends data byte from addressed register.
- If the master device sends acknowledge signal, the control register address will be incremented by one. Slave device sends data byte from addressed register.
- Read cycle ends when the master does not generate acknowledge signal after data byte and generates stop condition.

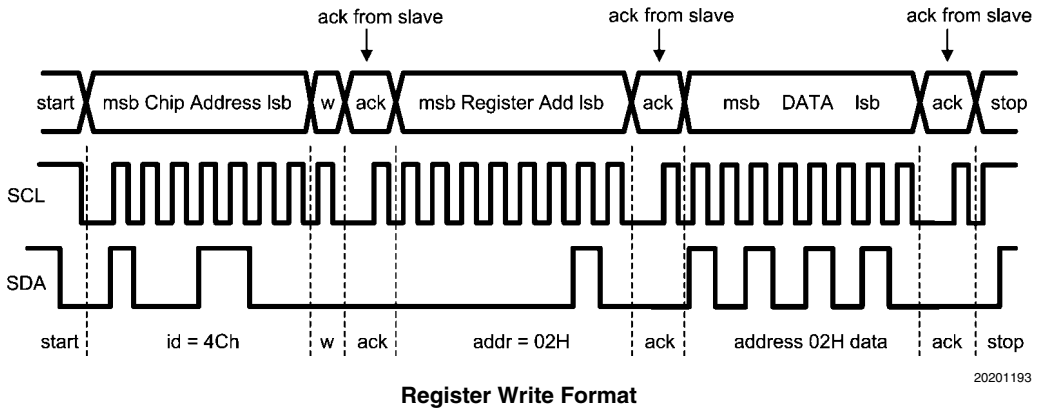
	Address Mode
Data Read	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Address>[Ack] <Repeated Start Condition> <Slave Address><r/w = 1>[Ack] [Register Data]<Ack or NAck> ...additional reads from subsequent register address possible <Stop Condition>
Data Write	<Start Condition> <Slave Address><r/w = 0>[Ack] <Register Address>[Ack] <Register Data>[Ack] ...additional writes to subsequent register address possible <Stop Condition>

< > Data from master, [ ] data from slave



Register Read Format

When a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in the Read Cycle waveform.

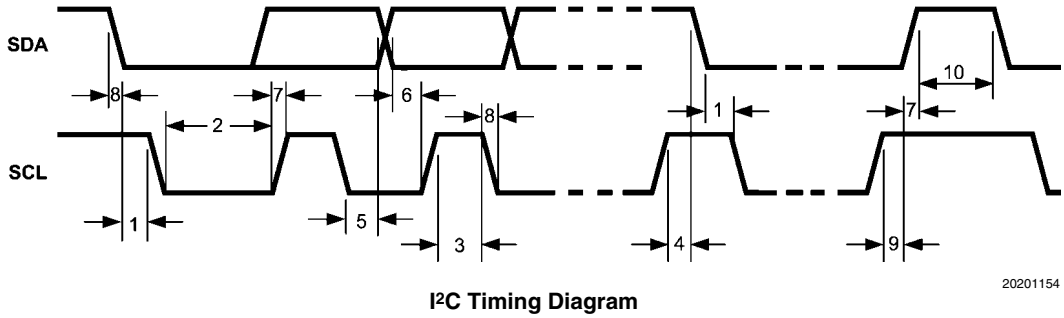


Register Write Format

- w = write (SDA = 0)
- r = read (SDA = 1)
- ack = acknowledge (SDA pulled down by either master or slave)
- rs = repeated start
- id = 7-bit device address

I²C Timing Parameters

$V_{DD1,2}$ = 3.0V to 4.5V, V_{DDIO} = 1.65V to $V_{DD1,2}$



I²C Timing Diagram

Symbol	Parameter	Limit		Units
		Min	Max	
1	Hold Time (repeated) START condition	0.6		µs
2	Clock Low Time	1.3		µs
3	Clock High Time	600		ns
4	Setup Time for a Repeated START Condition	600		ns
5	Data Hold Time	50		ns
6	Data Setup TIme	100		ns
7	Rise Time of SDA and SCL	$20 + 0.1C_b$	300	ns
8	Fall Time of SDA and SCL	$15 + 0.1C_b$	300	ns
9	Set-up Time for STOP condition	600		ns
10	Bus Free Time between a STOP and a START Condtion	1.3		µs
C_b	Capacitive Load for Each Bus Line	10	200	pF

Note: Data guaranteed by design

Recommended External Components

OUTPUT CAPACITOR, C_{OUT}:

The output capacitor C_{OUT} directly affects the magnitude of the output ripple voltage. In general, the higher the value of C_{OUT}, the lower the output ripple magnitude. Multilayer ceramic capacitors with low ESR are the best choice. At the lighter loads, the low ESR ceramics offer a much lower V_{OUT} ripple than the higher ESR tantalums of the same value. At the higher loads, the ceramics offer a slightly lower V_{OUT} ripple magnitude than the tantalums of the same value. However, the dv/dt of the V_{OUT} ripple with the ceramics is much lower than the tantalums under all load conditions. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

Some ceramic capacitors, espesically those in small packages, exhibit a strong capacitance reduction with the increased applied voltage. The capacitance value can fall to below half of the nominal capacitance. Too low output capacitance will increase the noise and it can make the boost converter unstable.

INPUT CAPACITOR, C_{IN}:

The input capacitor C_{IN} directly affects the magnitude of the input ripple voltage and to a lesser degree the V_{OUT} ripple. A higher value C_{IN} will give a lower V_{IN} ripple. Capacitor voltage rating must be sufficient, 10V or greater is recommended.

OUTPUT DIODE, D_1:

A Schottky diode should be used for the output diode. To maintain high efficiency the average current rating of the schottky diode shoulde be larger than the peak inductor current (1A). Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency in portable applications. Choose a reverse breakdown of the schottky diode larger than the output voltage. Do not use ordinary rectifier diodes, since slow switching speeds and long recovery times cause the efficiency and the load regulation to suffer.

INDUCTOR, L:

The LP55281's high switching frequency enables the use of the small surface mount inductor. A 4.7 µH shielded inductor is suggested for 2 MHz operation, 10 µH should be used at 1 MHz. The inductor should have a saturation current rating higher than the peak current it will experience during circuit operation **(~1A)**. Less than 300 mΩ ESR is suggested for high efficiency. Open core inductors cause flux linkage with circuit components and interfere with the normal operation of the circuit. This should be avoided. For high efficiency, choose an inductor with a high frequency core material such as ferrite to reduce the core losses. To minimize radiated noise, use a toroid, pot core or shielded core inductor. The inductor should be connected to the SW pin as close to the IC as possible. Recommended inductors are LPS3015 and LPS4012 from Coilcraft and VLF4012 from TDK.

LIST OF RECOMMENDED EXTERNAL COMPONENTS

Symbol	Symbol explanation	Value	Unit	Type
$C_{V_{DD1}}$	C between V_{DD1} and GND	100	nF	Ceramic, X7R/X5R
$C_{V_{DD2}}$	C between V_{DD2} and GND	100	nF	Ceramic, X7R/X5R
$C_{V_{DDIO}}$	C between V_{DDIO} and GND	100	nF	Ceramic, X7R/X5R
$C_{V_{DDA}}$	C between V_{DDA} and GND	1	µF	Ceramic, X7R/X5R
C_{OUT}	C between FB and GND	10	µF	Ceramic, X7R/X5R
C_{IN}	C between battery voltage and GND	10	µF	Ceramic, X7R/X5R
L_{BOOST}	L between SW and VBAT at 2 MHz	4.7	µH	Shielded, low ESR, I_{SAT} 1A
C_{VREF}	C between VREF and GND	100	nF	Ceramic, X7R
$C_{V_{DDIO}}$	C between V_{DDIO} and GND	100	nF	Ceramic, X7R
R_{RGB}	R between IRGB and GND	8.2	kΩ	±1%
R_{RT}	R between IRT and GND	82	kΩ	±1%
D_1	Rectifying Diode (V_f @ maxload)	0.3	V	Schottky diode
C_{ASE}	C between Audio input and ASEx	100	nF	Ceramic, X7R/X5R
LEDs		User defined		

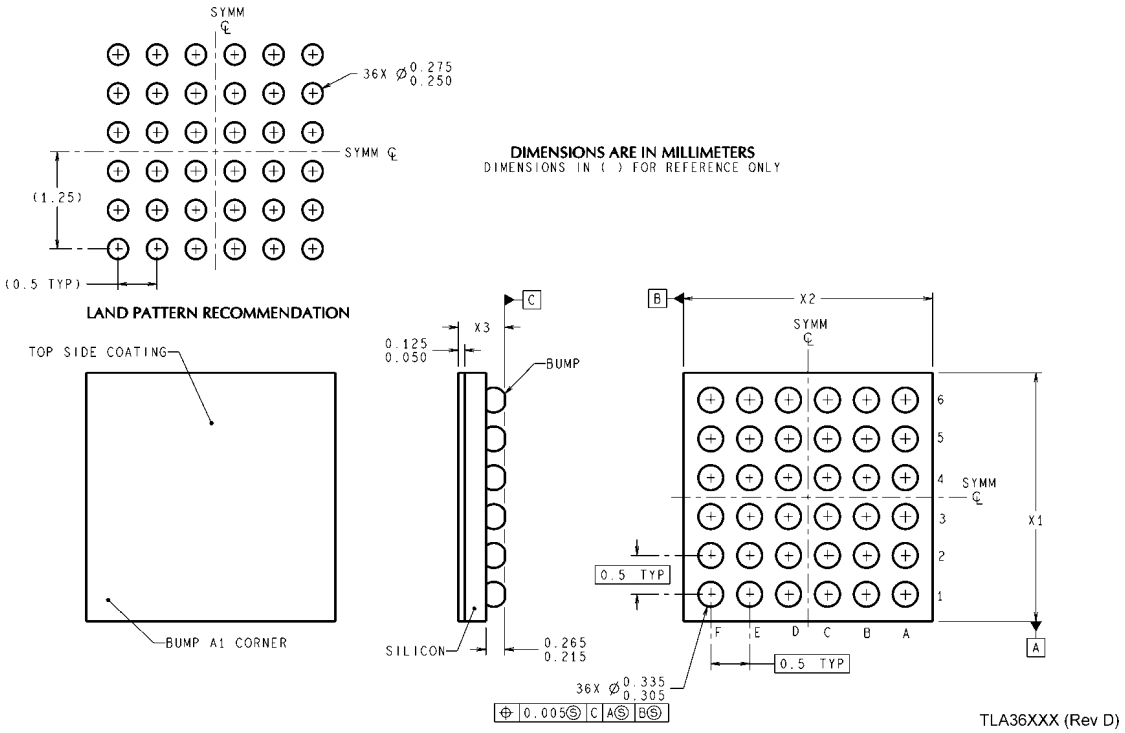
LP55281 Registers

Following table summarizes the registers and their default values

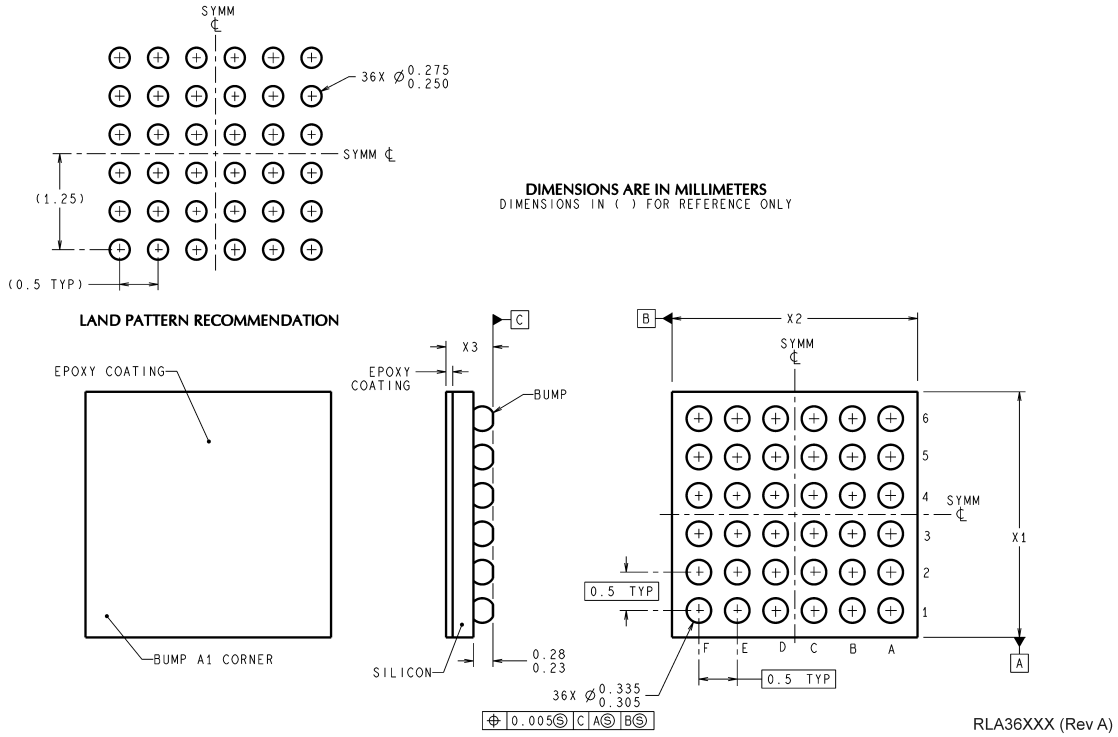
Address	Register	D7	D6	D5	D4	D3	D2	D1	D0
00h	RED1	R1 - IPLS[7:6]		R1_PWM[5:0]					
		0	0	0	0	0	0	0	0
01h	GREEN1	G1 - IPLS[7:6]		G1_PWM[5:0]					
		0	0	0	0	0	0	0	0
02h	BLUE1	B1 - IPLS[7:6]		B1_PWM[5:0]					
		0	0	0	0	0	0	0	0
03h	RED2	R2 - IPLS[7:6]		R2_PWM[5:0]					
		0	0	0	0	0	0	0	0
04h	GREEN2	G2 - IPLS[7:6]		G2_PWM[5:0]					
		0	0	0	0	0	0	0	0
05h	BLUE2	B2 - IPLS[7:6]		B2_PWM[5:0]					
		0	0	0	0	0	0	0	0
06h	RED3	R3 - IPLS[7:6]		R3_PWM[5:0]					
		0	0	0	0	0	0	0	0
07h	GREEN3	G3 - IPLS[7:6]		G3_PWM[5:0]					
		0	0	0	0	0	0	0	0
08h	BLUE3	B3 - IPLS[7:6]		B3_PWM[5:0]					
		0	0	0	0	0	0	0	0
09h	RED4	R4 - IPLS[7:6]		R4_PWM[5:0]					
		0	0	0	0	0	0	0	0
0Ah	GREEN4	G4 - IPLS[7:6]		G4_PWM[5:0]					
		0	0	0	0	0	0	0	0
0Bh	BLUE4	B4 - IPLS[7:6]		B4_PWM[5:0]					
		0	0	0	0	0	0	0	0
0Ch	ALED	ALED[7:0]							
		0	0	0	0	0	0	0	0
0Dh	Audio Sync CTRL1	GAIN_SEL[2:0]			DC_FREQ	EN_AGC	EN_SYNC	SPEED_CTRL[1:0]	
		0	0	0	0	0	0	1	1
0Eh	Audio Sync CTRL2					THRESHOLD[3:0]			
						0	0	0	0
0Fh	Boost Output	Boost[7:0]							
		0	0	1	1	1	1	1	1
10h	Frequency Selections			FPWM1	FPWM0		FRQ_SEL[2:0]		
				0	0		1	1	1
11h	Enables	NSTBY	EN_BOOST	EN_AUTOLOAD		EN_RGB4	EN_RGB3	EN_RGB2	EN_RGB1
		0	0	0		0	0	0	0
12h	LED Test				EN_LTEST	MUX_LED[3:0]			
					0	0	0	0	0
13h	ADC Output	DATA[7:0]							
		0	0	0	0	0	0	0	0
		r/o	r/o	r/o	r/o	r/o	r/o	r/o	r/o
60h	Reset	Writing any data to Reset Register resets LP55281							

Note: r/o = read-only

Physical Dimensions inches (millimeters) unless otherwise noted



NS Package Number TLA36AAA
36-bump Micro SMD package, 3 x 3 x 0.6 mm, 0.5 mm pitch



NS Package Number RLA36AAA
36-bump Micro SMDxt package, 3 x 3 x 0.65 mm, 0.5 mm pitch

See National Semiconductor Application Note AN–1112 Micro SMD Wafer Level Chip Scale Package for PCB design and assembly instructions for Micro SMD. For Micro SMDxt see National Semiconductor Application Note AN–1412 Micro SMDxt Wafer Level Chip Scale Package

Notes

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