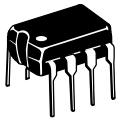
CAT93C46R

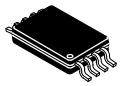
1 kb Microwire Serial EEPROM

ON Semiconductor®

http://onsemi.com

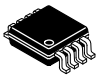


PDIP−8
L SUFFIX
CASE 646AA



TSSOP−8
Y SUFFIX
CASE 948AL

SOIC−8
V SUFFIX
CASE 751BD



SOIC−8
X SUFFIX
CASE 751BE

TDFN−8
VP2 SUFFIX
CASE 511AK

Description

The CAT93C46R is a 1 kb CMOS Serial EEPROM device which is organized as either 64 registers of 16 bits or 128 registers of 8 bits, as determined by the state of the ORG pin. The CAT93C46R features sequential read and self−timed internal write with auto−clear. On−chip Power−On Reset circuitry protects the internal logic against powering up in the wrong state.

In contrast to the CAT93C46, the CAT93C46R features an internal instruction clock counter which provides improved noise immunity for Write/Erase commands.

Features

- High Speed Operation: 4 MHz @ 5 V, 2 MHz @ 1.8 V
- 1.8 V to 5.5 V Supply Voltage Range
- Selectable x8 or x16 Memory Organization
- Sequential Read
- Software Write Protection
- Power−up Inadvertant Write Protection
- Low Power CMOS Technology
- 1,000,000 Program/Erase Cycles
- 100 Year Data Retention
- Industrial Temperature Range
- 8−pin PDIP, SOIC, TSSOP and 8−pad TDFN Packages
- This Device is Pb−Free, Halogen Free/BFR Free and RoHS Compliant*

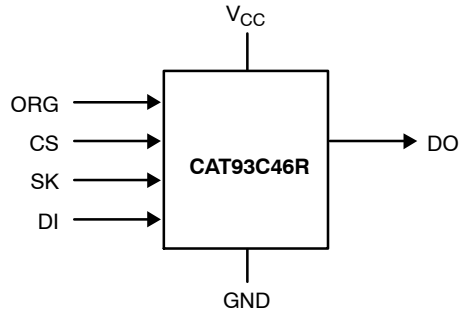
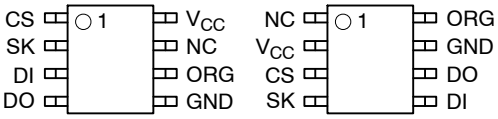


Figure 1. Functional Symbol

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PIN CONFIGURATIONS



PDIP (L), SOIC (V, X), TSSOP (Y), TDFN (VP2)

SOIC (W)

(Top Views)

PIN FUNCTION

Pin Name	Function
CS	Chip Select
SK	Clock Input
DI	Serial Data Input
DO	Serial Data Output
V_{CC}	Power Supply
GND	Ground
ORG	Memory Organization
NC	No Connection

Note: When the ORG pin is connected to V_{CC}, the x16 organization is selected. When it is connected to ground, the x8 pin is selected. If the ORG pin is left unconnected, then an internal pull−up device will select the x16 organization.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 13 of this data sheet.

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Units
Storage Temperature	−65 to +150	°C
Voltage on Any Pin with Respect to Ground (Note 1)	−0.5 to +6.5	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. The DC input voltage on any pin should not be lower than −0.5 V or higher than V_{CC} + 0.5 V. During transitions, the voltage on any pin may undershoot to no less than −1.5 V or overshoot to no more than V_{CC} + 1.5 V, for periods of less than 20 ns.

Table 2. RELIABILITY CHARACTERISTICS (Note 2)

Symbol	Parameter	Min	Units
N_{END} (Note 3)	Endurance	1,000,000	Program / Erase Cycles
T_{DR}	Data Retention	100	Years

2. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.
3. Block Mode, V_{CC} = 5 V, T_A = 25°C

Table 3. D.C. OPERATING CHARACTERISTICS (V_{CC} = +1.8 V to +5.5 V, unless otherwise specified.)

Symbol	Parameter	Test Conditions	Min	Max	Units
I_{CC1}	Power Supply Current (Write)	f_{SK} = 1 MHz V_{CC} = 5.0 V		1	mA
I_{CC2}	Power Supply Current (Read)	f_{SK} = 1 MHz V_{CC} = 5.0 V		500	μA
I_{SB1}	Power Supply Current (Standby) (x8 Mode)	CS = 0 V ORG = GND		10	μA
I_{SB2}	Power Supply Current (Standby) (x16 Mode)	CS = 0 V ORG = Float or V_{CC}		10	μA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}		2	μA
I_{LO}	Output Leakage Current (Including ORG pin)	V_{OUT} = 0 V to V_{CC}, CS = 0 V		2	μA
V_{IL1}	Input Low Voltage	4.5 V ≤ V_{CC} < 5.5 V	−0.1	0.8	V
V_{IH1}	Input High Voltage	4.5 V ≤ V_{CC} < 5.5 V	2	V_{CC} + 1	V
V_{IL2}	Input Low Voltage	1.8 V ≤ V_{CC} < 4.5 V	0	V_{CC} x 0.2	V
V_{IH2}	Input High Voltage	1.8 V ≤ V_{CC} < 4.5 V	V_{CC} x 0.7	V_{CC} + 1	V
V_{OL1}	Output Low Voltage	4.5 V ≤ V_{CC} < 5.5 V I_{OL} = 2.1 mA		0.4	V
V_{OH1}	Output High Voltage	4.5 V ≤ V_{CC} < 5.5 V I_{OH} = −400 μA	2.4		V
V_{OL2}	Output Low Voltage	1.8 V ≤ V_{CC} < 4.5 V I_{OL} = 1 mA		0.2	V
V_{OH2}	Output High Voltage	1.8 V ≤ V_{CC} < 4.5 V I_{OH} = −100 μA	V_{CC} − 0.2		V

Table 4. PIN CAPACITANCE

Symbol	Test	Conditions	Min	Typ	Max	Units
C_{OUT} (Note 4)	Output Capacitance (DO)	V_{OUT} = 0 V			5	pF
C_{IN} (Note 4)	Input Capacitance (CS, SK, DI, ORG)	V_{IN} = 0 V			5	pF

4. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

Table 5. A.C. CHARACTERISTICS (Note 5)

Symbol	Parameter	V_{CC} = 1.8 V − 5.5 V		V_{CC} = 4.5 V − 5.5 V		Units
		Min	Max	Min	Max	
t_{CSS}	CS Setup Time	50		50		ns
t_{CSH}	CS Hold Time	0		0		ns
t_{DIS}	DI Setup Time	100		50		ns
t_{DIH}	DI Hold Time	100		50		ns
t_{PD1}	Output Delay to 1		0.25		0.1	μs
t_{PD0}	Output Delay to 0		0.25		0.1	μs
t_{HZ} (Note 6)	Output Delay to High−Z		100		100	ns
t_{EW}	Program/Erase Pulse Width		5		5	ms
t_{CSMIN}	Minimum CS Low Time	0.25		0.1		μs
t_{SKHI}	Minimum SK High Time	0.25		0.1		μs
t_{SKLOW}	Minimum SK Low Time	0.25		0.1		μs
t_{SV}	Output Delay to Status Valid		0.25		0.1	μs
SK_{MAX}	Maximum Clock Frequency	DC	2	DC	4	MHz

5. Test conditions according to “A.C. Test Conditions” table.
6. These parameters are tested initially and after a design or process change that affects the parameter according to appropriate AEC−Q100 and JEDEC test methods.

Table 6. POWER−UP TIMING (Notes 4 and 7)

Symbol	Parameter	Max	Units
t_{PUR}	Power−up to Read Operation	1	ms
t_{PUW}	Power−up to Write Operation	1	ms

7. t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 7. A.C. TEST CONDITIONS

Input Rise and Fall Times	≤ 50 ns	
Input Pulse Voltages	0.4 V to 2.4 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Timing Reference Voltages	0.8 V, 2.0 V	4.5 V ≤ V_{CC} ≤ 5.5 V
Input Pulse Voltages	0.2 V_{CC} to 0.7 V_{CC}	1.8 V ≤ V_{CC} ≤ 4.5 V
Timing Reference Voltages	0.5 V_{CC}	1.8 V ≤ V_{CC} ≤ 4.5 V
Output Load	Current Source I_{OLmax}/I_{OHmax}; C_L = 100 pF	

Table 8. INSTRUCTION SET

Instruction	Start Bit	Opcode	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A6–A0	A5–A0			Read Address AN–A0
ERASE	1	11	A6–A0	A5–A0			Clear Address AN–A0
WRITE	1	01	A6–A0	A5–A0	D7–D0	D15–D0	Write Address AN–A0
EWEN	1	00	11XXXXX	11XXXX			Write Enable
EWDS	1	00	00XXXXX	00XXXX			Write Disable
ERAL	1	00	10XXXXX	10XXXX			Clear All Addresses
WRAL	1	00	01XXXXX	01XXXX	D7–D0	D15–D0	Write All Addresses

Device Operation

The CAT93C46R is a 1024−bit nonvolatile memory intended for use with industry standard microprocessors. The CAT93C46R can be organized as either registers of 16 bits or 8 bits. When organized as X16, seven 9−bit instructions control the reading, writing and erase operations of the device. When organized as X8, seven 10−bit instructions control the reading, writing and erase operations of the device. The CAT93C46R operates on a single power supply and will generate on chip the high voltage required during any write operation.

Instructions, addresses, and write data are clocked into the DI pin on the rising edge of the clock (SK). The DO pin is normally in a high impedance state except when reading data from the device, or when checking the ready/busy status after a write operation.

The ready/busy status can be determined after the start of a write operation by selecting the device (CS high) and polling the DO pin; DO low indicates that the write operation is not completed, while DO high indicates that the device is ready for the next instruction. If necessary, the DO pin may be placed back into a high impedance state during chip select by shifting a dummy “1” into the DI pin. The DO pin will enter the high impedance state on the rising edge of the clock (SK). Placing the DO pin into the high impedance state is recommended in applications where the DI pin and the DO pin are to be tied together to form a common DI/O pin. The Ready/Busy flag can be disabled only in Ready state; no change is allowed in Busy state.

The format for all instructions sent to the device is a logical “1” start bit, a 2−bit (or 4−bit) opcode, 6−bit address (an additional bit when organized X8) and for write operations a 16−bit data field (8−bit for X8 organization).

Read

Upon receiving a READ command and an address (clocked into the DI pin), the DO pin of the CAT93C46R will come out of the high impedance state and, after sending an initial dummy zero bit, will begin shifting out the data addressed (MSB first). The output data bits will toggle on the rising edge of the SK clock and are stable after the specified time delay (t_{PD0} or t_{PD1}).

Sequential Read

After the 1st data word has been shifted out and CS remains asserted with the SK clock continuing to toggle, the CAT93C46R will automatically increment to the next address and shift out the next data word. As long as CS is continuously asserted and SK continues to toggle, the device will keep incrementing to the next address automatically until it reaches the end of the address space, then loops back to address 0. In the sequential Read mode, only the initial data word is preceeded by a dummy zero bit; all subsequent data words will follow without a dummy zero bit.

Erase/Write Enable and Disable

The CAT93C46R powers up in the write disable state. Any writing after power−up or after an EWDS (write disable) instruction must first be preceded by the EWEN (write enable) instruction. Once the write instruction is enabled, it will remain enabled until power to the device is removed, or the EWDS instruction is sent. The EWDS instruction can be used to disable all CAT93C46R write and erase instructions, and will prevent any accidental writing or clearing of the device. Data can be read normally from the device regardless of the write enable/disable status.

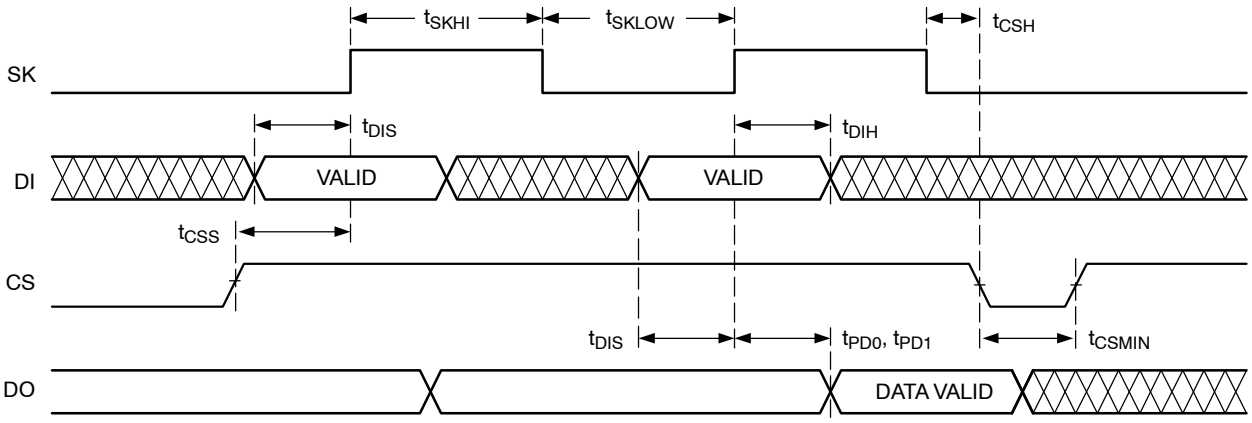


Figure 2. Synchronous Data Timing

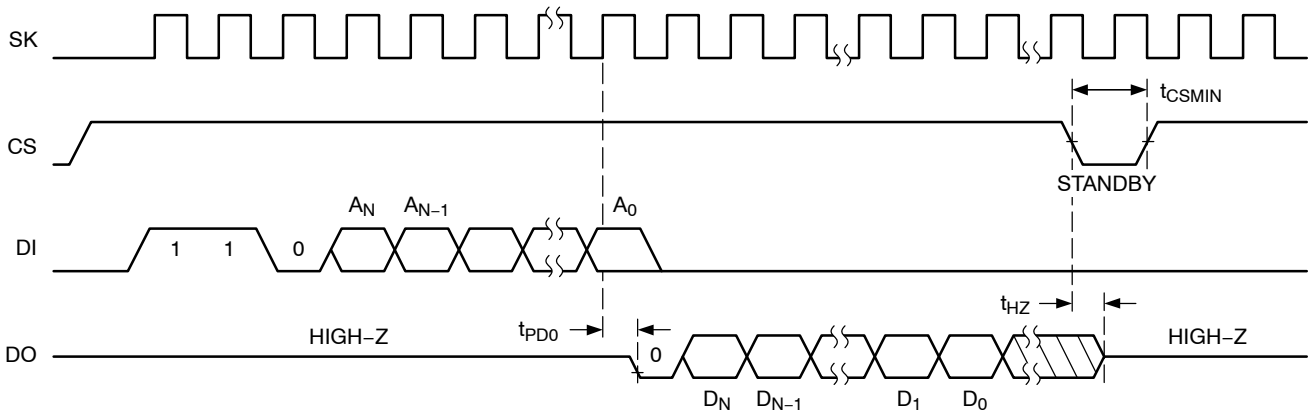


Figure 3. Read Instruction Timing

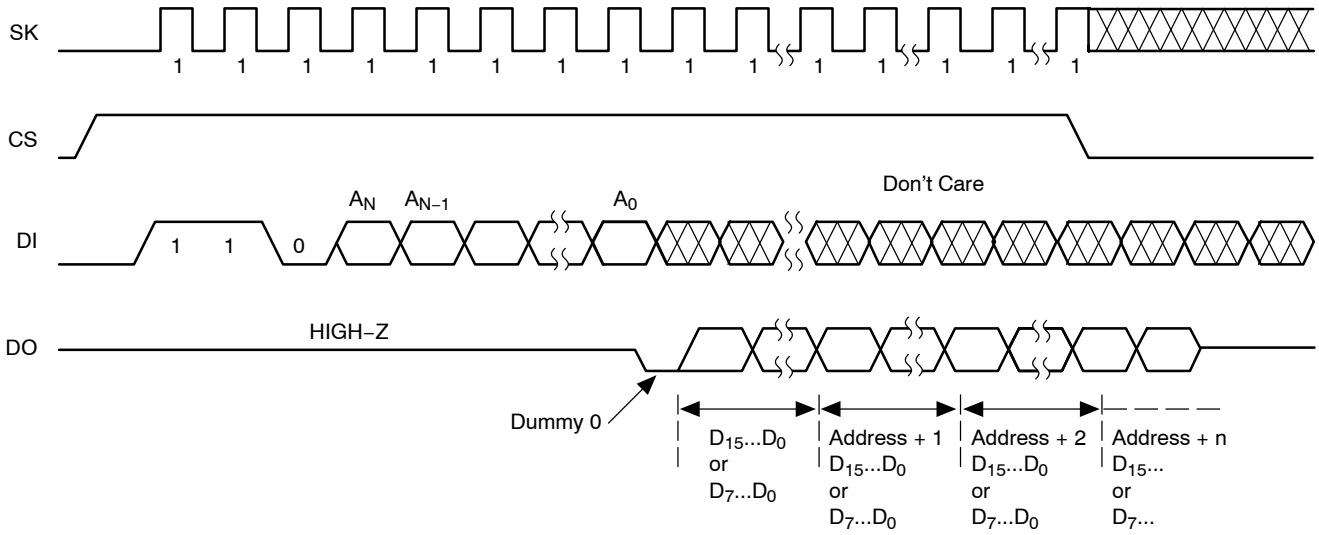


Figure 4. Sequential Read Instruction Timing

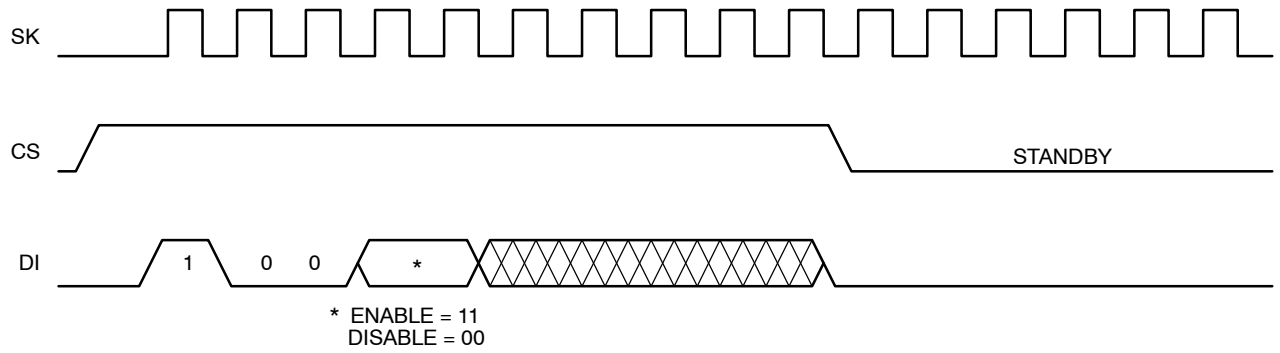


Figure 5. EWEN/EWDS Instruction Timing

Write

After receiving a WRITE command, address and the data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN} (See **Design Note** for details). The falling edge of CS will start the self clocking clear and data store cycle of the memory location specified in the instruction. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46R can be determined by selecting the device and polling the DO pin. Since this device features Auto−Clear before write, it is NOT necessary to erase a memory location before it is written into.

Erase

Upon receiving an ERASE command and address, the CS (Chip Select) pin must be deasserted for a minimum of t_{CSMIN} after the proper number of clock pulses (See **Design Note**). The falling edge of CS will start the self clocking clear cycle of the selected memory location. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46R can be determined by selecting the device and polling the DO pin. Once cleared, the content of a cleared location returns to a logical “1” state.

Erase All

Upon receiving an ERAL command, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking clear cycle of all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46R can be determined by selecting the device and polling the DO pin. Once cleared, the contents of all memory bits return to a logical “1” state.

Write All

Upon receiving a WRAL command and data, the CS (Chip Select) pin must be deselected for a minimum of t_{CSMIN}. The falling edge of CS will start the self clocking data write to all memory locations in the device. The clocking of the SK pin is not necessary after the device has entered the self clocking mode. The ready/busy status of the CAT93C46R can be determined by selecting the device and polling the DO pin. It is not necessary for all memory locations to be cleared before the WRAL command is executed.

Design Note

With CAT93C46R, after the last data bit has been sampled, Chip Select (CS) must be brought Low before the next rising edge of the clock (SK) in order to start the self−timed high voltage cycle. This is important because if the CS is brought low before or after this specific frame window, the addressed location will not be programmed or erased.

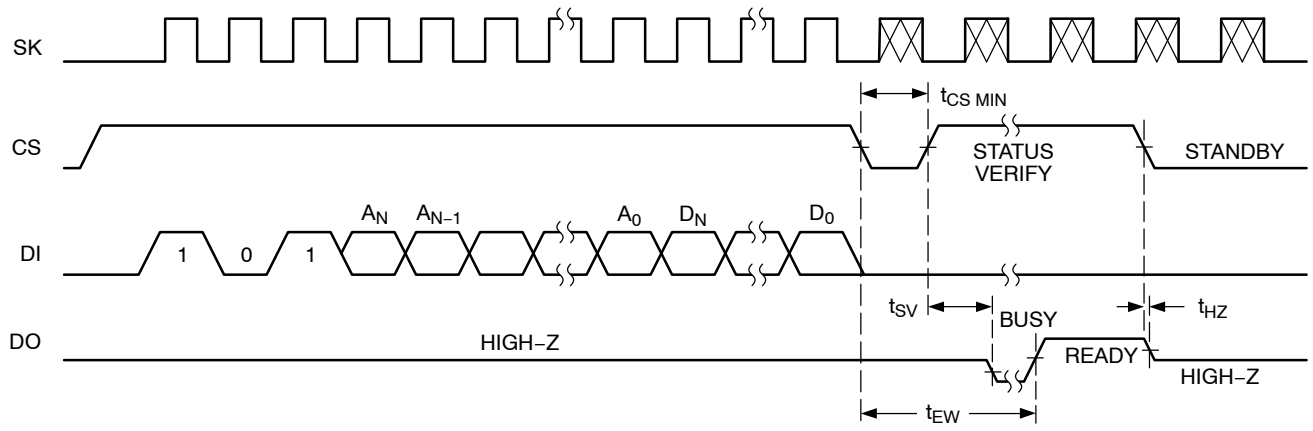


Figure 6. Write Instruction Timing

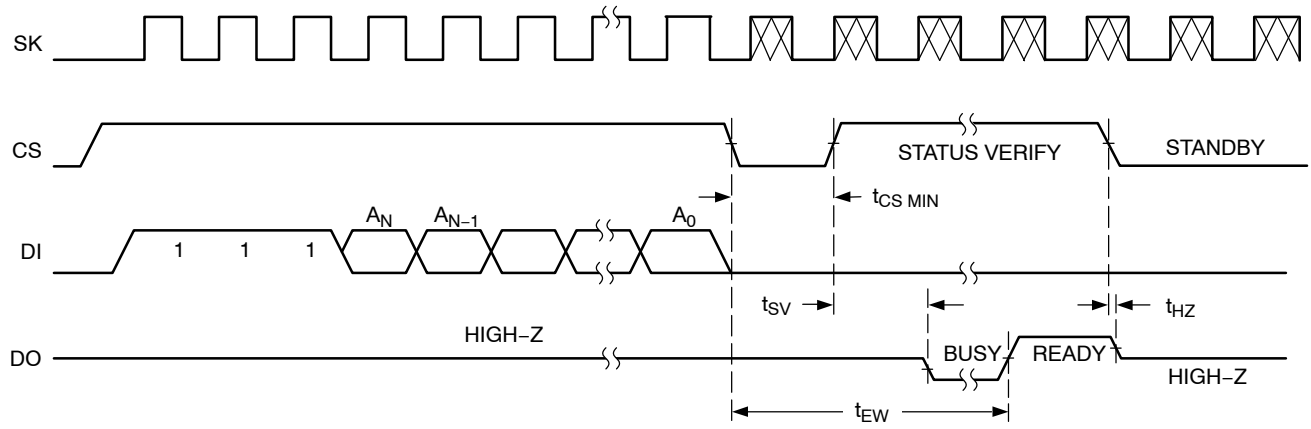


Figure 7. Erase Instruction Timing

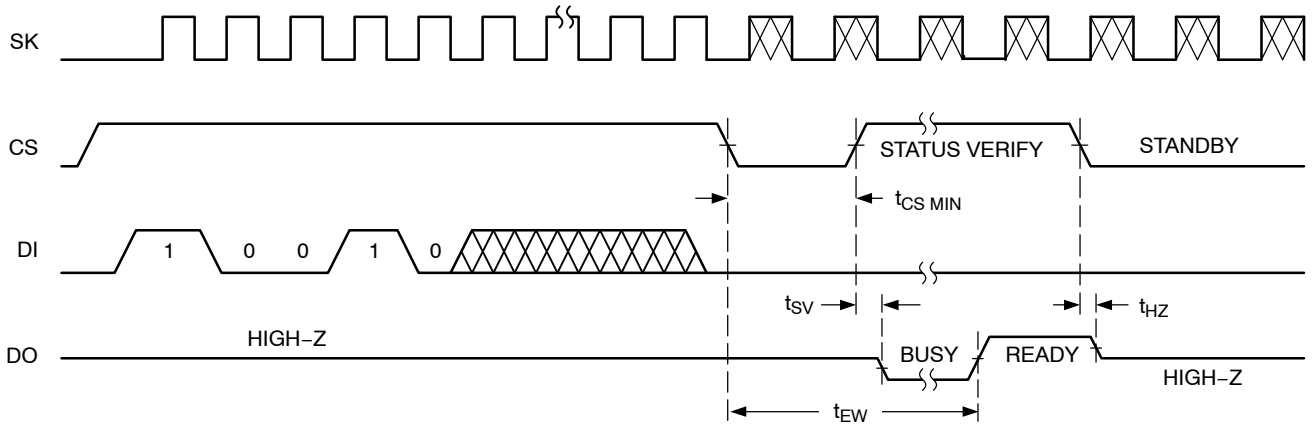


Figure 8. ERAL Instruction Timing

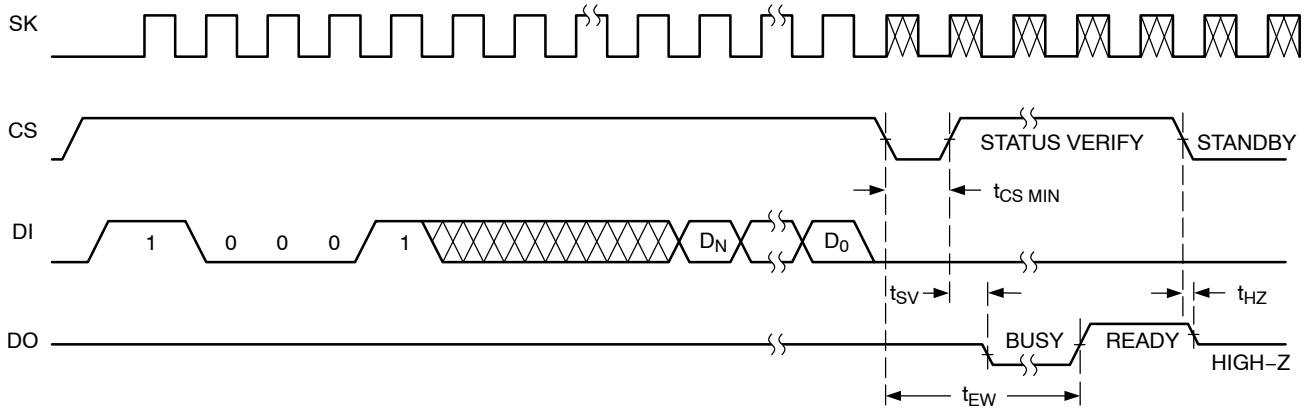
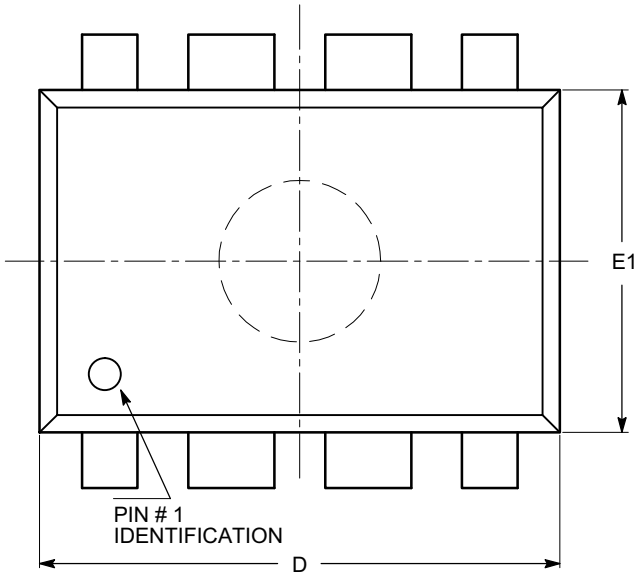


Figure 9. WRAL Instruction Timing

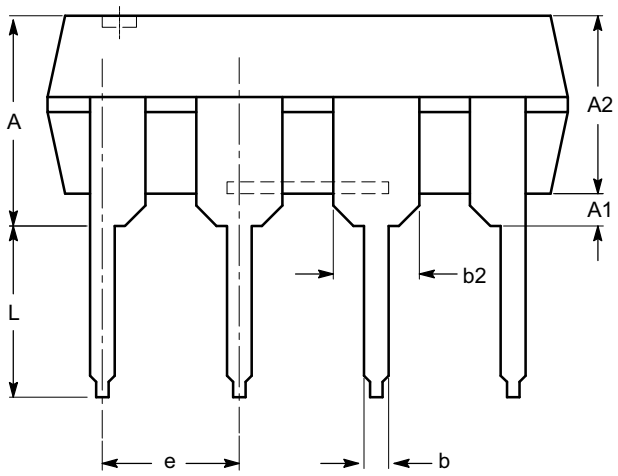
PACKAGE DIMENSIONS

PDIP−8, 300 mils
CASE 646AA−01
ISSUE A

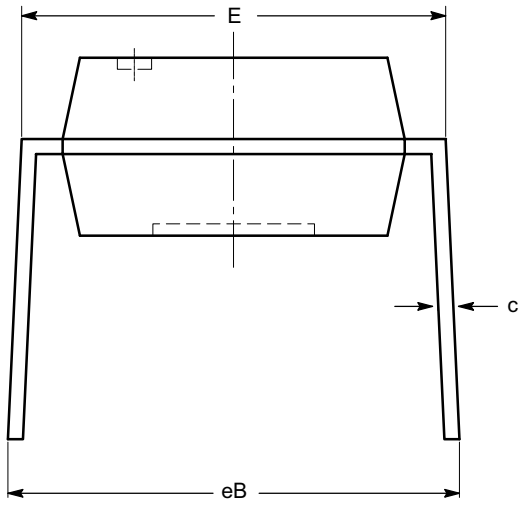


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.46	0.56
b2	1.14	1.52	1.78
c	0.20	0.25	0.36
D	9.02	9.27	10.16
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.87		10.92
L	2.92	3.30	3.80



SIDE VIEW

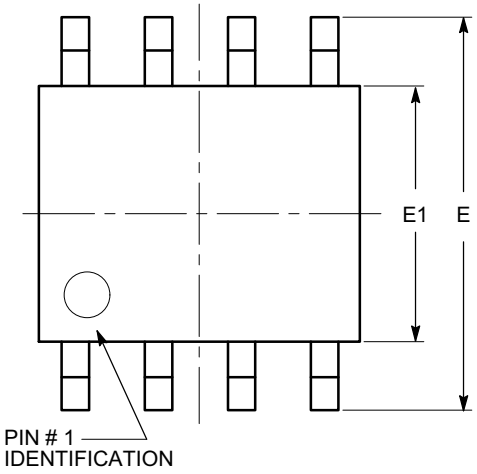


END VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MS-001.

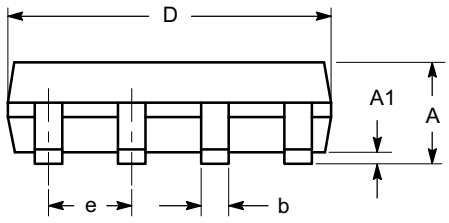
PACKAGE DIMENSIONS

SOIC 8, 150 mils
CASE 751BD−01
ISSUE O

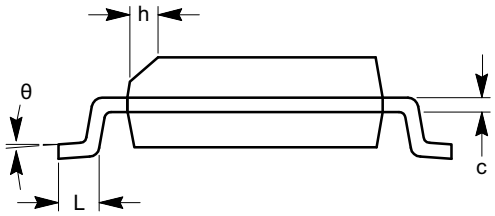


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	4.80		5.00
E	5.80		6.20
E1	3.80		4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

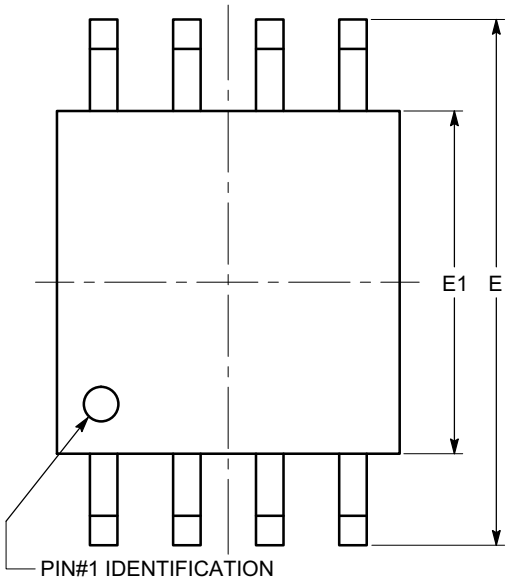


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

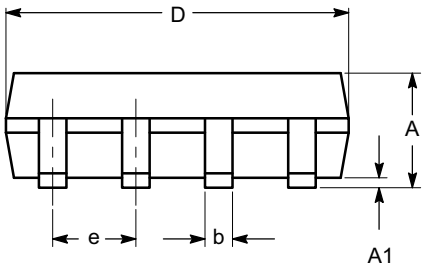
PACKAGE DIMENSIONS

SOIC−8, 208 mils
CASE 751BE−01
ISSUE O

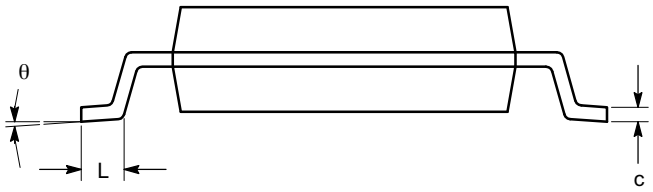


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			2.03
A1	0.05		0.25
b	0.36		0.48
c	0.19		0.25
D	5.13		5.33
E	7.75		8.26
E1	5.13		5.38
e		1.27 BSC	
L	0.51		0.76
θ	0°		8°



SIDE VIEW

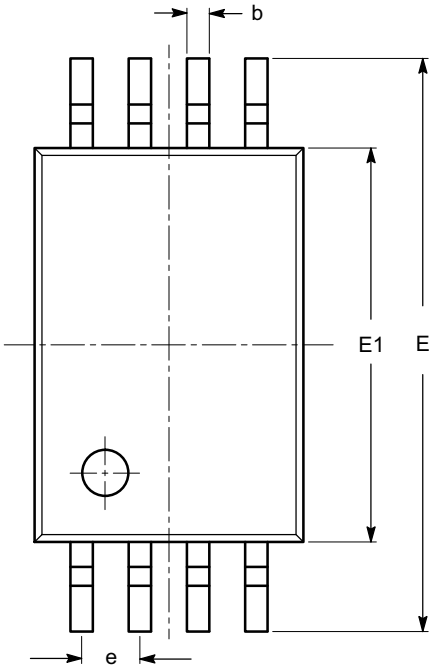


END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with EIAJ EDR-7320.

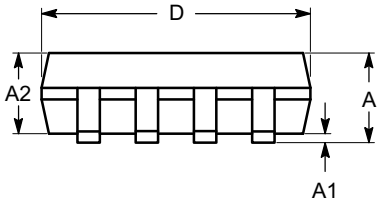
PACKAGE DIMENSIONS

TSSOP8, 4.4x3
CASE 948AL−01
ISSUE O

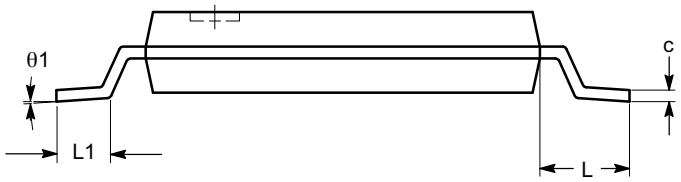


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80	0.90	1.05
b	0.19		0.30
c	0.09		0.20
D	2.90	3.00	3.10
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e	0.65 BSC		
L	1.00 REF		
L1	0.50	0.60	0.75
θ	0°		8°



SIDE VIEW

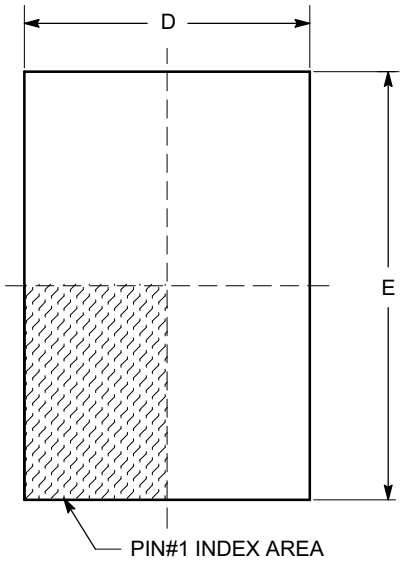


END VIEW

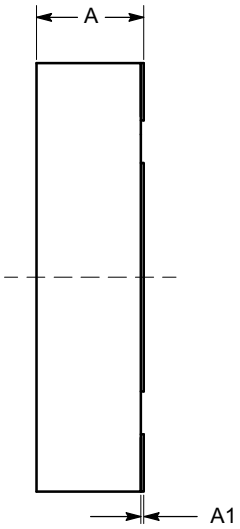
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

PACKAGE DIMENSIONS

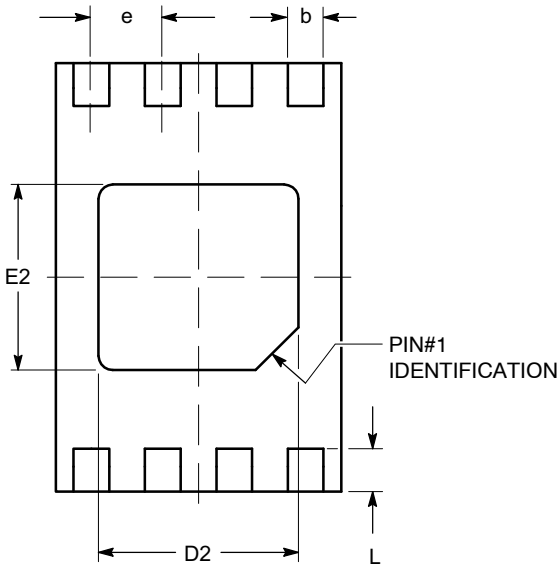
TDFN8, 2x3
CASE 511AK−01
ISSUE A



TOP VIEW

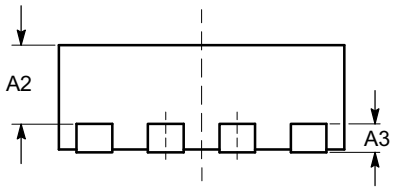


SIDE VIEW



BOTTOM VIEW

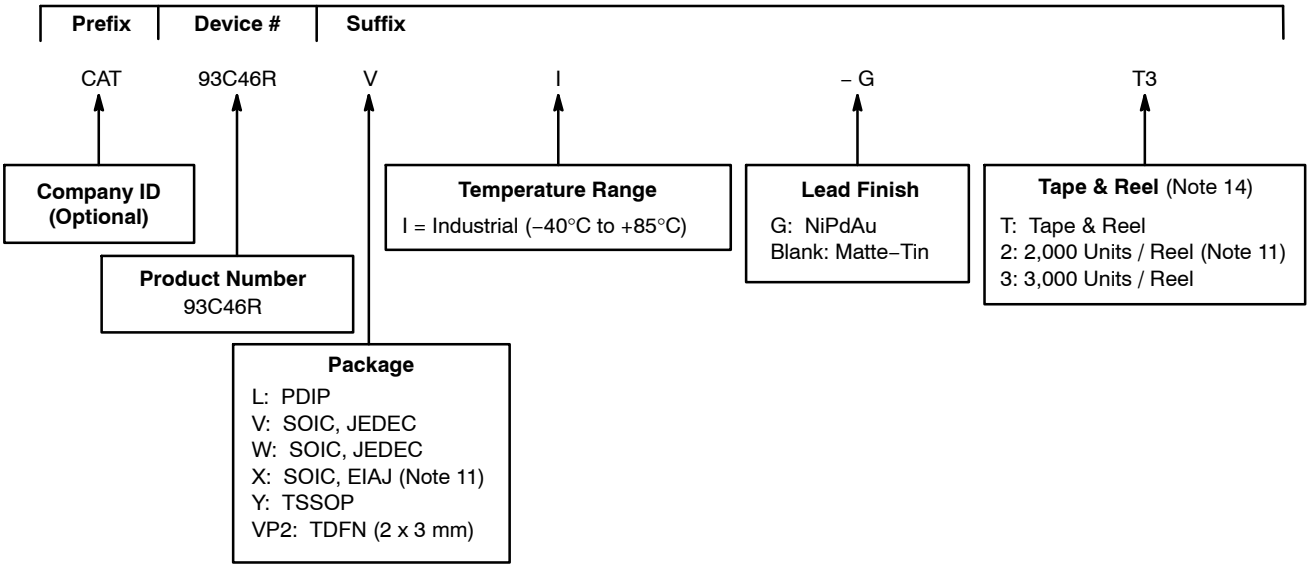
SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.45	0.55	0.65
A3		0.20 REF	
b	0.20	0.25	0.30
D	1.90	2.00	2.10
D2	1.30	1.40	1.50
E	2.90	3.00	3.10
E2	1.20	1.30	1.40
e		0.50 TYP	
L	0.20	0.30	0.40



FRONT VIEW

Notes:
(1) All dimensions are in millimeters.
(2) Complies with JEDEC MO-229.

Example of Ordering Information (Note 8)



ORDERING INFORMATION

Orderable Part Numbers
CAT93C46RLI–G
CAT93C46RVI–GT3
CAT93C46RWI–GT3
CAT93C46RXI–T2
CAT93C46RYI–GT3
CAT93C46RVP2IGT3 (Note 13)

8. The device used in the above example is a CAT93C46RVI–GT3 (SOIC, Industrial Temperature, NiPdAu, Tape & Reel).
9. All packages are RoHS–compliant (Lead–free, Halogen–free).
10. The standard lead finish is NiPdAu.
11. For SOIC, EIAJ (X) package the standard lead finish is Matte–Tin. This package is available in 2,000 pcs/reel, i.e. CAT93C46RXI–T2.
12. For additional package and temperature options, please contact your nearest ON Semiconductor Sales office.
13. Part number is not exactly the same as the "Example of Ordering Information" shown above. For this part number there is NO hyphen in the orderable part number.
14. For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303–675–2175 or 800–344–3860 Toll Free USA/Canada
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N. American Technical Support: 800–282–9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81–3–5773–3850

ON Semiconductor Website: **www.onsemi.com**

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For additional information, please contact your local Sales Representative

CAT93C46R/D