CY62177EV30 MoBL®

32 Mbit (2M x 16 / 4M x 8) Static RAM

Features

- TSOP I Configurable as 2M x 16 or as 4M x 8 SRAM
- Very High Speed
  - 55 ns
- Wide Voltage Range
  - 2.2V to 3.7V
- Ultra Low Standby Power
  - Typical Standby Current: 3 μA
  - Maximum Standby Current: 25 μA
- Ultra Low Active Power
  - Typical Active Current: 4.5 mA at f = 1 MHz
- Easy Memory Expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ Features
- Automatic Power Down when Deselected
- CMOS for Optimum Speed and Power
- Available in Pb-Free 48-Ball FBGA and TSOPI Package

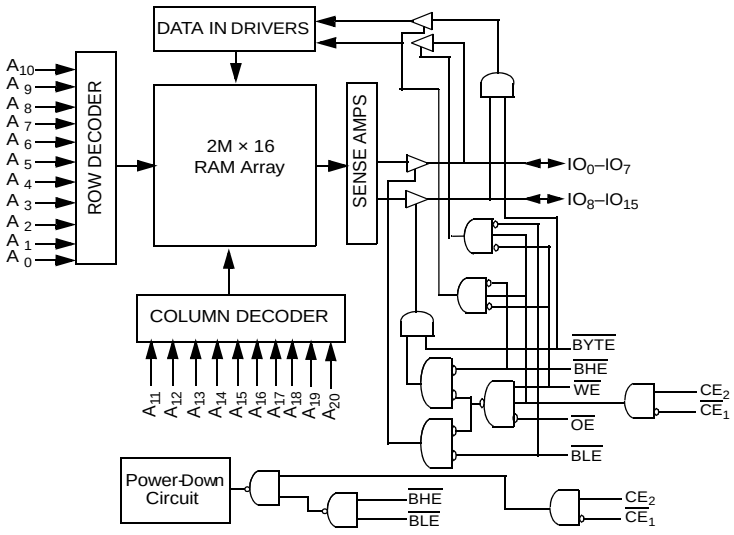
Functional Description

The CY62177EV30 is a high performance CMOS static RAM organized as 2M words by 16 bits and 4M words by 8 bits[1]. This device features advanced circuit design to provide ultra low active current. It is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption by 99 percent when addresses are not toggling. The device can also be put into standby mode when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW or both $\overline{BHE}$ and $\overline{BLE}$ are HIGH). The input and output pins (IO_0 through IO_{15}) are placed in a high impedance state when: deselected ($\overline{CE}_1$HIGH or CE_2 LOW), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}_1$ LOW, CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Write Enable ($\overline{WE}$) input LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins (IO_0 through IO_7), is written into the location specified on the address pins (A_0 through A_{20}). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins (IO_8 through IO_{15}) is written into the location specified on the address pins (A_0 through A_{20}). To read from the device, take Chip Enables ($\overline{CE}_1$ LOW and CE_2 HIGH) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins appear on IO_0 to IO_7. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory appears on IO_8 to IO_{15}. See the Truth Table on page 9 for a complete description of read and write modes.

Pin #13 of the 48 TSOP1 package is a DNU pin that must be left floating at all times to ensure proper application.

Logic Block Diagram



Note

1. For best practice recommendations, refer to the Cypress application note “System Design Guidelines” on http://www.cypress.com.

Pin Configuration

Figure 1. 48-Ball VFBGA [2, 3]

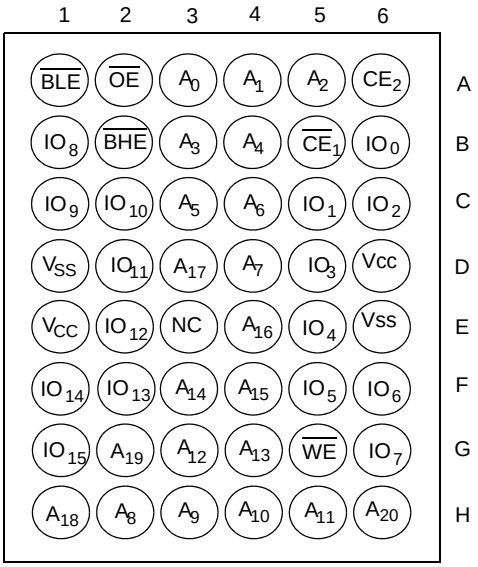
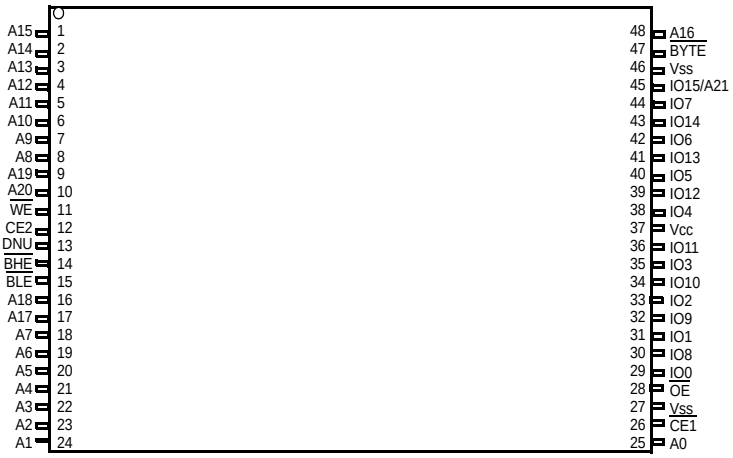


Figure 2. 48-Pin TSOPI (Forward) (2M x 16 / 4M x 8) [3, 4, 5]



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
					f = 1 MHz		f = f_{Max}			
	Min	Typ[6]	Max		Typ[6]	Max	Typ[6]	Max	Typ[6]	Max
CY62177EV30LL	2.2	3.0	3.7	55	4.5	5.5	35	45	3	25

Notes
2. Ball E3 for the FBGA package is used to upgrade to a 64M density.
3. NC pins are not connected on the die.
4. DNU Pin# 13 needs to be left floating to ensure proper application.
5. The BYTE pin in the 48-TSOPI package has to be tied to V_{CC} to use the device as a 2M x 16 SRAM. The 48-TSOPI package can also be used as a 4M x 8 SRAM by tying the BYTE signal to V_{SS}. In the 4M x 8 configuration, Pin 45 is A21, while BHE, BLE, and IO_8 to IO_{14} pins are not used.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25°C$.

Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to + 150°C

Ambient Temperature with Power Applied ..... –55°C to + 125°C

Supply Voltage to Ground Potential .....–0.3V to $V_{CC(max)}$ + 0.3V

DC Voltage Applied to Outputs in High Z State [7, 8].....–0.3V to $V_{CC\ (max)}$ + 0.3V

DC Input Voltage [7, 8] ..... –0.3V to $V_{CC\ (max)}$ + 0.3V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch Up Current .....>200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[9]
CY62177EV30LL	Industrial	–40°C to +85°C	2.2V to 3.7V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		55 ns			Unit
				Min	Typ[6]	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = –0.1 mA	V_{CC} = 2.20V	2.0			V
		I_{OH} = –1.0 mA	V_{CC} = 2.70V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 0.1 mA	V_{CC} = 2.20V			0.4	V
		I_{OL} = 2.1 mA	V_{CC} = 2.70V			0.4	V
V_{IH}	Input HIGH Voltage	V_{CC} = 2.2V to 2.7V		1.8		V_{CC} + 0.3V	V
		V_{CC}= 2.7V to 3.7V		2.2		V_{CC} + 0.3V	V
V_{IL}	Input LOW Voltage	V_{CC} = 2.2V to 2.7V		–0.3		0.6	V
		V_{CC}= 2.7V to 3.7V	For VFBGA package	–0.3		0.8	V
			For TSOP I package	–0.3		0.7[10]	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1		+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1		+1	µA
I_{CC}	V_{CC} Operating Supply Current	f = f_{Max} = $1/t_{RC}$	V_{CC} = $V_{CC(max)}$ I_{OUT} = 0 mA CMOS levels		35	45	mA
		f = 1 MHz			4.5	5.5	mA
I_{SB2} [5, 11]	Automatic CE Power Down Current—CMOS Inputs	$\overline{CE_1}$ ≥ V_{CC} – 0.2V or CE_2 ≤ 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0, V_{CC} = 3.7V			3	25	µA

Capacitance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	15	pF
C_{OUT}	Output Capacitance		15	pF

Notes

7. $V_{IL(min)}$ = –2.0V for pulse durations less than 20 ns.
8. $V_{IH(max)}$ = V_{CC} + 0.75V for pulse durations less than 20 ns.
9. Full Device AC operation assumes a 100 µs ramp time from 0 to V_{CC} (min) and 200 µs wait time after V_{CC} stabilization.
10. Under DC conditions the device meets a V_{IL} of 0.8V. However, in dynamic conditions Input LOW Voltage applied to the device must not be higher than 0.7V. This is applicable to TSOP I package only.
11. Chip enables ($\overline{CE_1}$ and CE_2) need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Thermal Resistance

Tested initially and after any design or process changes that may affect these parameters.

Parameter	Description	Test Conditions	TSOPI	FBGA	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 × 4.5 inch, 2-layer printed circuit board	44.66	28.12	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		12.12	12.06	°C/W

Figure 3. AC Test Loads and Waveforms

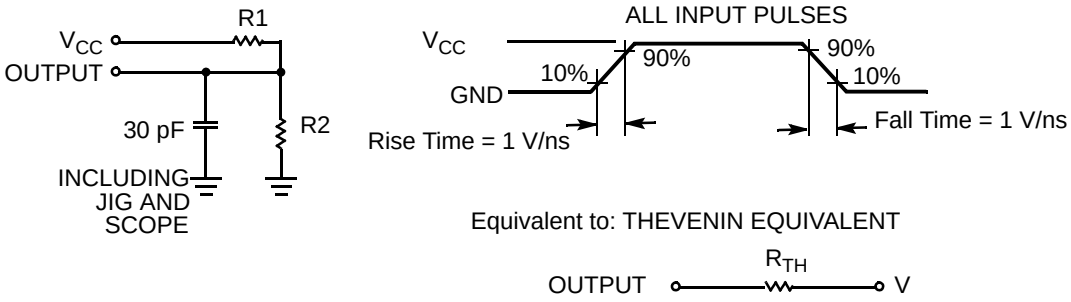


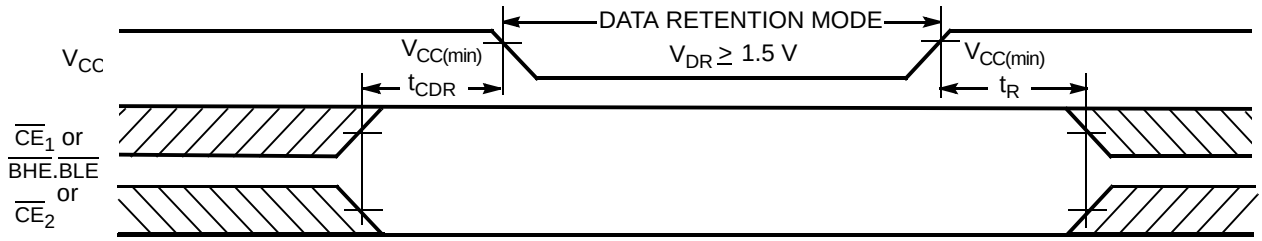
Table 1. AC Test Loads

Parameter	2.5V	3.3V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Data Retention Characteristics Over the Operating Range

Parameter	Description	Conditions	Min	Typ[6]	Max	Unit
V_{DR}	V_{CC} for Data Retention		1.5			V
I_{CCDR} [11]	Data Retention Current	V_{CC}= 1.5V, $\overline{CE_1} \geq V_{CC} - 0.2V$, $CE_2 \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$			17	µA
t_{CDR}[12]	Chip Deselect to Data Retention Time		0			ns
t_R[13]	Operation Recovery Time		t_{RC}			ns

Figure 4. Data Retention Waveform [14]



Notes

12. Tested initially and after any design or process changes that may affect these parameters.
13. Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq 100$ µs or stable at $V_{CC(min)} \geq 100$ µs.
14. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip is deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.

Switching Characteristics

Over the Operating Range [15]

Parameter	Description	55 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read Cycle Time	55		ns
t_{AA}	Address to Data Valid		55	ns
t_{OHA}	Data Hold from Address Change	6		ns
t_{ACE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Data Valid		55	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		25	ns
t_{LZOE}	$\overline{OE}$ LOW to LOW Z[16]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[16, 17]		18	ns
t_{LZCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Low Z[16]	10		ns
t_{HZCE}	$\overline{CE}_1$ HIGH and CE_2 LOW to High Z[16, 17]		18	ns
t_{PU}	$\overline{CE}_1$ LOW and CE_2 HIGH to Power Up	0		ns
t_{PD}	$\overline{CE}_1$ HIGH and CE_2 LOW to Power Down		55	ns
t_{DBE}	BLE/BHE LOW to Data Valid		55	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to Low Z [16]	10		ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z [16, 17]		18	ns
Write Cycle[18]				
t_{WC}	Write Cycle Time	55		ns
t_{SCE}	$\overline{CE}_1$ LOW and CE_2 HIGH to Write End	40		ns
t_{AW}	Address Setup to Write End	40		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Setup to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	40		ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to Write End	40		ns
t_{SD}	Data Set up to Write End	25		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[16, 17]		20	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[16]	10		ns

Notes

15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 1V/ns, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in AC Test Loads on page 4.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZBE} is less than t_{LZBE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, t_{HZBE}, and t_{HZWE} transitions are measured when the outputs enter a high impedence state.
18. The internal Write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}_1 = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 5. Read Cycle 1 (Address Transition Controlled)[19, 20]

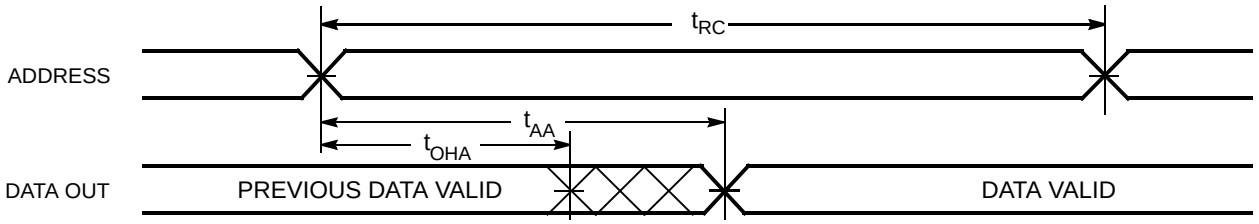
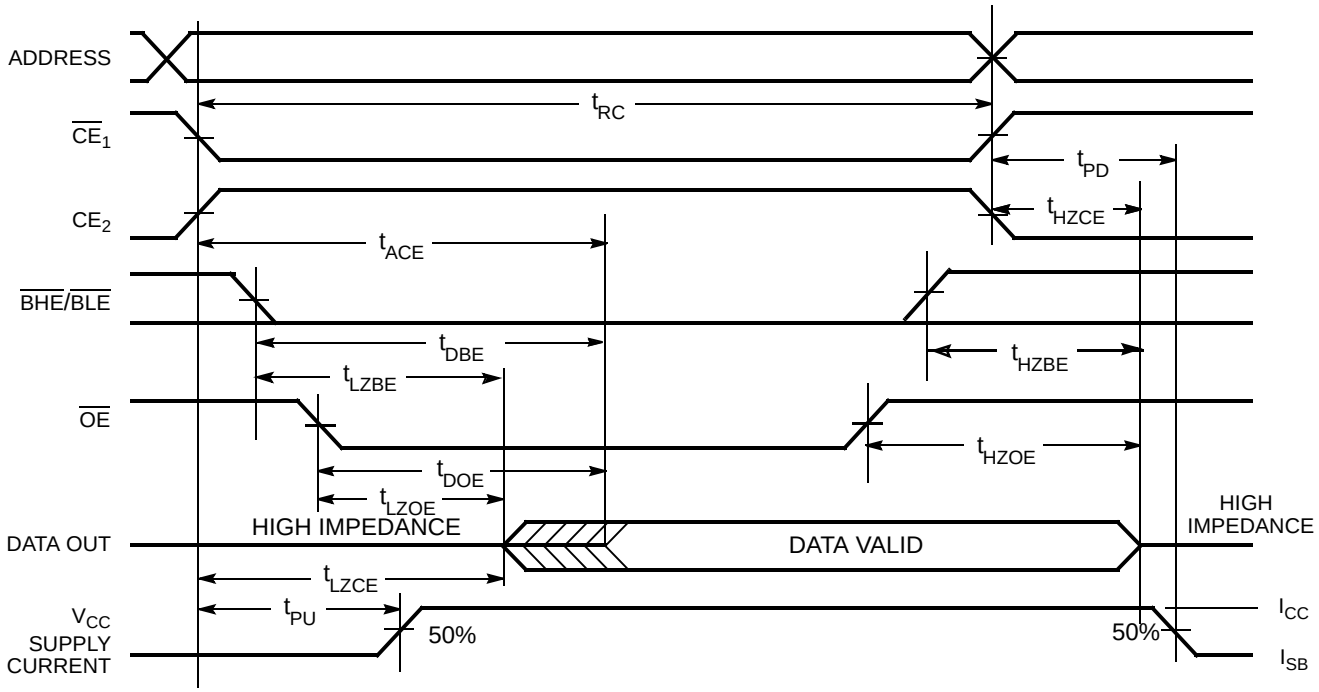


Figure 6. Read Cycle 2 ($\overline{OE}$ Controlled)[20, 21]



Notes
19. The device is continuously selected. $\overline{OE}$, $\overline{CE_1} = V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE} = V_{IL}$, and $CE_2 = V_{IH}$.
20. $\overline{WE}$ is HIGH for read cycle.
21. Address valid prior to or coincident with $\overline{CE_1}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 7. Write Cycle 1 ($\overline{WE}$ Controlled) [18, 22, 23, 24]

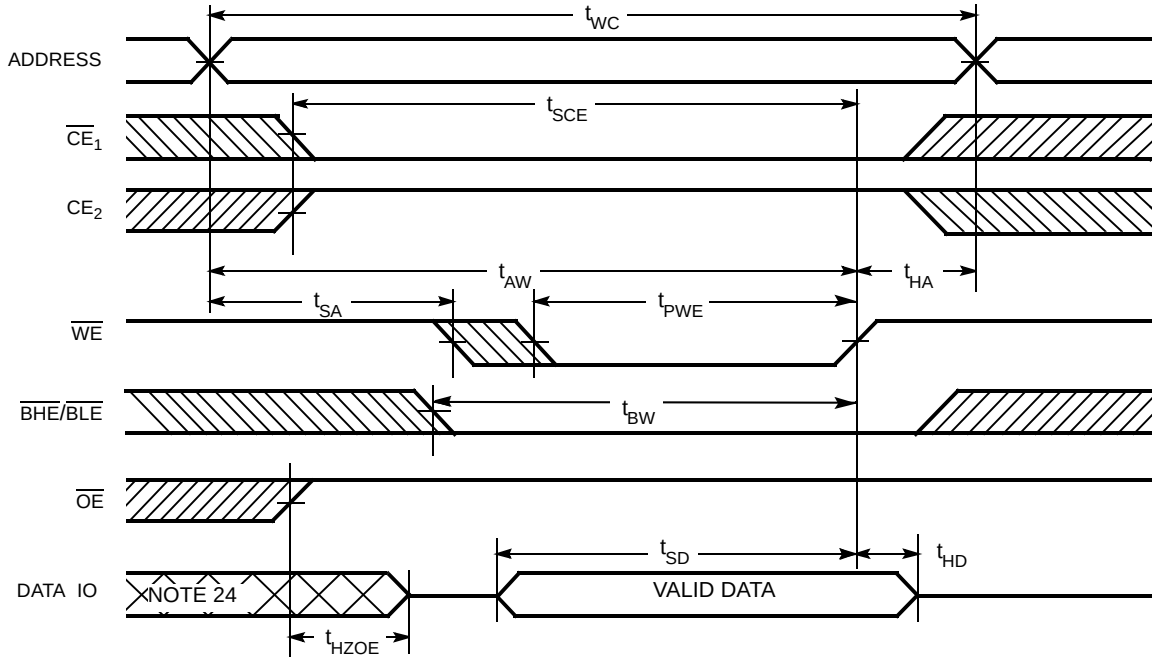
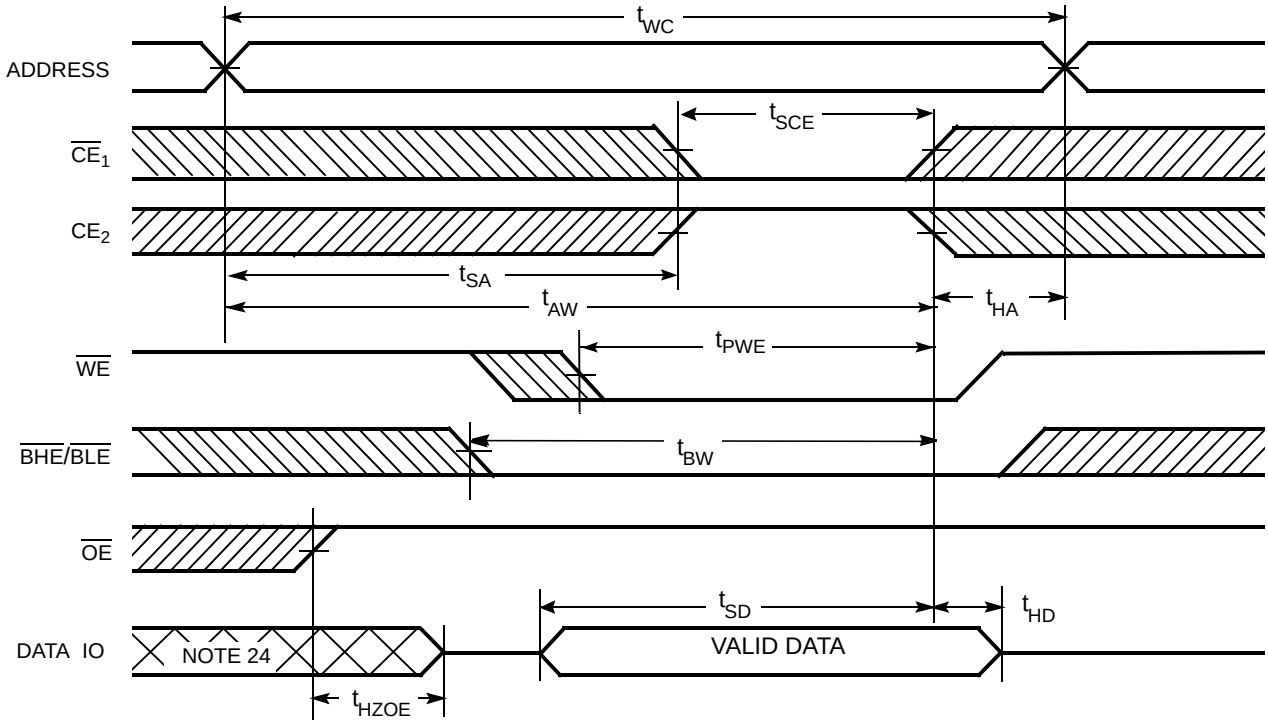


Figure 8. Write Cycle 2 ($\overline{CE_1}$ or CE_2 Controlled) [18, 22, 23, 24]



Notes
22. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
23. If $\overline{CE_1}$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
24. During this period the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 9. Write Cycle 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[23, 24]

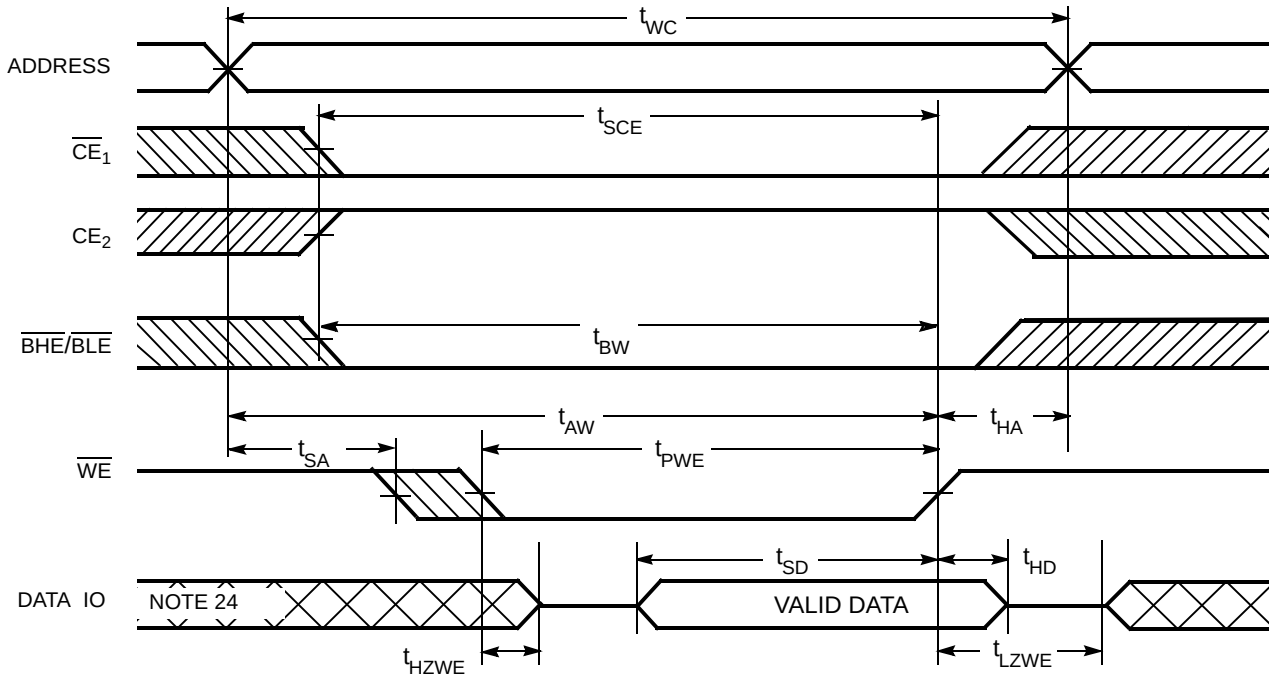
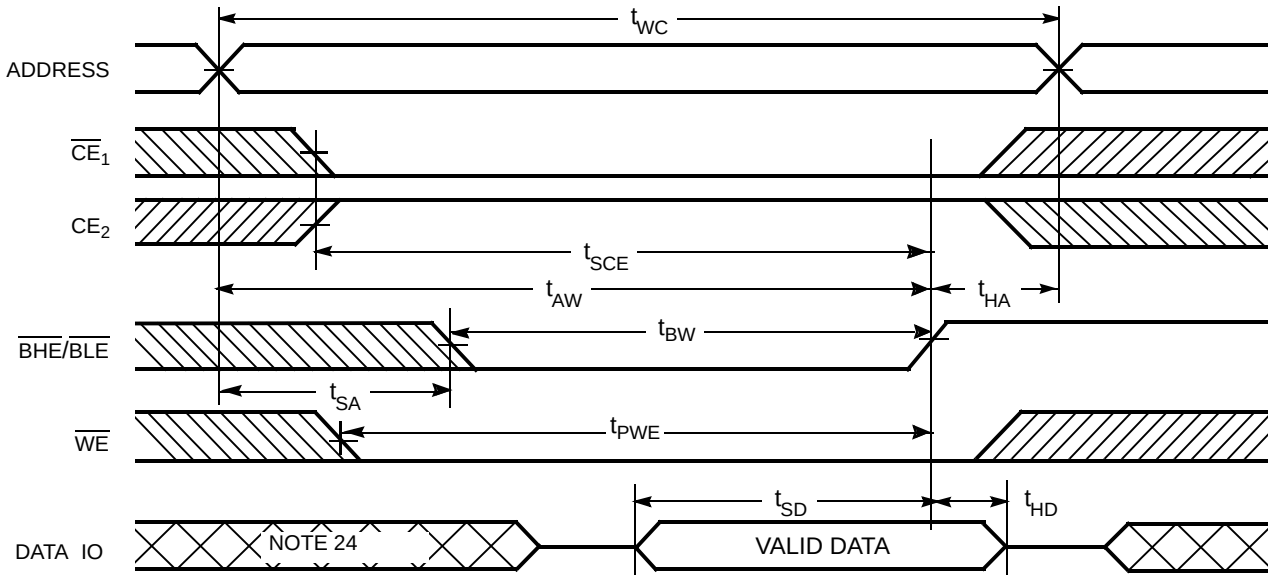


Figure 10. Write Cycle 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)[23,24]



Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X	L	X	X	X	X	High Z	Deselect/Power Down	Standby (I_{SB})
X	X	X	X	H	H	High Z	Deselect/Power Down	Standby (I_{SB})
L	H	H	L	L	L	Data Out (IO_0–IO_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	High Z (IO_8–IO_{15}): Data Out (IO_0–IO_7)	Read	Active (I_{CC})
L	H	H	L	L	H	Data Out (IO_8–IO_{15}); High Z (IO_0–IO_7)	Read	Active (I_{CC})
L	H	L	X	L	L	Data In (IO_0–IO_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	High Z (IO_8–IO_{15}); Data In (IO_0–IO_7)	Write	Active (I_{CC})
L	H	L	X	L	H	Data In (IO_8–IO_{15}); High Z (IO_0–IO_7)	Write	Active (I_{CC})
L	H	H	H	L	H	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output Disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output Disabled	Active (I_{CC})

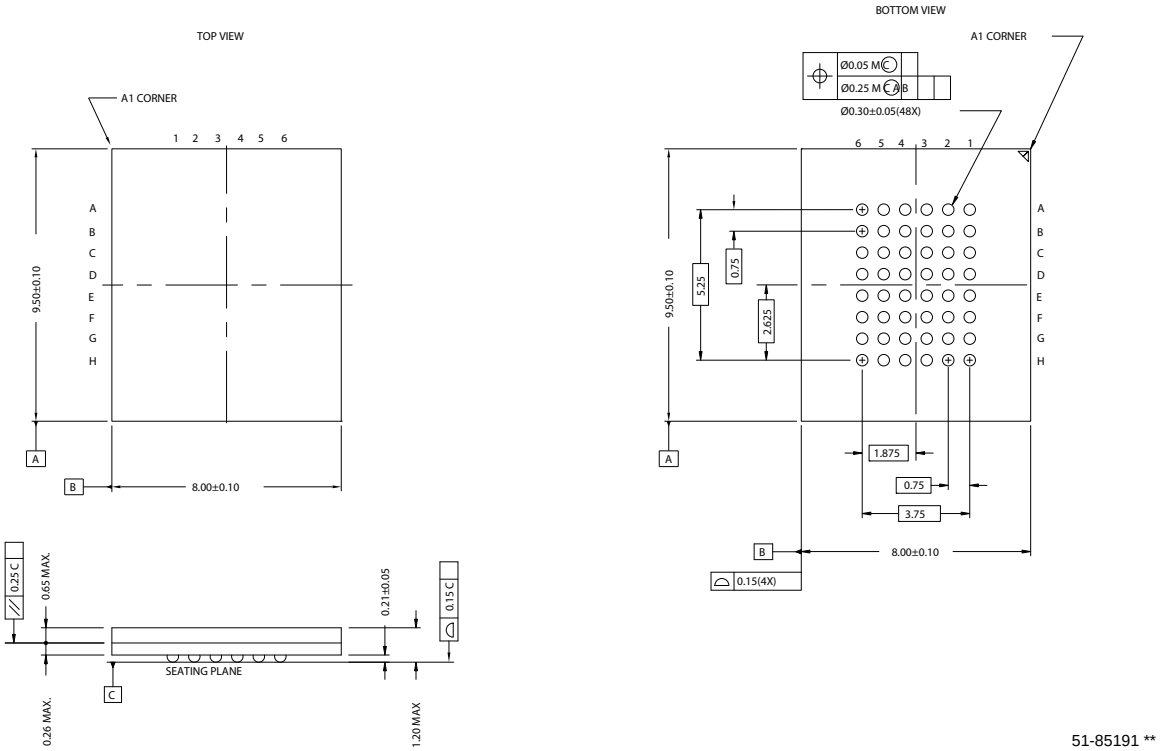
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
55	CY62177EV30LL-55BAXI	51-85191	48-Ball Fine Pitch Ball Grid Array (8 × 9.5 × 1.2 mm) Pb-Free	Industrial
	CY62177EV30LL-55ZXI	51-85183	48-Pin TSOP I (12 x 18.4 x 1 mm) Pb-Free	

Shaded areas contain advance information. Please contact your local Cypress sales representative for availability of these parts.

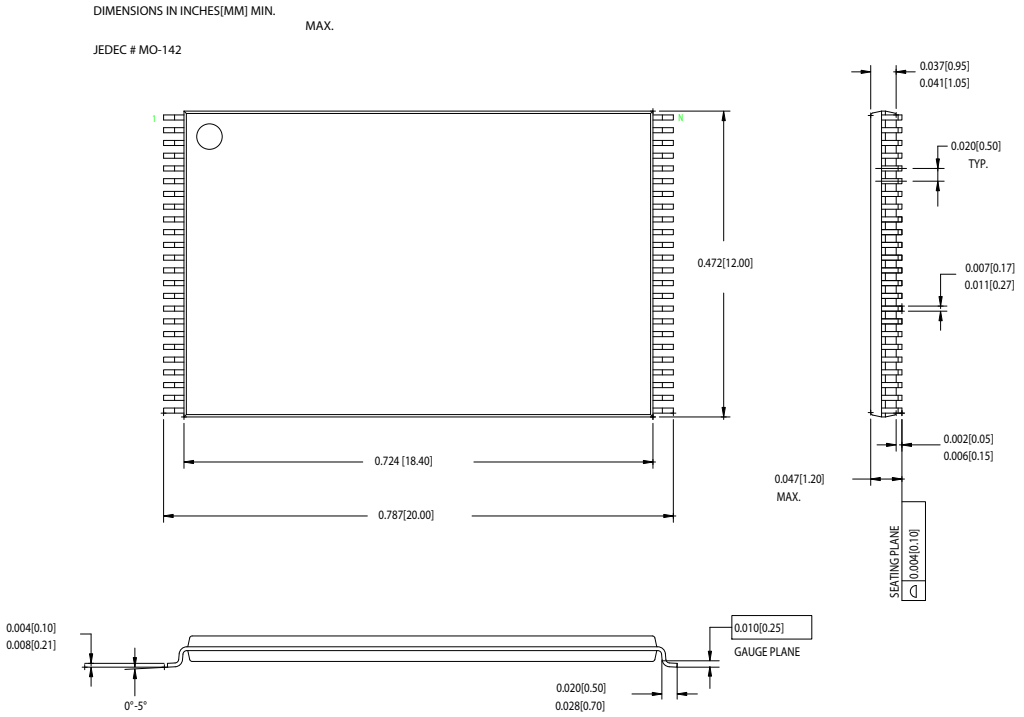
Package Diagrams

Figure 11. 48-Ball FBGA (8 x 9.5 x 1.2 mm)



Package Diagrams (continued)

Figure 12. 48-Pin TSOP I (12 x 18.4 x 1 mm)



51-85183 *A

Document History Page

Document Title: CY62177EV30 MoBL® 32 Mbit (2M x 16 / 4M x 8) Static RAM Document Number: 001-09880				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	498562	NXR	See ECN	New Datasheet
*A	2544845	VKN/PYRS	07/29/08	Removed 45 ns speed bin Added 70 ns speed bin Added 48-Pin TSOPI package Added footnote# 4 related to TSOPI package Added footnote# 9 related to I_{SB2} and I_{CCDR} Updated Ordering information table
*B	2589750	VKN/PYRS	10/15/08	Changed pin functions of pin# 10 from NC to A20 and pin# 13 from A20 to DNU in 48-Pin TSOPI package
*C	2668432	VKN/PYRS	03/03/09	Replaced 70 ns speed with 55 ns Extended the V_{CC} range to 3.7V Changed $I_{CC\ (max)}$ spec from 2.8 mA to 4.5 mA at f = 1 MHz Changed $I_{CC\ (max)}$ spec from 30 mA to 45 mA at f = $f_{(max)}$ Removed I_{SB1} spec Changed $I_{SB2\ (max)}$ spec from 17 µA to 25 µA Modified footnote #10
*D	2779867	VKN	10/06/09	Converted from Preliminary to Final Changed $I_{CC\ (max)}$ spec from 4.5 mA to 5.5 mA at f = 1 MHz Changed $I_{CC\ (typ)}$ spec from 2.2 mA to 4.5 mA at f = 1 MHz Changed $I_{CC\ (typ)}$ spec from 28 mA to 35 mA at f = $f_{(max)}$ Added V_{IL} spec for TSOP I package and footnote# 10 Changed C_{OUT} spec from 10 pF to 15 pF Included thermal specs Changed t_{OHA} spec from 10ns to 6ns

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