

## High Power LED Driver

The ISL97801 is a high-power LED backlight driver with an integrated 36V FET designed to drive up to 8 high-power LEDs in series. The PWM converter runs from an internally generated 1MHz clock. With efficiencies over 90% the regulator provides tight control of LED current and may be configured in either boost or buck topologies, allowing from 3 to 8 series diodes to be driven from wide input voltages.

LED light level may be controlled either by:

1. LED DC bias current set via the LEVEL pin, or
2. External low frequency PWM control via the ENABLE/PWM pin.

In both control modes optional over temperature thermal protection of the LED reduces the LED DC bias current above an adjustable set temperature, protecting the LED from thermal damage. An optional fault monitor drives an external FET between the input supply and inductor, providing short circuit current protection for the LED and inductor as well as load dump protection for automotive applications. For low cost applications the pass transistor may be omitted and the fault pin bypassed.

The ISL97801 is packaged in a 20 Ld 4mm x 4mm QFN package and is specified for operation over the -40°C to +105°C temperature range.

## Ordering Information

PART NUMBER (Note)	PART MARKING	TAPE & REEL/ QTY	PACKAGE (Pb-free)	PKG. DWG. #
ISL97801ARZ	978 01ARZ	-	20 Ld 4x4 QFN	L20.4x4C
ISL97801ARZ-TK	978 01ARZ	13"/ 1,000	20 Ld 4x4 QFN	L20.4x4C
ISL97801ARZ-T	978 01ARZ	13"/ 6,000	20 Ld 4x4 QFN	L20.4x4C

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

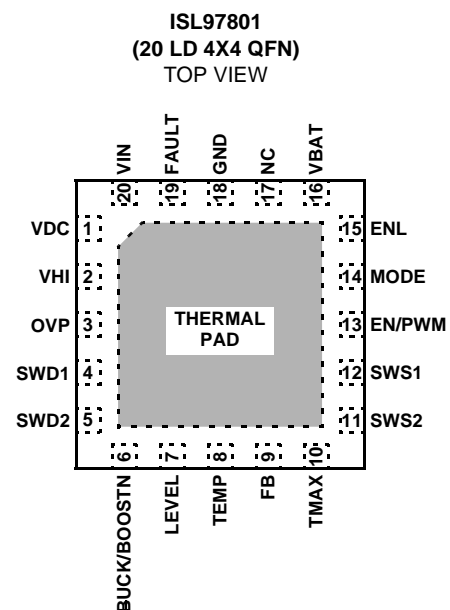
## Features

- Drives 3-8 high-power LEDs in series, up to 32V
- 2.7V to 16V input voltage range
- Boost or Buck configurable switch
- 3A integrated FET
- Automotive load dump protection
- Light output temperature compensation
- LED over-temperature protection
- LED disconnect
- PWM/analog light level control
- Small, 20 Ld 4mm x 4mm QFN package
- Pb-free plus anneal available (RoHS compliant)

## Applications

- Display backlighting
  - Automotive
  - LCD monitor
  - Notebook displays
- LED accent lighting
- Automotive lighting

## Pinout



# ISL97801

## Absolute Maximum Ratings ( $T_A = +25^\circ\text{C}$ )

Maximum pin voltage, all pins except below 6.5V	
$V_{IN}$ , SWS1, SWS2, EN/PWM	18V
VBAT, FAULT, FB	24V
VHI - SWS1, SWS2	6.5V
SWD1, SWD2, OVP	34V
Continuous Output Current	1A

## Thermal Information

Thermal Resistance	$\theta_{JA}$ ( $^\circ\text{C}/\text{W}$ ) /	$\theta_{JC}$ ( $^\circ\text{C}/\text{W}$ )
QFN-20 Package (Notes 1, 2)	39	2.5
Maximum Junction Temperature	+135 $^\circ\text{C}$	
Storage Temperature	-65 $^\circ\text{C}$ to +150 $^\circ\text{C}$	

## Operating Conditions

Temperature Range . . . . . -40 $^\circ\text{C}$  to +105 $^\circ\text{C}$

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

**IMPORTANT NOTE:** All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$

Operating continuously at a junction temperature of +135 $^\circ\text{C}$  will shorten the life of the device while the thermal shutdown may trigger at a higher temperature than +135 $^\circ\text{C}$  since it is a typical number.

### NOTE:

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
- For  $\theta_{JC}$ , the "case temp" location is the center of the exposed metal pad on the package underside.

## Electrical Specifications $V_{BAT} = V_{IN} = 12\text{V}$ , $V_{DC} = 5\text{V}$ , $T_A = -40^\circ\text{C}$ to +105 $^\circ\text{C}$ unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IN}$	Input Supply Voltage	$I_{OUT} = 350\text{mA}$ , 8 LEDs, BUCK/BOOSTN = GND	5		16	V
$V_{IN}$	Input Supply Voltage	$I_{OUT} = 350\text{mA}$ , 5 LEDs, BUCK/BOOSTN = GND, TMAX disabled	2.7		12	V
$V_{BAT}$	Input Supply Monitor	Normal operating range	2.7		16	V
$V_{BATFAULT}$	Supply Fault Threshold	If $V_{BAT} > V_{BATFAULT}$ , FAULT pin is switched to ground	17.6	21	24	V
$I_{SEN}$	Supply Current in $V_{IN}$	No switching, EN/PWM = 1		2.7	3.5	mA
$I_{SDIS}$	Supply Current in $V_{IN}$	No switching, EN/PWM = 0		0.6	2.5	$\mu\text{A}$
$R_{SWITCH}$	Power FET On Resistance	$I_{SWITCH} = 600\text{mA}$		0.15	0.25	$\Omega$
$V_{DC}$	Regulated Auxiliary Supply		4.75	5	5.25	V
$R_{OUTOL}$	Auxiliary Supply Open Loop Output Resistance	$V_{IN} < V_{DC}$			40	$\Omega$
$R_{OUTCL}$	Auxiliary Supply Closed Loop Output Resistance	$V_{IN} > 6\text{V}$ , $F < 100\text{Hz}$			6.5	$\Omega$
$I_{OUT}$	Output Drive Current	4 LED output string, $V_{IN} = V_{BAT} = 10\text{V}$		1		A
$I_{LIMBOOST}$	Power Switch Current Limit	BUCK/BOOSTN = GND		3.6		A
$I_{LIMBUCK}$	Power Switch Current Limit	BUCK/BOOSTN = VDC		2.4		A
OVPH	Over Voltage Positive Going Voltage Mode Threshold	Upper threshold to enter overvoltage fault mode, $T_A = +25^\circ\text{C}$	31	32		V
OVPL	Over Voltage Negative Going Voltage Mode Threshold	Lower threshold to exit overvoltage fault mode, $T_A = +25^\circ\text{C}$		20	23	V
$V_{GATE}$	Protection FET VGS (gate clamp)	$V_{IN} - V_{FAULT}$	9.76	12.2	14.64	V
$V_{GATE}$	Protection FET VGS (gate clamp)	$V_{FAULT} - V_{IN}$	8.16	10.2	12.24	V
$V_{FB}$	Feedback Voltage	System in regulation, $V_{LEVEL} = 1\text{V}$ , $V_{IN} = 12\text{V}$ , 6 LEDs	0.19	0.2	0.21	V

# ISL97801

## Electrical Specifications $V_{BAT} = V_{IN} = 12V$ , $V_{DC} = 5V$ , $T_A = -40^{\circ}C$ to $+105^{\circ}C$ unless otherwise specified. (Continued)

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{LEVEL}$	Light Control Voltage Linear Input Range	Mode = 1, analog control of LED current	0.25		3	V
FB <sub>UV</sub> FAULT	Feedback Undervoltage Fault	$V_{LEVEL} = 1V$ , EN/PWM = 3V	120	160	180	mV
FB <sub>OV</sub> FAULT	Feedback Overvoltage Fault	$V_{LEVEL} = 1V$ , EN/PWM = 3V	220	250	280	mV
$f_{SW}$	Switching Frequency		850	1000	1150	kHz
$f_{DIMMING}$	Maximum Recommended PWM Dimming Frequency	Mode = 1, modulation signal applied to EN/PWM		10		kHz
$t_{SWITCH}$	Load Switch Transition Time	$C_{GATE} = 2nF$		100		ns
RLS <sub>DRIVERL</sub>	Load Switch Driver Impedance Low	EN/PWM = 0		30	50	$\Omega$
RLS <sub>DRIVERH</sub>	Load Switch Driver Impedance High	EN/PWM = 3V		30	50	$\Omega$
$t_{FAULT}$	Fault Timer Period		40	50	58	ms
$t_{DELAY}$	Start-up Delay	Timed LX switching delay	0.85	1	1.17	ms
$V_{FAULTPUMP}$	Fault Pin Charge Pump	$V_{BAT} = V_{IN} = 3V$	6			V
$V_{BOOST}$	Boost Mode Threshold	BUCK/BOOSTN = GND			$0.4V_{DC}$	V
$V_{BUCK}$	Buck Mode Threshold	BUCK/BOOSTN = $V_{DC}$	$0.94V_{DC}$			V
$V_{MODEL}$	Mode Low Threshold	MODE = GND			$1/3V_{DC}$	V
$V_{MODEH}$	Mode High Threshold	MODE = $V_{DC}$	$2/3V_{DC}$			V
en <sub>FAULT</sub>	Input Level Applied to TMAX Pin to Enable Fault Protection				$0.9V_{DC}$	V
dis <sub>FAULT</sub>	Input Level Applied to TMAX Pin to Disable Fault Protection		$0.96V_{DC}$			V
en <sub>TEMP</sub>	Input Level Applied to TEMP Pin to Enable Temperature Compensation		0.5			V
dis <sub>TEMP</sub>	Input Level Applied to TEMP Pin to Disable Temperature Compensation				0.08	V
$T_{COMPP}$	VFB Positive Temperature Compensation; VFB/VFB <sub>nom</sub>	$V_{TEMP}/V_{DC} = 0.80$		1.26		
$T_{COMPN}$	VFB Negative Temperature Compensation; VFB/VFB <sub>nom</sub>	$V_{TEMP}/V_{DC} = 0.20$		0.74		
$T_{TRIP}$	Internal Temperature Protection Threshold			135		$^{\circ}C$
$T_{HYS}$	Internal Temperature Protection Hysteresis			25		$^{\circ}C$
$V_{EN/PWM_L}$	EN/PWM Pin Input Low Threshold				1.2	V
$V_{EN/PWM_H}$	EN/PWM Pin Input High Threshold		2.5			V
$V_{DCUVLO}$	$V_{DC}$ Under Voltage Lockout				2.6	V
Rschottky	Internal Schottky Diode for Buck			15	23	$\Omega$

TABLE 1. LIGHT OUTPUT CONTROL,  $V_{DC} = 5.0V$

MODE	TEMP	OPERATING MODE
1	$(V_{DC} - 0.25) > V > 0.25V$	<b>Standard Mode</b> light level to PWM modulation of EN/PWM input; LED bias current determined by LEVEL voltage, nominal 1V
Don't Care	$V < 0.25V$	Disable temperature compensation
0	$V < (V_{DC} - 0.25)$	<b>Fixed Bias Mode</b> $V_{FB}$ level internally set to 0.4V, independent of $V_{LEVEL}$

Typical Performance Curves

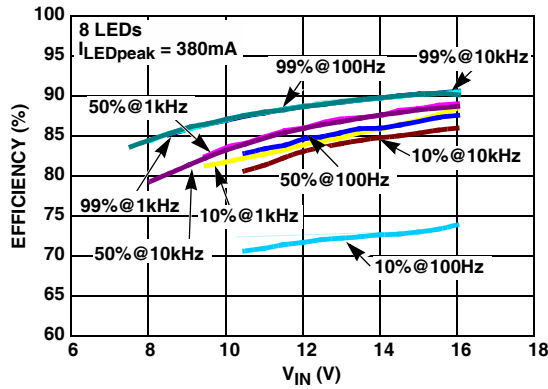


FIGURE 1. 8 LEDs EFFICIENCY vs INPUT VOLTAGE vs DIMMING FREQUENCY AND DUTY CYCLE

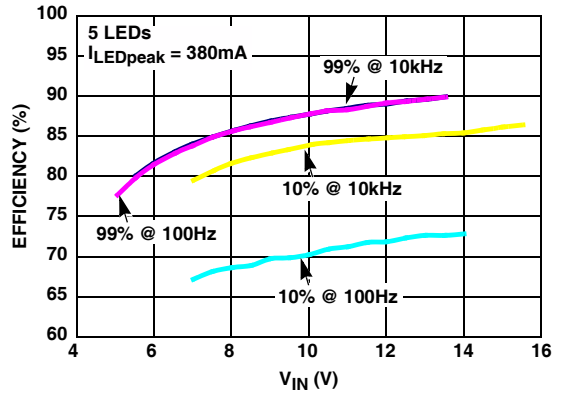


FIGURE 2. 5 LEDs EFFICIENCY vs INPUT VOLTAGE vs DIMMING FREQUENCY AND DUTY CYCLE

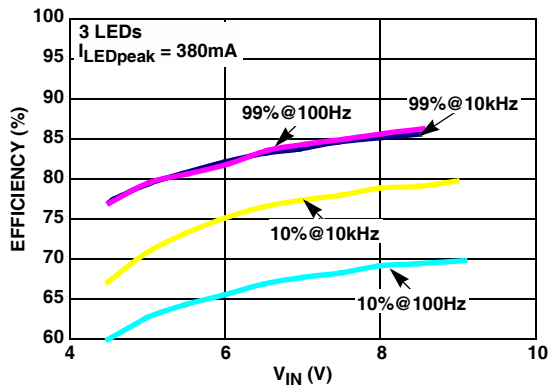


FIGURE 3. 3 LEDs EFFICIENCY vs INPUT VOLTAGE vs DIMMING FREQUENCY AND DUTY CYCLE

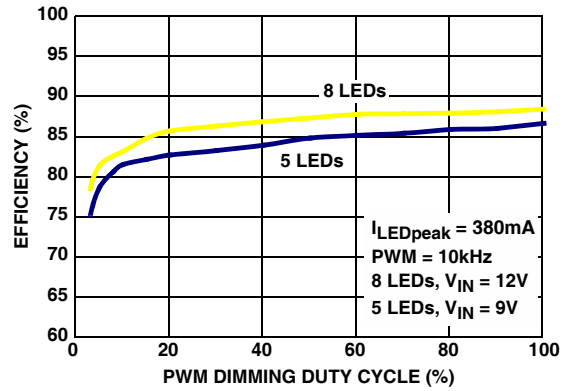


FIGURE 4. 8 AND 5 LEDs EFFICIENCY vs PWM DUTY CYCLE

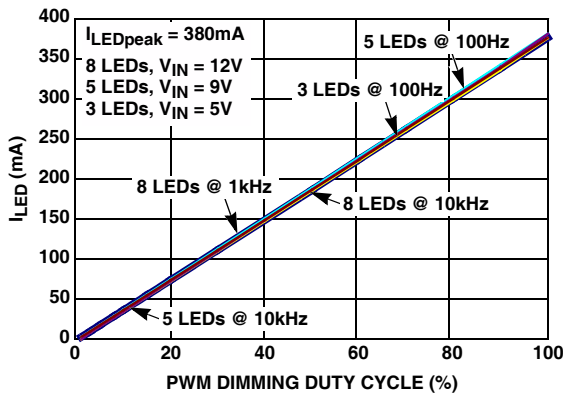


FIGURE 5. LEDs PWM DIMMING LINEARITY

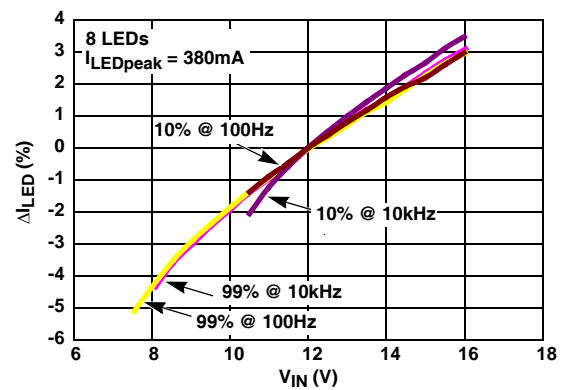


FIGURE 6. 8 LEDs CURRENT ACCURACY vs INPUT VOLTAGE

Typical Performance Curves (Continued)

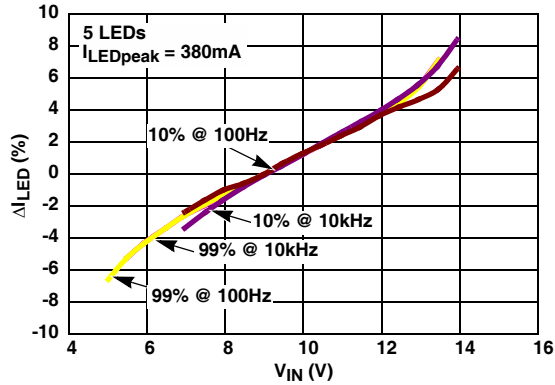


FIGURE 7. 5 LEDs CURRENT ACCURACY vs INPUT VOLTAGE

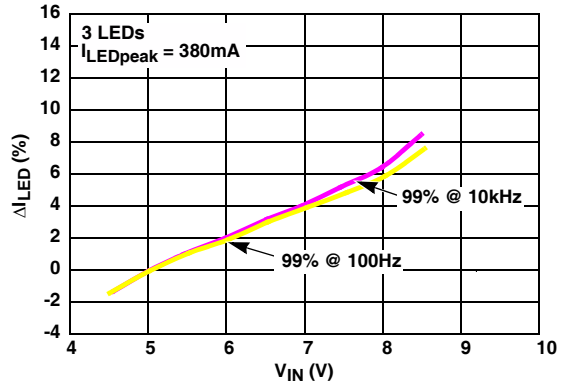


FIGURE 8. 3 LEDs CURRENT ACCURACY vs INPUT VOLTAGE

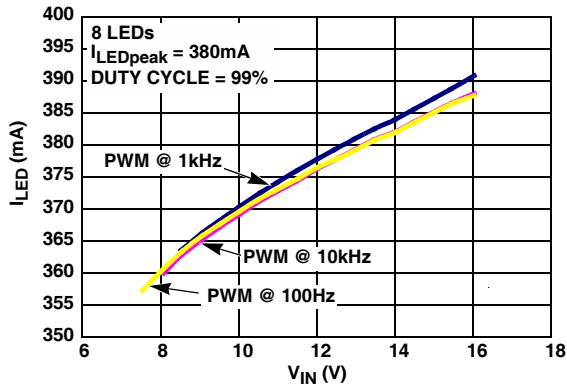


FIGURE 9. 8 LEDs LINE REGULATION OF PWM DUTY CYCLE OF 99%

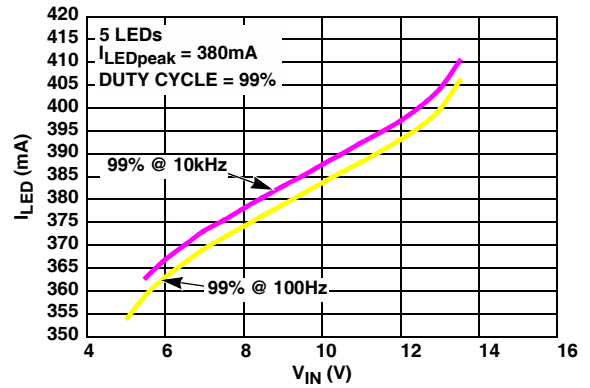


FIGURE 10. 5 LEDs LINE REGULATION OF PWM DUTY CYCLE OF 99%

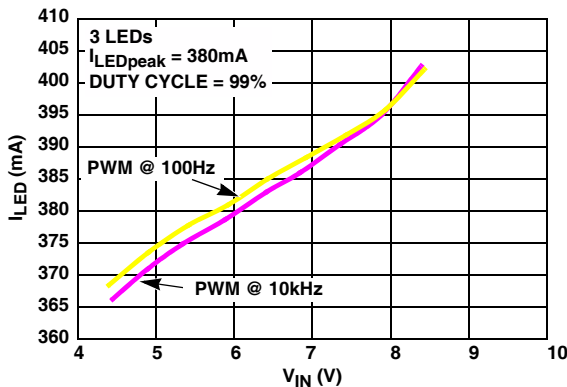


FIGURE 11. 3 LEDs LINE REGULATION OF PWM DUTY CYCLE OF 99%

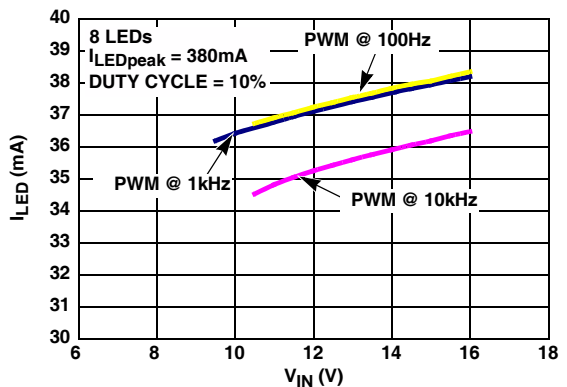


FIGURE 12. 8 LEDs LINE REGULATION OF PWM DUTY CYCLE OF 10%

Typical Performance Curves (Continued)

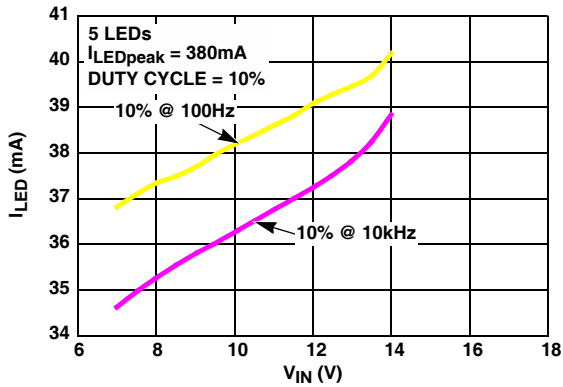


FIGURE 13. 5 LEDs LINE REGULATION OF PWM DUTY CYCLE OF 10%

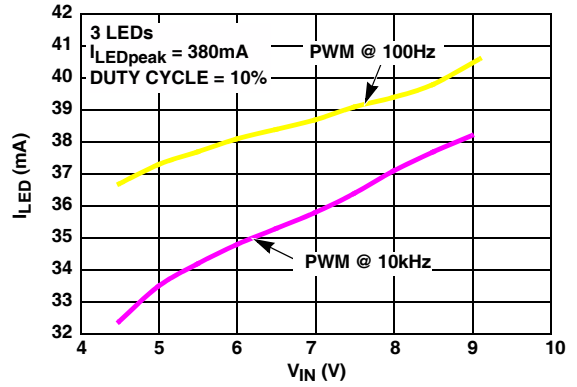


FIGURE 14. 3 LEDs LINE REGULATION OF PWM DUTY CYCLE OF 10%

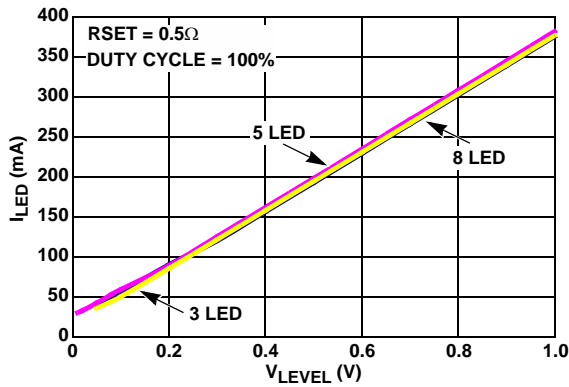


FIGURE 15. LED CURRENT vs  $V_{LEVEL}$  BIAS

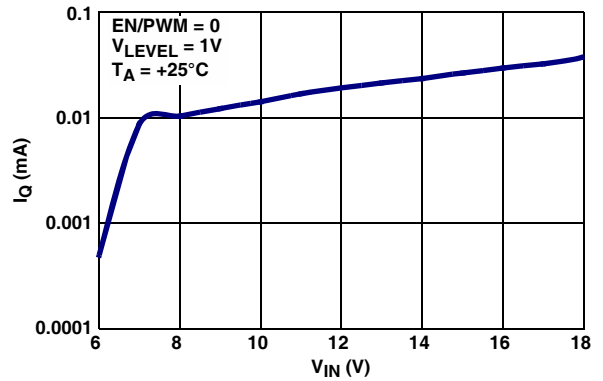


FIGURE 16. QUIESCENT CURRENT (NON-SWITCHING)

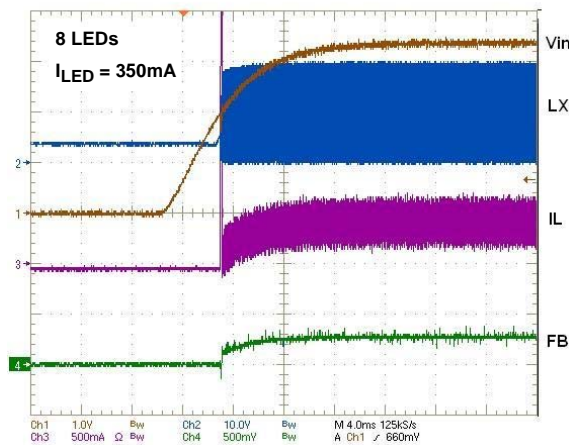


FIGURE 17. START-UP WAVEFORMS

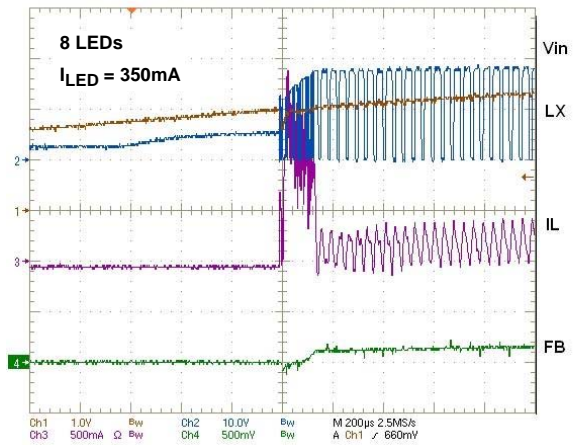


FIGURE 18. START-UP WAVEFORMS ZOOM-IN

Typical Performance Curves (Continued)

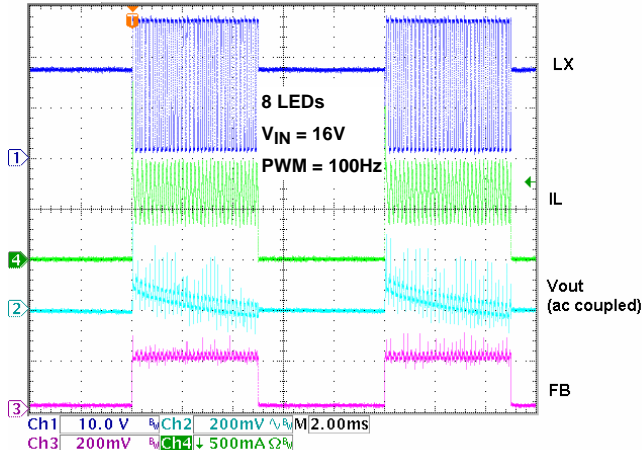


FIGURE 19. 50% PWM DIMMING AT 100Hz

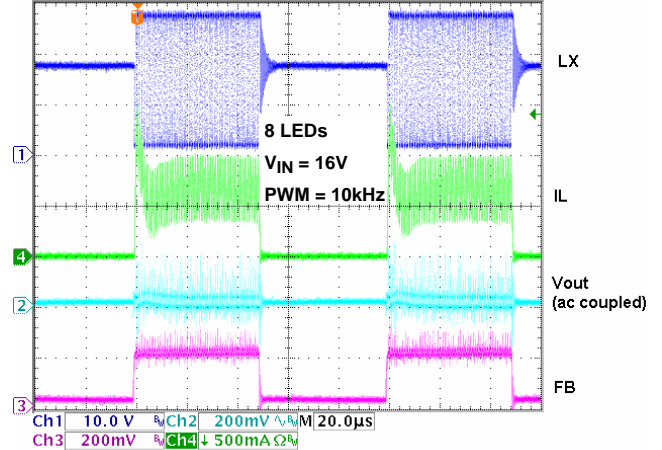


FIGURE 20. 50% PWM DIMMING AT 10kHz

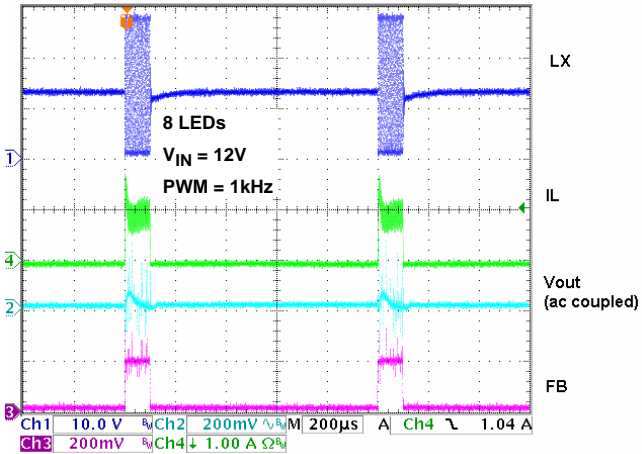


FIGURE 21. 10% PWM DIMMING AT 1kHz

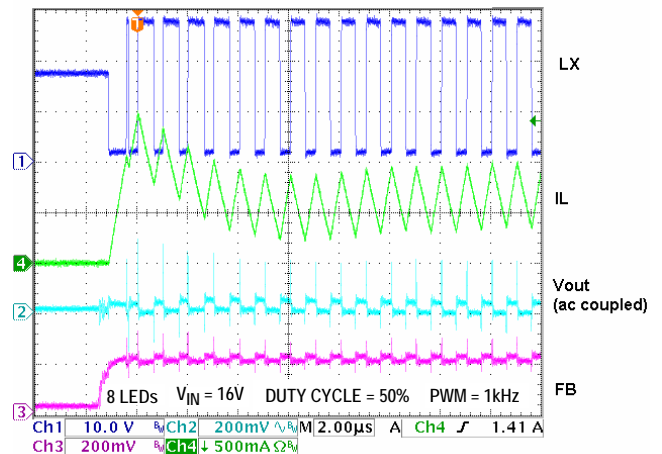


FIGURE 22. 50% PWM DIMMING AT 1kHz ZOOM-IN

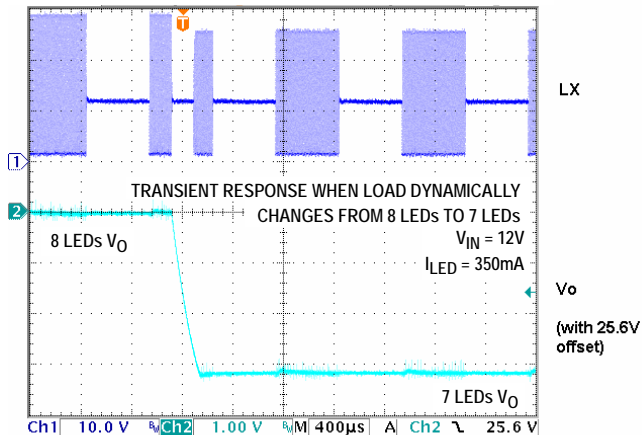


FIGURE 23. TRANSIENT RESPONSE OPERATES FROM 8 TO 7 LEDs

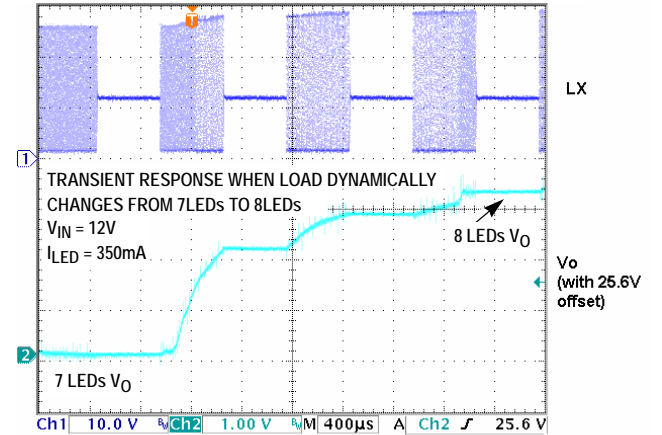


FIGURE 24. TRANSIENT RESPONSE OPERATES FROM 7 TO 8 LEDs



Typical Performance Curves (Continued)

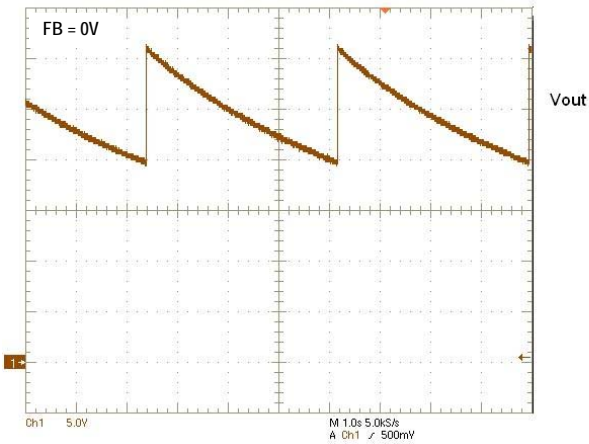


FIGURE 25. OVP AND RESET

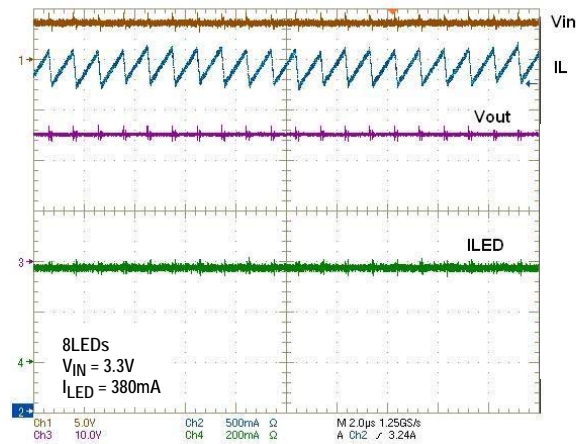


FIGURE 26. CURRENT LIMIT

Typical Boost Mode Application Diagram

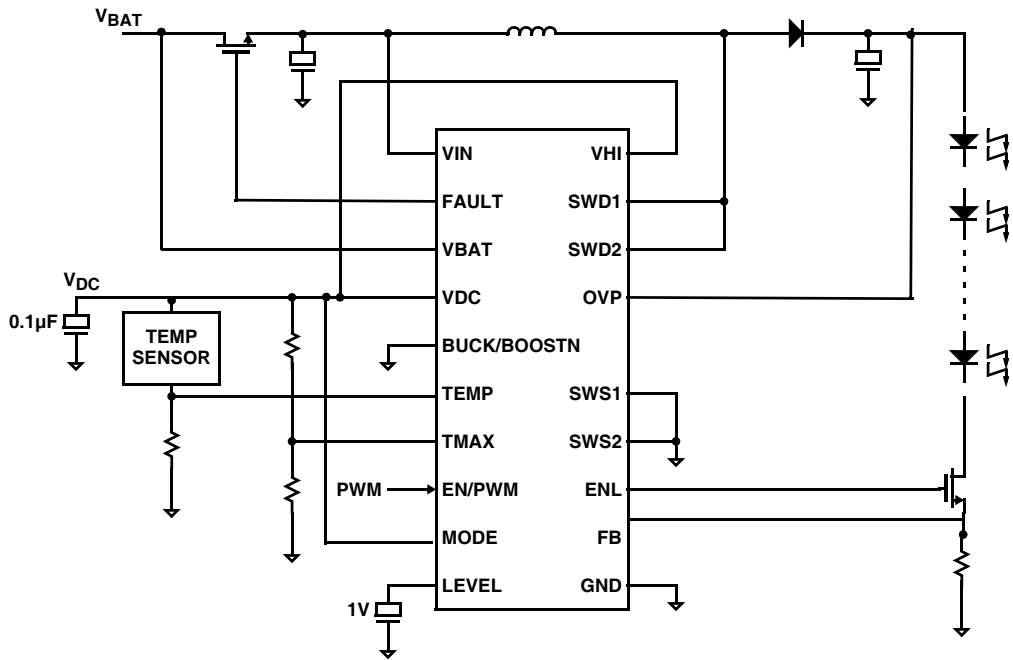


FIGURE 27. TYPICAL BOOST MODE APPLICATION CIRCUIT



**Pin Descriptions**

PIN	NAME	DESCRIPTION
1	VDC	Internally regulated 5V supply, tracks $V_{IN}$ for input voltages less than 5V. LDO output can also be biased with external supply if VIN is <5.5V. A minimum of 3.3 $\mu$ F decoupling capacitor is needed in this pin.
2	VHI	Power FET gate drive supply. Can be biased with external supply if Vin is <5.5V
3	OVP	Overvoltage monitor input; tie to VOUT for normal operation
4	SWD1	NMOS power FET drain
5	SWD2	NMOS power FET drain
6	BUCK/BOOSTN	Tie to GND for BOOST operation and to VDC for Buck operation
7	LEVEL	Sets LED bias current level; $V_{FB}(\text{nominal}) = V_{LEVEL}/5$
8	TEMP	Temperature reference, tie to GND to disable temperature compensation
9	FB	LED current feedback
10	TMAX	Maximum LED temperature set point; if TEMP voltage exceeds TMAX, FB set point will be reduced
11	SWS2	NMOS power FET source
12	SWS1	NMOS power FET source
13	EN/PWM	Chip enable and light modulation PWM dimming input
14	MODE	Digital Input; tie to GND to set FB reference to 400mV, tie to VDC to control FB reference with LEVEL input
15	ENL	LED load isolation MOS gate driver
16	VBAT	Input supply monitor
17	NC	Leave floating (internally connected)
18	GND	Ground return and FB ground reference
19	FAULT	Gate drive of fault protection FET. Driven low under fault conditions
20	VIN	Input supply

Functional Block Diagram

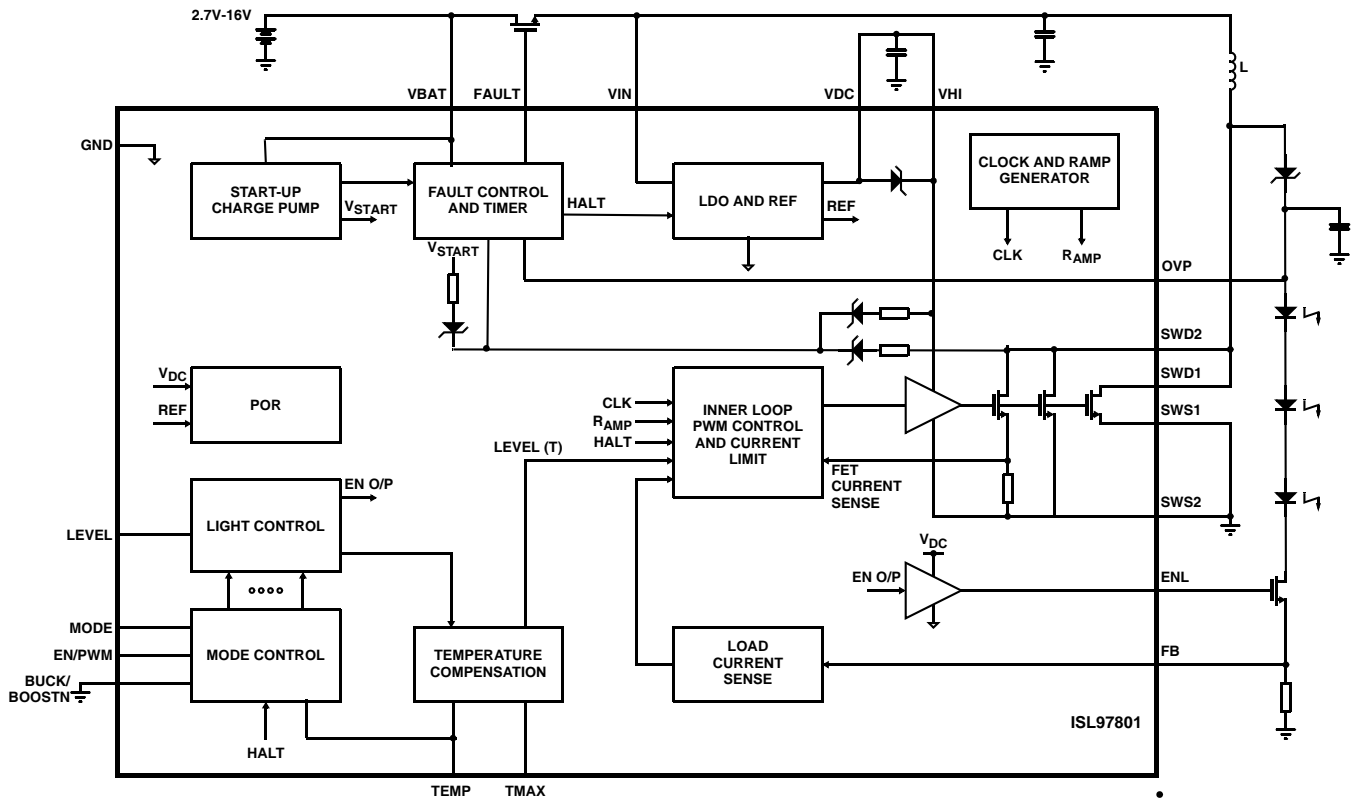


FIGURE 28. ISL97801 BLOCK DIAGRAM

## Theory of Operation

### General Description

The ISL97801 is a flexible, highly integrated high-power LED driver consisting of a PWM switching controller and integrated 36V NDMOS power FET. The device can drive up to 8 series high-power LED's at currents up to 1A at 16V input or 5 LEDs at current up to 350mA at 2.7V input. The control loop can be configured as either as a boost or buck regulator with the configuration of the buck/boost pin, providing an output voltage above or below the input supply voltage, depending on the number of stacked LED's. The controller operates from 2.7V to 16V depending on the numbers of LEDs and current required and can be powered by a single lithium ion battery, 5V or 12V regulated supplies or automotive electrical systems. LED current is sensed through a low value resistor in series with the LED. A thermistor can be used to implement a thermal protection scheme to limit the maximum LED temperature to a preset desirable level.

### Switching Regulator

The ISL97801 employs a current mode PWM control scheme with a nominal switching frequency of 1MHz. This provides fast transient response and enables the use of low profile inductors and compact multilayer ceramic capacitors. Settling time is optimized by the use of a simple control loop without an error amplifier, relying instead on intrinsic gain within the direct summing path. Due to the lower loop gain, offset must be accounted for when setting up initial LED bias current. Refer to the applications section of the datasheet for further information. Figure 28 shows a block diagram of the system.

## Application Configurations

### Operating Modes

The ISL97801 can operate as either a buck or boost regulator. Hardwire BUCK/BOOSTN to GND for boost mode or to VDC for buck mode. In buck mode the power NDMOS drive circuit is "floated" (boot-strapped) allowing the NDMOS gate to be driven above VIN to fully enhance the power NDMOS. An internal Schottky diode between VDC (5V) and VHI reduces external component count. Use a ceramic capacitor of at least 50nF between VHI and SWS1/2 to bootstrap VHI.

### LED Load Connection

ISL97801 includes an auto-sensing FB level shift circuit that enables the LED load to be connected to either GND or VIN. An internal sense circuit monitors the FB pin voltage. When the level exceeds VDC/2, the feedback reference voltage is switched from GND to VIN. Refer to the application section of the datasheet for typical application schematics.

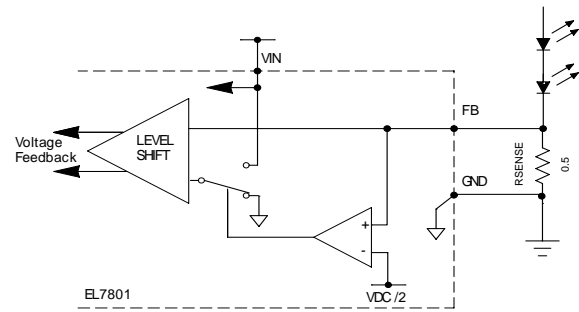


FIGURE 29. FB REFERENCE AUTO SWITCH

### Start-up

To maximize external PWM switching speed, the ISL97801 does not include an internal soft-start circuit. When VDC exceeds the power on reset threshold, switching is delayed for 1ms ( $T_{DELAY}$ ) allowing the output capacitor to charge through the inductor. If soft-start control is required, a suitable application circuit is shown in Figure 30.

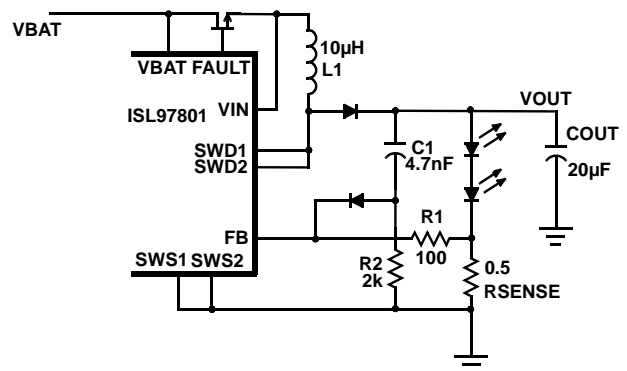


FIGURE 30. EXTERNAL SOFT-START CIRCUIT

### Light Level Control

Two light control schemes are provided:

1. An external PWM signal via the EN/PWM pin, providing low frequency PWM dimming.
2. Bias current level adjustment via the LEVEL input or fixed internal bias.

### PWM Dimming

LED color temperature varies with bias current. In backlighting applications PWM dimming offers better control of color temperature because current through the LED's is kept constant. A 5V gate driver (ENL) synchronized to EN/PWM can be used to control an external N-Ch FET and disconnect the LED stack during the PWM off period. The switch prevents discharge of the output capacitor by the LED load, maintaining a constant bias independent of PWM duty cycle. Operation at 1kHz PWM rate is shown in Figure 31 and Figure 32. The load disconnect switch improves PWM dynamic range, linearity and color temperature control. To

further improve the linearity of PWM dimming, an internal timer delays system shutdown via EN/PWM for 50ms.

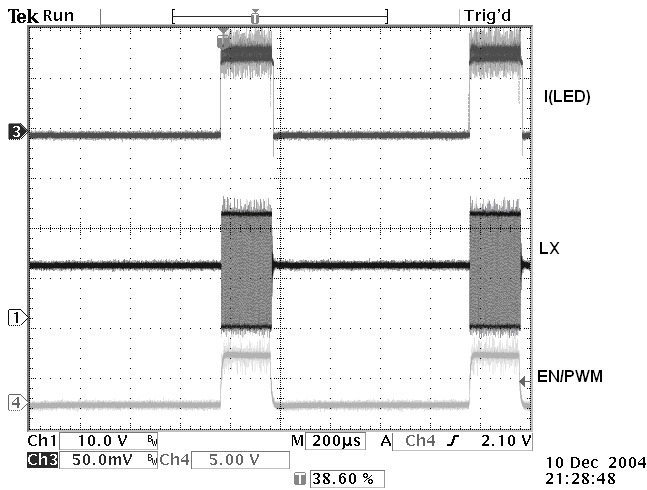


FIGURE 31. OPERATION WITH ENL CONTROLLED FET

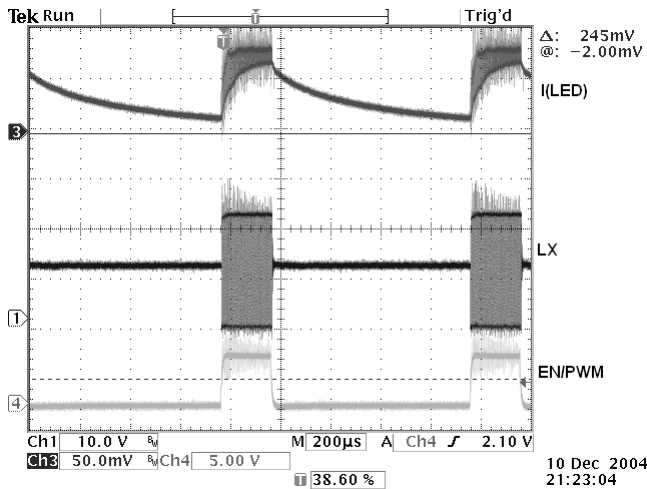


FIGURE 32. OPERATION WITH NO ENL CONTROLLED FET

### Bias Current Dimming

Current in the LED load is determined by the value of the feedback resistor and the target feedback regulation voltage:

$$I_{LED} = \frac{V_{FB}}{R_{SENSE}} \quad (EQ. 1)$$

With MODE tied to VDC, voltage across the feedback resistor is set by  $V_{LEVEL}$ :

$$V_{FB} = \frac{V_{LEVEL}}{5} \quad (EQ. 2)$$

The value of  $V_{FB}$  should be limited to between 50mV and 450mV for linear operation. For minimum light output,  $V_{FB}$  may be set below 50mV. With MODE tied to GND, voltage across the feedback resistor is set at ~400mV via an internal reference. In either operating mode, if LED temperature control is enabled the value of  $V_{FB}$  will be reduced when maximum LED temperature is exceeded.

### Input Overvoltage

For automotive applications, an external high voltage NFET driven by the FAULT pin disconnects the device from the input supply in response to voltage spikes on the input supply. During start-up an internal charge pump drives the FAULT pin above the input voltage, ensuring the NFET is fully enhanced and powering up the device. In normal operation the switching node of the boost regulator or the floating supply of the buck regulator is used to pump FAULT above  $V_{IN}$ . On detection of an overvoltage, the FAULT pin is discharged to GND. The gate to source voltage of the NDMOS is internally limited to  $\pm 15V$  to prevent voltage stress.

### Fault Protection

The external NFET is also used as a fault protection switch, disconnecting the input supply if a fault occurs for more than 50ms. The system monitors feedback voltage regulation, output overvoltage and input overvoltage. For applications not requiring input voltage or fault protection, connect  $V_{BAT}$  and  $V_{IN}$  directly together. All faults except input supply overvoltage latch the ISL97801 into an off state that can be cleared by either power cycling the input supply or the EN/PWM pin. Connecting the TMAX pin to VDC disables the fault latch function (LED over temperature control is also disabled).

### Output Overvoltage Protection (OVP)

If the FB pin is shorted to ground or an LED fails open circuit, output voltage in BOOST mode can increase to potentially damaging voltages. An optional overvoltage protection circuit can be enabled by connection of the OVP pin to the output voltage. The device will stop switching if the output voltage exceeds  $OVP_{H}$  and re-start when the output voltage falls below  $OVP_{L}$ . During sustained OVP fault conditions,  $V_{OUT}$  will saw-tooth between the upper and lower threshold voltages at a frequency determined by the magnitude of current available to discharge the output capacitor and the value of output capacitor used.

The OVP threshold can be set to a lower value by using an external zener diode and resistor, as shown in Figure 33. R1 should be adjusted to minimize offset in the FB voltage due to FB pin input current. A value of  $100\Omega$  is recommended.

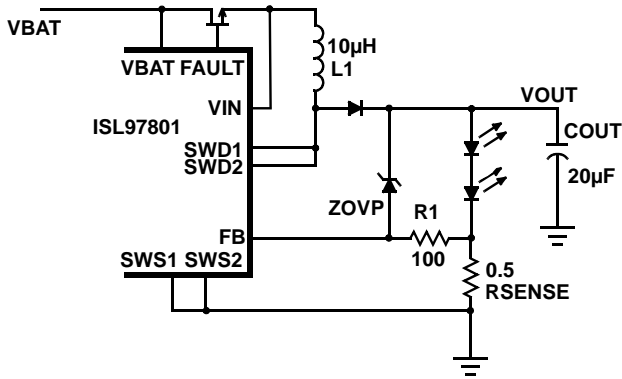


FIGURE 33. EXTERNAL OVP CIRCUIT

### Over Temperature Shutdown

An internal sense circuit disables PWM switching if the die temperature exceeds +135°C. Switching is re-enabled when the temperature falls below +100°C.

### Internal 5V LDO

An internal LDO between VIN and VDC regulates VDC to 5V, to power control and gate drive circuits when VIN exceeds 5.1V. In normal operation decouple VDC with at least 3.3µF. In applications where the input supply is less than 5.5V, VDC should be tied directly to VIN.

### LED Temperature Control

LED lifetime reduces dramatically with elevated temperature. An over temperature control circuit utilizing the thermistor voltage at TEMP reduces the LED bias current when VTEMP exceeds the threshold voltage on TMAX. To minimize noise injection use a potential divider between VDC and GND to set the voltage on TMAX, as shown in Figure 34. The value of TMAX for a specific threshold temperature is determined by the choice of thermistor temperature coefficient. Disable the function by connecting the TMAX pin to VDC and TEMP pin to GND.

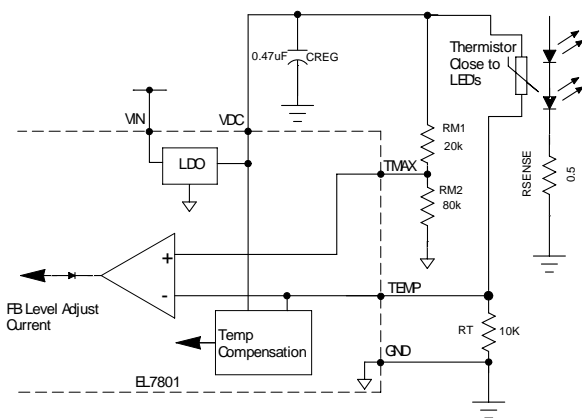


FIGURE 34. OVER-TEMPERATURE CIRCUIT

## Component Selection

### Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

Considerably more input current ripple is generated in buck mode than boost mode. In buck mode input current is alternately switched between  $I_{OUT}$  and zero. The rms current flow in the input capacitor is given by:

$$I_{CAPRMS} = I_{OUT} \cdot \sqrt{(D - D^2)} \quad (\text{EQ. 3})$$

Where: D = Duty Cycle

The input current is maximum for D = 0.5 and when  $I_{OUT}$  approaches current limit (2.4A) giving a value of around 1.2A.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic caps.

In boost mode input current flows continuously into the inductor, with an AC ripple component proportional to the rate of inductor charging only and smaller value input capacitors may be used. It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

In automotive applications the input capacitor can be protected from exposure to high voltages present during fault conditions (load dump) by connecting it downstream of the fault protection switch, as shown in Figures 39 and 40.

### Inductor

Careful selection of inductor value will optimise circuit operation. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability. Internal slope compensation has been optimised for inductor values between 4.7µH and 10µH. Ensure the inductor current rating is capable of handling the current limit value in the configuration used (2.4A for buck, 3.5A for boost). If an inductor core is chosen with too low a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core.

**Rectifier Diode**

A high speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current will minimize losses, making Schottky diodes the preferred choice. Similarly to the inductor, a diode with a suitable current rating to handle current limit in the configuration must be used.

**Output Capacitor**

The output capacitor acts to smooth the output voltage and in the boost configuration supplies load current directly during the conduction phase of the power switch. Ripple voltage consists of two components, the first due to charging and discharging of the capacitor; the second due to IR drop across the ESR of the capacitor by inductor ripple current.

In boost mode:

$$V_{RIPPLE} = \frac{I_O}{C_{OUT}} \times \frac{D}{F_S} + I_{LPK} \times ESR \quad (EQ. 4)$$

where:

$$D = \frac{V_{OUT} - V_{IN}}{V_{OUT}} \quad (EQ. 5)$$

and

$$I_{LPK} = \frac{I_O}{1-D} + \frac{(V_{OUT} - V_{IN})}{2 \times L} \times \frac{(1-D)}{f_s} \quad (EQ. 6)$$

In buck mode:

$$V_{RIPPLE} = \frac{(V_{IN} - V_{OUT}) \times D}{2 \times f_s \times L} \times \left( \frac{D}{f_s \times C_{OUT}} + ESR \right) \quad (EQ. 7)$$

where:

$$D = \frac{V_{OUT}}{V_{IN}} \quad (EQ. 8)$$

For a low ESR ceramic capacitor, output ripple is dominated by the charging and discharging of the output capacitor. Care should be taken to ensure the voltage rating of the capacitor exceeds the maximum output voltage.

**Compensation**

The ISL97801 employs a direct summing control loop with current feedback. No error amplifier is used in the system. The arrangement provides fast transient response and makes use of the output capacitor to compensate the loop. The effect of the pole associated with the inductor is minimized by the current feedback. The number of LEDs, their DC bias current and the value of feedback resistor alter loop stability due to their effect on feedback factor which is heavily influenced by the small signal impedance of the LEDs. Generally, higher numbers of LEDs, lower bias levels and smaller values of feedback resistor will require smaller output capacitors to achieve loop stability. A combination of low ESR electrolytic and ceramic capacitors may be used to reduce implementation costs.

**TABLE 2. BOOST MODE COMPENSATION. 2.7V OPERATION**

VFB	I <sub>OUT</sub>	VOUT (V)	7	10.5	14	17.5	21	24.5	28
		LED's	2	3	4	5	6	7	8
50mV	50mA	Electrolytic	94µF	47µF				DMAX	DMAX
		Ceramic	40µF	20µF	40µF	20µF	20µF		
100mV	100mA	Electrolytic	94µF						
		Ceramic	60µF	60µF	40µF	40µF	40µF		
200mV	350mA	Electrolytic	94µF	47µF	47µF	47µF	ILIM	ILIM	ILIM
		Ceramic	60µF	40µF	40µF	40µF			
200mV	1A	Electrolytic	ILIM	ILIM	ILIM	ILIM	ILIM	ILIM	ILIM
		Ceramic							

**TABLE 3. BOOST MODE COMPENSATION 6V OPERATION**

VFB	I <sub>OUT</sub>	VOUT (V)	7	10.5	14	17.5	21	24.5	28
		LED's	2	3	4	5	6	7	8
50mV	50mA	Electrolytic	94µF	47µF					
		Ceramic	40µF	20µF	40µF	20µF	20µF	20µF	20µF
100mV	100mA	Electrolytic	141µF	47µF					
		Ceramic	60µF	60µF	60µF	40µF	40µF	40µF	40µF
200mV	350mA	Electrolytic	141µF	47µF	47µF				
		Ceramic	60µF	60µF	40µF	60µF	40µF	40µF	40µF
200mV	1A	Electrolytic	94µF	47µF	ILIM	ILIM	ILIM	ILIM	ILIM
		Ceramic	40µF	40µF					

TABLE 4. BOOST MODE COMPENSATION 12V OPERATION

VFB	I <sub>OUT</sub>	VOUT (V)	7	10.5	14	17.5	21	24.5	28
		LED's	2	3	4	5	6	7	8
50mV	50mA	Electrolytic							
		Ceramic	DMIN	DMIN	DMIN	60μF	40μF	40μF	40μF
100mV	100mA	Electrolytic				47μF	47μF		
		Ceramic	DMIN	DMIN	DMIN	40μF	20μF	40μF	40μF
200mV	350mA	Electrolytic				47μF	47μF		
		Ceramic	DMIN	DMIN	DMIN	40μF	20μF	40μF	40μF
200mV	1A	Electrolytic				47μF	47μF		
		Ceramic	DMIN	DMIN	DMIN	20μF	20μF	40μF	40μF

A Note about Ceramic Capacitors:

Many ceramic capacitors have strong voltage and temperature coefficients which reduces effective capacitance as the applied voltage or operating temperature is increased. Pay careful attention when selecting ceramic capacitor type. X5R and X7R families provide much better stability than Y5V, which should generally be avoided unless additional capacitance is added to compensate for the significant changes in value which occurs over voltage and temperature.

TABLE 5. CERAMIC CAPACITOR VARIABILITY

CAPACITOR TYPE	TYPICAL VOLTAGE VARIATION	TEMPERATURE VARIATION
X7R, 10V	-30% at 10V	-15% at +125°C
X5R, 25V	-50% at 25V	-9% at +85°C
Y5V, 6.3V	-90% at 6.3V	-65% at +85°C

## Layout Considerations

PCB layout is very important for the converter to function properly. The following general guidelines should be followed:

- Separate the Power Ground and Signal Ground; connect them only at one point close to the GND pin.
- Maximize the Power Ground area as much as possible. It is essential to ensure the Power Ground return between Cin, Cout, and SWS1,2 as least obstructive as possible.
- Place the input capacitor close to VIN and SWS1,2 pins in boost mode-
- Make the following PC traces as short as possible:
  - from SWD1,2 to the inductor in boost mode
  - from SWS1,2 to the inductor in buck mode
  - from Cout to PGND

- Feedback signals levels are small to improve efficiency. Ensure the reference connection (GND or VIN) between the sense resistor and IC pin doesn't carry switching current.
- Place several via holes (thermal vias) under the chip to a backside ground plane to improve heat dissipation
- Maximize the copper area around the thermal vias to spread heat away from the chip.

## Cost-Sensitive Applications

For cost-sensitive applications, the BOM can be reduced considerably by:

1. Removing temperature compensation
2. Removing the fault-protection switch
3. Removing the load isolation switch
4. Switching the FB into internal fixed bias mode (400mV across V<sub>FB</sub>)

In this configuration, light level may be controlled using the EN/PWM input to modulate the output current.

In the absence of the load isolation switch, LED bias current will vary with PWM duty cycle, due to the discharge of the output capacitor by the LED's during the PWM off time therefore low dimming frequencies can only be used in such application.



**Boost Mode Application Diagram**

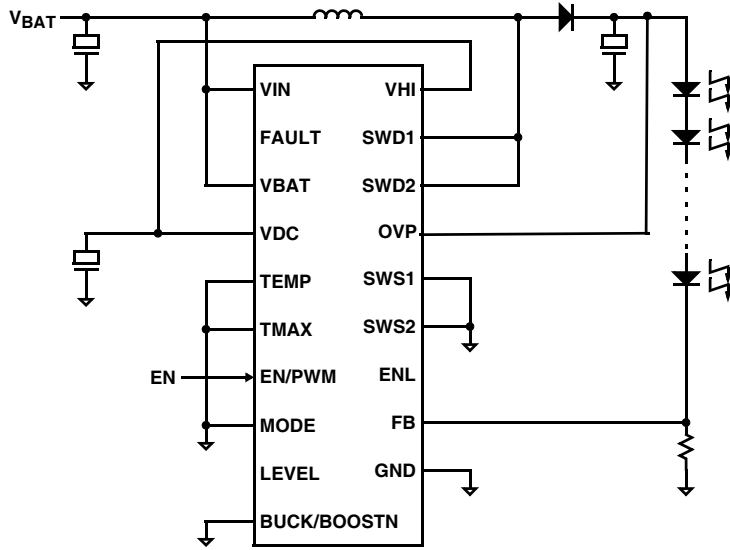


FIGURE 35. BASIC BOOST APPLICATION CIRCUIT

**Boost Mode with Over Current Fault and LED Temperature Protections Application Diagram**

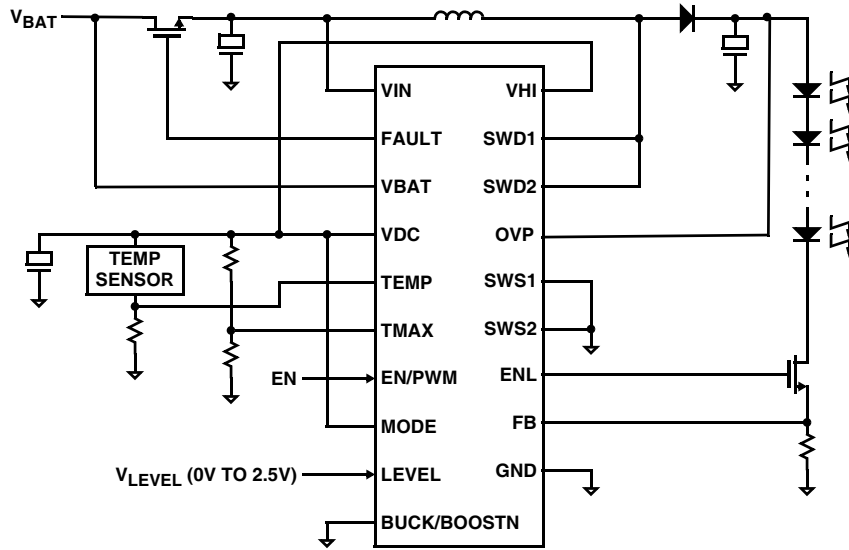


FIGURE 36. BOOST MODE APPLICATION WITH OVER CURRENT FAULT PROTECTION AND LED TEMPERATURE PROTECTION

**Typical Buck Application Diagram**

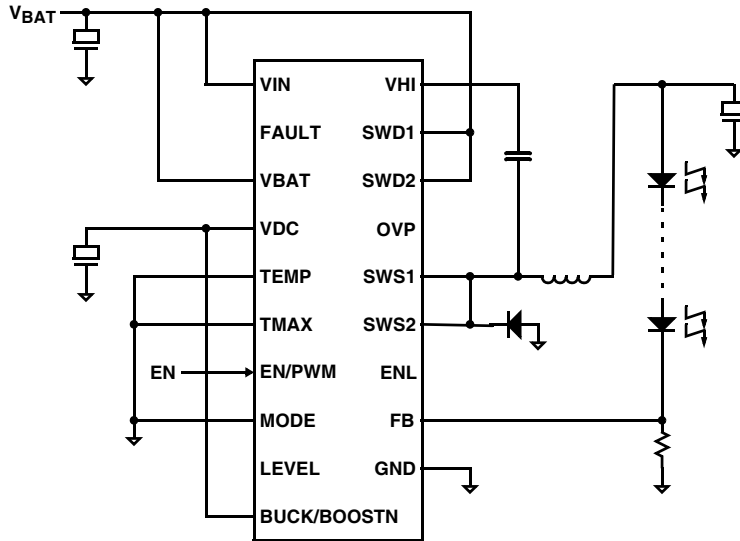


FIGURE 37. BASIC BUCK APPLICATION CIRCUIT

**Buck Mode with Over Current Fault and LED Temperature Protections Application Diagram**

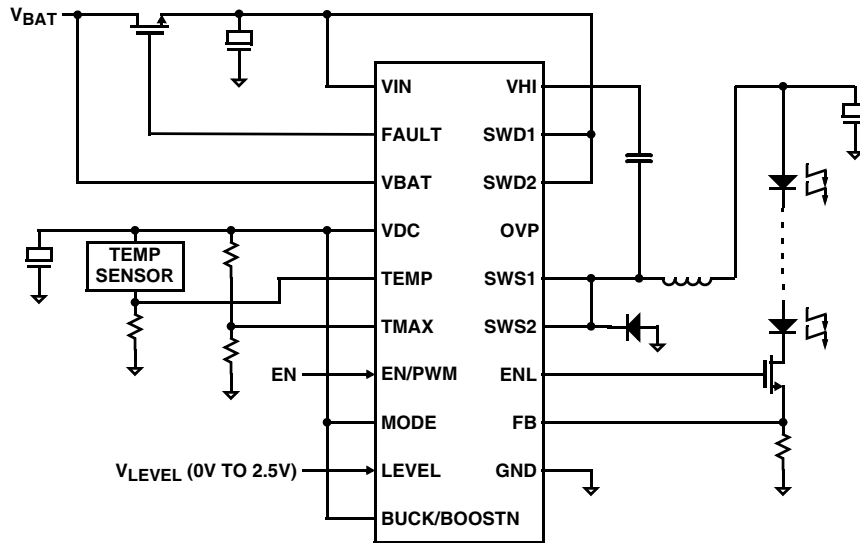


FIGURE 38. BUCK MODE WITH OVER CURRENT FAULT AND LED TEMPERATURE PROTECTIONS APPLICATION

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### Automotive Applications

The LED load and ISL97801 may be protected against load dumps and other electrical faults in automotive supplies with a minor addition to the standard application schematic:

- A reverse transient automotive-rated protection power schottky must be added in series with the input supply
- A 500Ω current limit resistor must be inserted in series with the V<sub>BAT</sub> pin
- The fault protection NFET must be specified to handle 100V VDS conditions.

The protection circuit is applicable to buck, boost, and supply-return load applications.

A small reduction in efficiency is caused by the drop in the power schottky.

Unless alternative transient protection is provided, minimum BOM automotive applications must include the circuit changes noted above.

### Automotive Boost Application Diagram

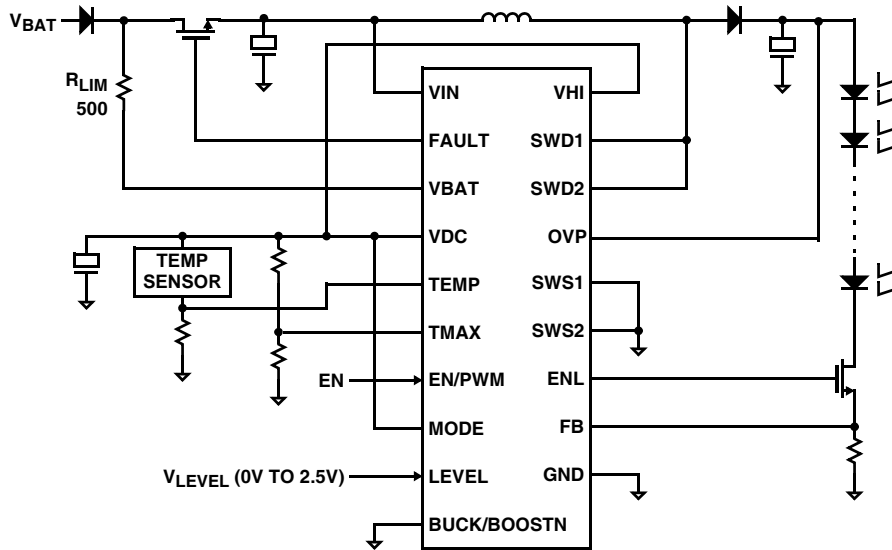


FIGURE 39. AUTOMOTIVE BOOST MODE APPLICATION DIAGRAM

### Automotive Minimum BOM Boost Application Diagram

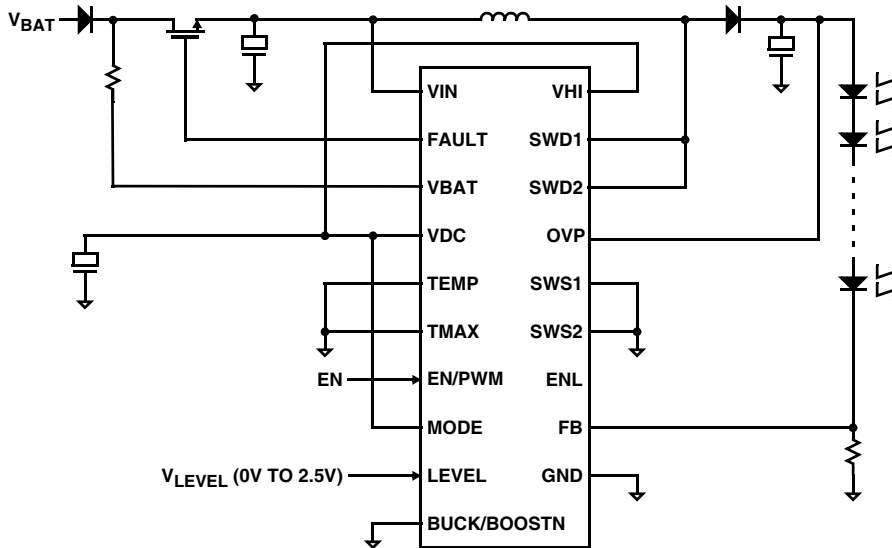


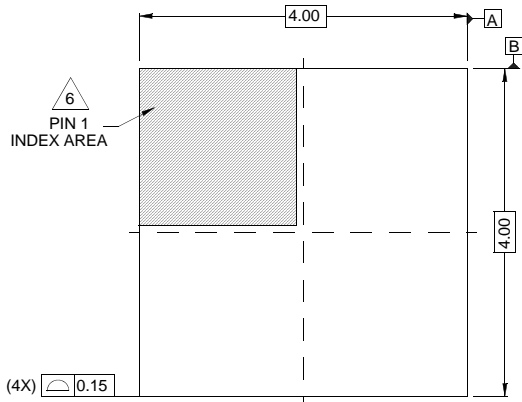
FIGURE 40. AUTOMOTIVE MINIMUM BOM BOOST MODE APPLICATION

# Package Outline Drawing

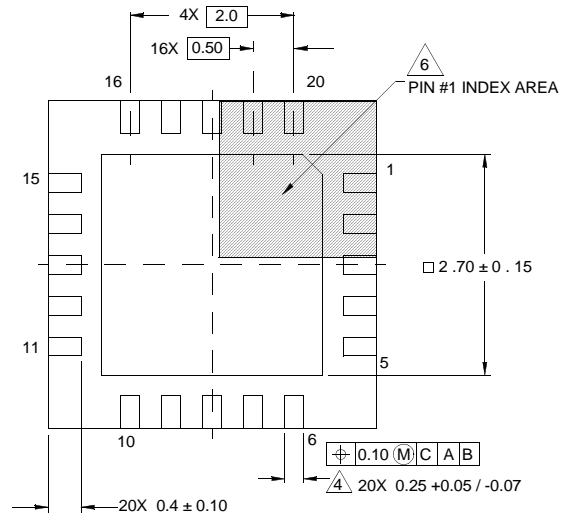
## L20.4x4C

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

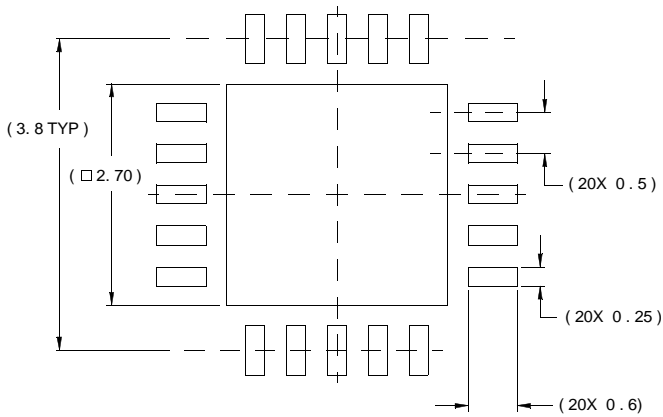
Rev 0, 11/06



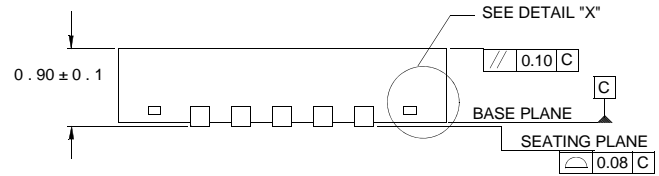
TOP VIEW



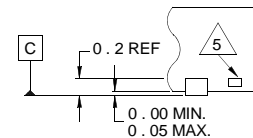
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

### NOTES:

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal  $\pm 0.05$
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.