National Semiconductor

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LM3509
High Efficiency Boost for White LED's and/or OLED Displays with Dual Current Sinks and I²C Compatible Brightness Control

General Description

The LM3509 current mode boost converter offers two separate outputs. The first output (MAIN) is a constant current sink for driving series white LED's. The second output (SUB/FB) is configurable as a constant current sink for series white LED bias, or as a feedback pin to set a constant output voltage for powering OLED panels.

When configured as a dual output white LED bias supply, the LM3509 adaptively regulates the supply voltage of the LED strings to maximize efficiency and insure the current sinks remain in regulation. The maximum current per output is set via a single external low power resistor. An I²C compatible interface allows for independent adjustment of the LED current in either output from 0 to max current in 32 exponential steps. When configured as a white LED + OLED bias supply the LM3509 can independently and simultaneously drive a string of up to 5 white LED's and deliver a constant output voltage of up to 21V for OLED panels.

Output over-voltage protection shuts down the device if V_{OUT} rises above 21V allowing for the use of small sized low voltage output capacitors. The LM3509 is offered in a small 10-pin thermally- enhanced LLP package and operates over the -40°C to +85°C temperature range.

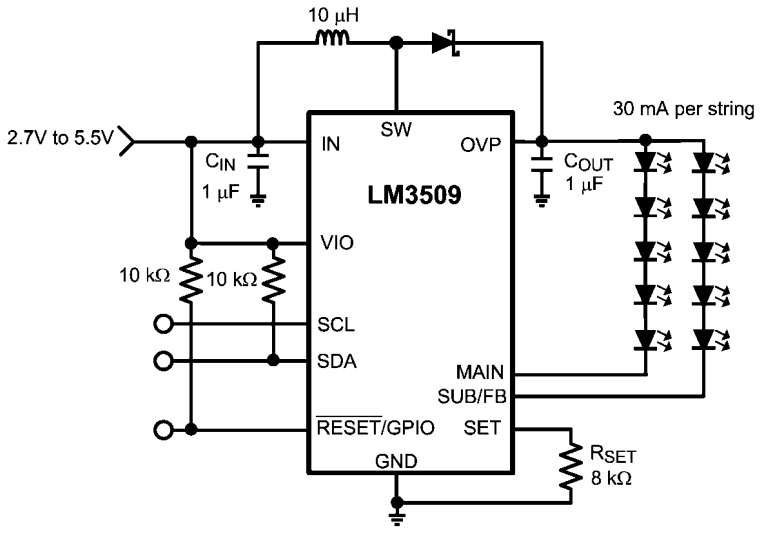
Features

- Integrated OLED Display Power Supply and LED Driver
- Drives up to 10 LED's at 30mA
- Drives up to 5 LED's at 20mA and delivers up to 21V at 40mA
- Over 90% Efficient
- 32 Exponential Dimming Steps
- 0.15% Accurate Current Matching Between Strings
- Internal Soft-Start Limits Inrush Current
- True Shutdown Isolation for LED's
- Wide 2.7V to 5.5V Input Voltage Range
- 21V Over-Voltage Protection
- 1.27MHz Fixed Frequency Operation
- Low Profile 10-pin LLP Package (3mm x 3mm x 0.8mm)
- General Purpose I/O
- Active Low Hardware Reset

Applications

- Dual Display LCD Backlighting for Portable Applications
- Large Format LCD Backlighting
- OLED Panel Power Supply

Typical Application Circuits



Dual White LED Bias Supply

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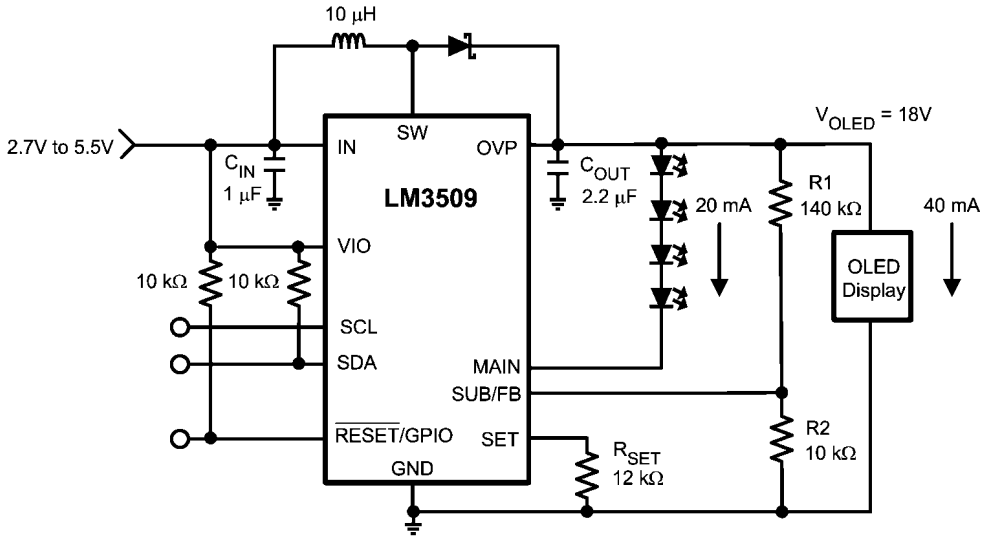

OLED Panel Power Supply

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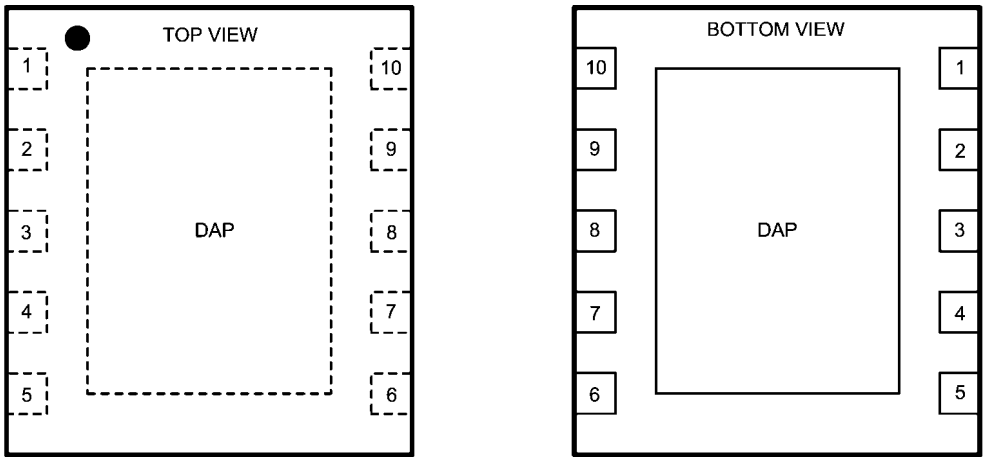
Connection Diagram

Top View



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10-Pin LLP (3mm × 3mm × 0.8mm)

Ordering Information

Order Number	Package Type	NSC Package Drawing	Top Mark	Supplied As
LM3509SD	10-Pin LLP	SDA010A	L3509	1000 units, Tape-and-Reel, No-Lead
LM3509SDX	10-Pin LLP	SDA010A	L3509	4500 units, Tape-and-Reel, No Lead

Pin Descriptions/Functions

Pin	Name	Function
1	MAIN	Main Current Sink Input.
2	SUB/FB	Secondary Current Sink Input or 1.25V Feedback Connection for Constant Voltage Output.
3	SET	LED Current Setting Connection. Connect a resistor from SET to GND to set the maximum LED current into MAIN or SUB/FB (when in LED mode), where I_{LED_MAX} = 192×1.244V/R_{SET}.
4	VIO	Logic Voltage Level Input
5	$\overline{\text{RESET}}$/GPIO	Active Low Hardware Reset and Programmable General Purpose I/O.
6	SW	Drain Connection for Internal NMOS Switch
7	OVP	Over-Voltage Protection Sense Connection. Connect OVP to the positive terminal of the output capacitor.
8	IN	Input Voltage Connection. Connect IN to the input supply, and bypass to GND with a 1µF ceramic capacitor.
9	SDA	Serial Data Input/Output
10	SCL	Serial Clock Input
DAP	GND	Ground

Absolute Maximum Ratings (Notes 1, 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

V_{IN}	−0.3V to 6V
V_{SW}, V_{OVP},	−0.3V to 25V
$V_{SUB/FB}$, V_{MAIN}	−0.3V to 23V
V_{SCL}, V_{SDA}, $V_{\overline{RESET}\backslash GPIO}$, V_{IO} , V_{SET}	−0.3V to 6V
Continuous Power Dissipation	Internally Limited
Junction Temperature (T_{J-MAX})	+150ºC
Storage Temperature Range	-65ºC to +150º C
Maximum Lead Temperature (Soldering, 10s)(Note 3)	+300°C
ESD Rating(Note 10) Human Body Model	2.5kV

Operating Ratings (Notes 1, 2)

V_{IN}	2.7V to 5.5V
V_{SW}, V_{OVP},	0V to 23V
$V_{SUB/FB}$, V_{MAIN}	0V to 21V
Junction Temperature Range (T_J)(Note 4)	-40ºC to +110ºC
Ambient Temperature Range (T_A)(Note 5)	-40ºC to +85ºC

Thermal Properties

Junction to Ambient Thermal Resistance (θ_{JA})(Note 6)	54°C/W

ESD Caution Notice

National Semiconductor recommends that all integrated circuits be handled with appropriate ESD precautions. Failure to observe proper ESD handling techniques can result in damage to the device.

Electrical Characteristics

Specifications in standard type face are for T_A = 25°C and those in **boldface type** apply over the Operating Temperature Range of T_A = −40°C to +85°C. Unless otherwise specified V_{IN} = 3.6V, V_{IO} = 1.8V, $V_{\overline{RESET}/GPIO}$ = V_{IN}, $V_{SUB/FB}$ = V_{MAIN} = 0.5V, R_{SET} = 12.0kΩ, OLED = '0', ENM = ENS = '1', BSUB = BMAIN = Full Scale.(Notes 2, 7)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{LED}	Output Current Regulation MAIN or SUB/FB Enabled	UNI = '0', or '1'	**18.6**	20	**21.8**	mA
	Maximum Current Per Current Sink	R_{SET} = 8.0kΩ		30		
$I_{LED-MATCH}$	I_{MAIN} to $I_{SUB/FB}$ Current Matching	UNI = '1' (Note 11)		0.15	**1**	%
V_{SET}	SET Pin Voltage	3.0V < V_{IN} < 5V		1.244		V
I_{LED}/I_{SET}	I_{LED} Current to I_{SET} Current Ratio			192		
V_{REG_CS}	Regulated Current Sink Headroom Voltage			500		mV
V_{REG_OLED}	$V_{SUB/FB}$ Regulation Voltage in OLED Mode	3.0V < V_{IN} < 5.5V, OLED = '1'	**1.172**	1.21	**1.239**	V
V_{HR}	Current Sink Minimum Headroom Voltage	I_{LED} = 95% of nominal		300		mV
R_{DSON}	NMOS Switch On Resistance	I_{SW} = 100mA		0.58		Ω
I_{CL}	NMOS Switch Current Limit	V_{IN} = 3.0V	**650**	770	**875**	mA
V_{OVP}	Output Over-Voltage Protection	ON Threshold	**21.2**	22	**22.9**	V
		OFF Threshold	**19.7**	20.6	**21.2**	
f_{SW}	Switching Frequency		**1.0**	1.27	**1.4**	MHz
D_{MAX}	Maximum Duty Cycle			90		%
D_{MIN}	Minimum Duty Cycle			10		%
I_Q	Quiescent Current, Device Not Switching	V_{MAIN} and $V_{SUB/FB}$ > V_{REG_CS}, BSUB = BMAIN = 0x00		400	**440**	µA
		$V_{SUB/FB}$ > V_{REG_OLED}, OLED='1', ENM=ENS='0'		250	**305**	
I_{SHDN}	Shutdown Current	ENM = ENS = OLED = '0'		3.6	**5**	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$\overline{\text{RESET}}$/GPIO Pin Voltage Specifications						
V_{IL}	Input Logic Low	2.7V < V_{IN} <5.5V, MODE bit = 0			**0.5**	V
V_{IH}	Input Logic High	2.7V < V_{IN} < 5.5V, MODE bit = 0	**1.1**			V
V_{OL}	Output Logic Low	I_{LOAD}=3mA, MODE bit = 1			**400**	mV
I²C Compatible Voltage Specifications (SCL, SDA, VIO)						
V_{IO}	Serial Bus Voltage Level	2.7V < V_{IN} < 5.5V (Note 9)	**1.4**		**V_{IN}**	V
V_{IL}	Input Logic Low	2.7V < V_{IN} < 5.5V			**0.36×V_{IO}**	V
V_{IH}	Input Logic High	2.7V < V_{IN} < 5.5V	**0.7×V_{IO}**		**V_{IO}**	V
V_{OL}	Output Logic Low	I_{LOAD} = 3mA			**400**	mV
I²C Compatible Timing Specifications (SCL, SDA, VIO, see Figure 1) (Notes 8, 9)						
t_1	SCL Clock Period		**2.5**			µs
t_2	Data In Setup Time to SCL High		**100**			ns
t_3	Data Out Stable After SCL Low		**0**			ns
t_4	SDA Low Setup Time to SCL Low (Start)		**100**			ns
t_5	SDA High Hold Time After SCL High (Stop)		**100**			ns

Note 1: Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be guaranteed. For guaranteed specifications and test conditions, see the Electrical Characteristics.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: For detailed soldering specifications and information, please refer to National Semiconductor Application Note 1187: Leadless Lead frame Package (AN-1187).

Note 4: Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J=150ºC (typ.) and disengages at T_J=140ºC (typ.).

Note 5: In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature (TJ-MAX-OP = +105ºC), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} - (\theta_{JA} \times P_{D-MAX})$.

Note 6: Junction-to-ambient thermal resistance (θ_{JA}) is taken from a thermal modeling result, performed under the conditions and guidelines set forth in the JEDEC standard JESD51-7. The test board is a 4-layer FR-4 board measuring 114mm x 76mm x 1.6mm with a 2x1 array of thermal vias. The ground plane on the board is 113mm x 75mm. Thickness of copper layers are 71.5µm/35µm/35µm/71.5µm (2oz/1oz/1oz/2oz). Ambient temperature in simulation is 22°C, still air. Power dissipation is 1W. The value of θ_{JA} of this product in the LLP package could fall in a range as wide as 50ºC/W to 150ºC/W (if not wider), depending on board material, layout, and environmental conditions. In applications where high maximum power dissipation exists special care must be paid to thermal dissipation issues. For more information on these topics, please refer to Application Note 1187: Leadless Leadframe Package (LLP) and the Power Efficiency and Power Dissipation section of this datasheet.

Note 7: Min and Max limits are guaranteed by design, test, or statistical analysis. Typical (Typ) numbers are not guaranteed, but represent the most likely norm.

Note 8: SCL and SDA must be glitch-free in order for proper brightness control to be realized.

Note 9: SCL and SDA signals are referenced to VIO and GND for minimum VIO voltage testing.

Note 10: The human body model is a 100pF capacitor discharged through 1.5kΩ resistor into each pin. (MIL-STD-883 3015.7).

Note 11: The matching specification between MAIN and SUB is calculated as 100 × ((I_{MAIN} or I_{SUB}) - I_{AVE}) / I_{AVE}. This simplifies out to be 100 × (I_{MAIN} - I_{SUB})/(I_{MAIN} + I_{SUB}).

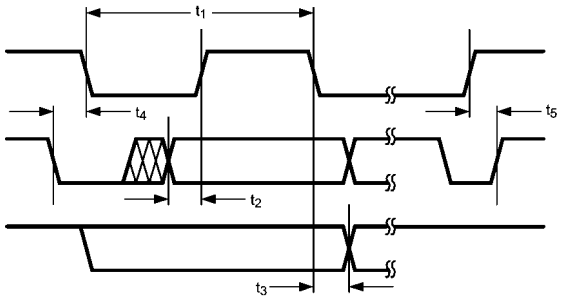
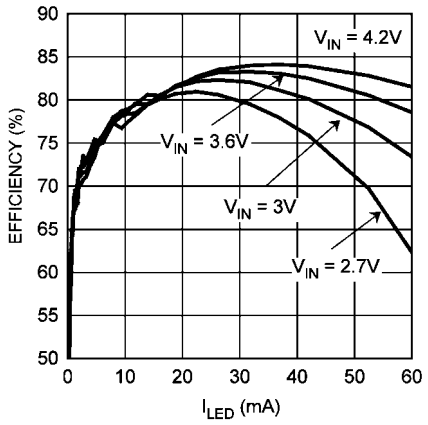


FIGURE 1. I²C Timing

Typical Performance Characteristics

V_{IN} = 3.6V, LEDs are OSRAM (LW M67C), C_{OUT} = 1µF (LED Mode), C_{OUT} = 2.2µF (OLED Mode), C_{IN} = 1µF, L = TDK VLF4012AT-100MR79, (R_L = 0.3Ω), R_{SET} = 8.06kΩ, UNI = '1', I_{LED} = I_{SUB} + I_{MAIN}, T_A = +25°C unless otherwise specified.

10 LED Efficiency vs I_{LED} (2 Strings of 5LEDs)



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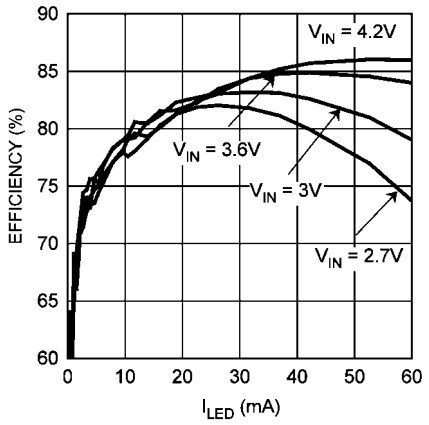
8 LED Efficiency vs I_{LED} (2 Strings of 4LEDs)



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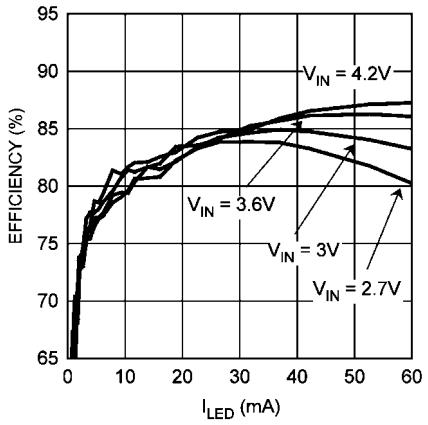
6 LED Efficiency vs I_{LED} (2 Strings of 3LEDs)



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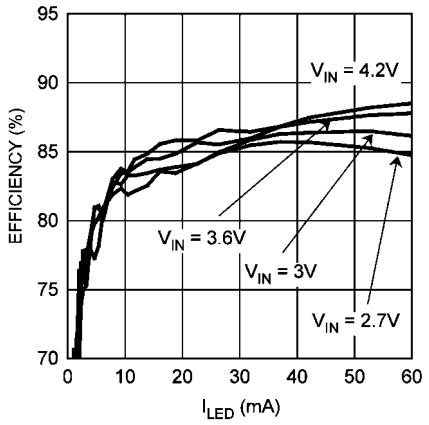
4 LED Efficiency vs I_{LED} (2 Strings of 2LEDs)



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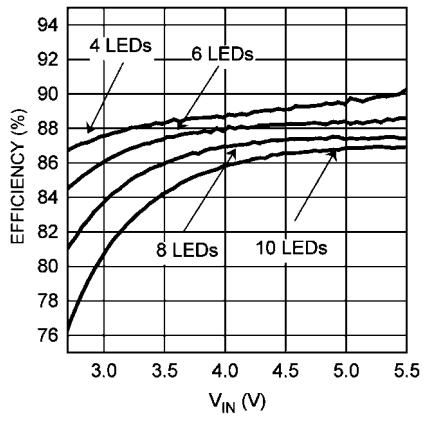
LED Efficiency vs V_{IN} (L = TDK VLF3012AT-100MR49, R_L = 0.36Ω, I_{LED} = 40mA)



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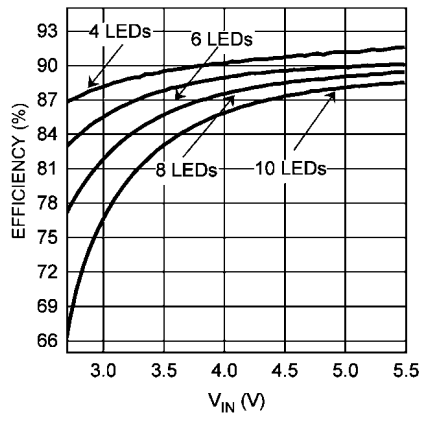
LED Efficiency vs V_{IN} (L = TDK VLF5014AT-100MR92, R_L = 0.2Ω, I_{LED} = 60mA)



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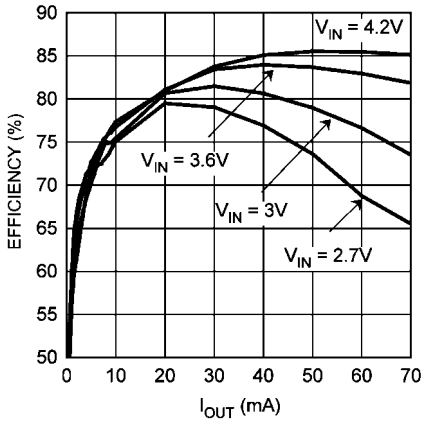
18V OLED Efficiency vs I_{OUT}



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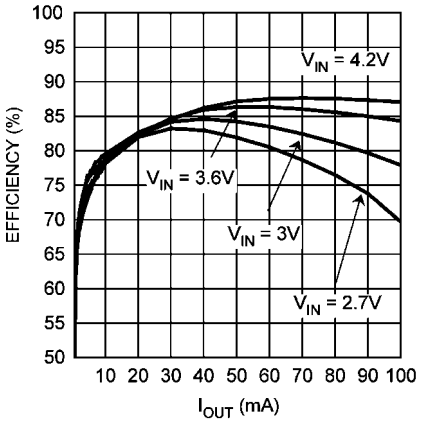
12V OLED Efficiency vs I_{OUT}



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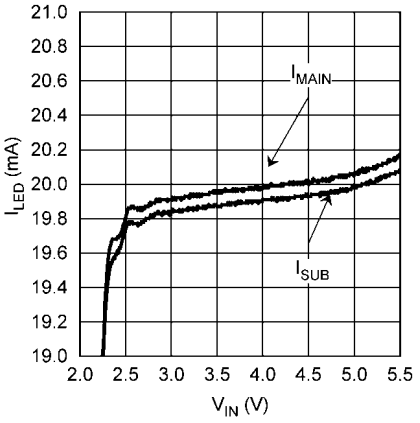
LED Line Regulation (UNI = '0')



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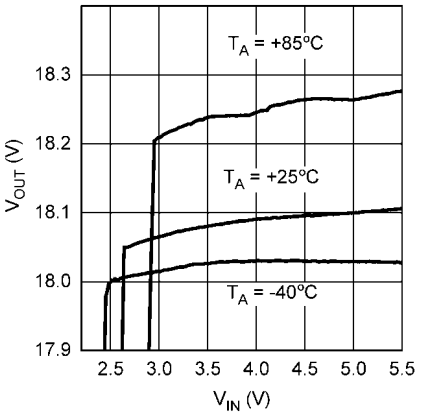
OLED Line Regulation I_{OLED} = 60mA



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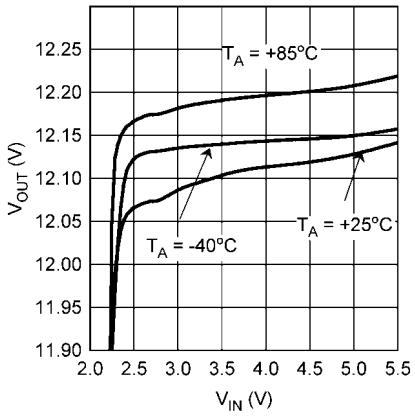
OLED Line Regulation I_{OLED} = 60mA



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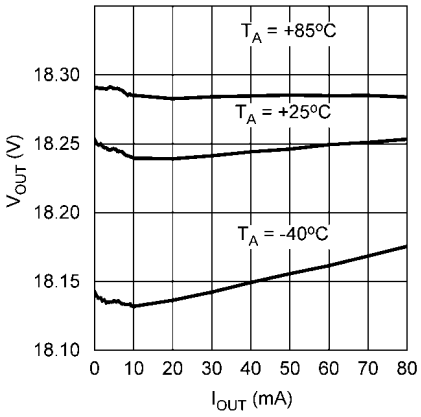
OLED Load Regulation V_{OLED} = 18V



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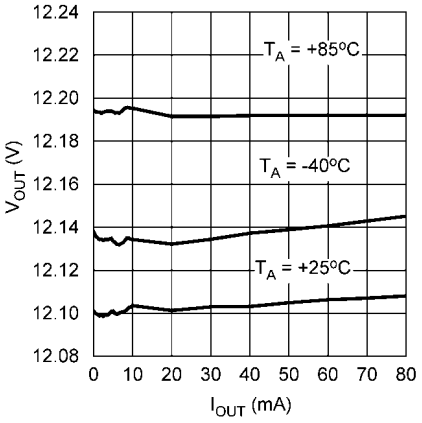
OLED Load Regulation
V_{OLED} = 12V



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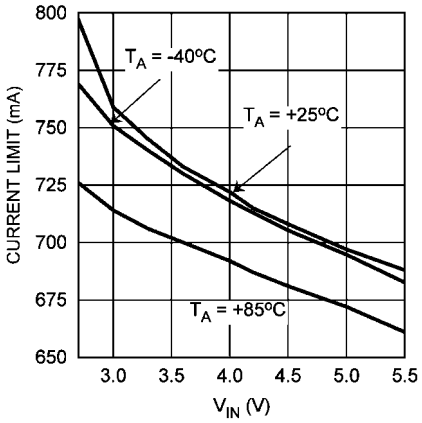
Peak Current Limit vs. V_{IN}



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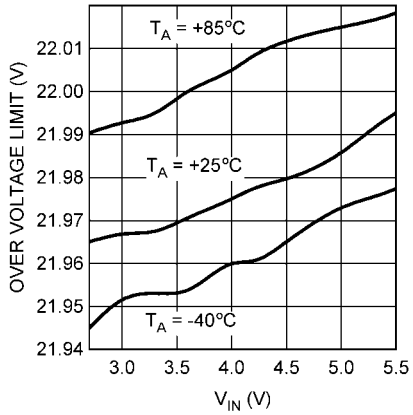
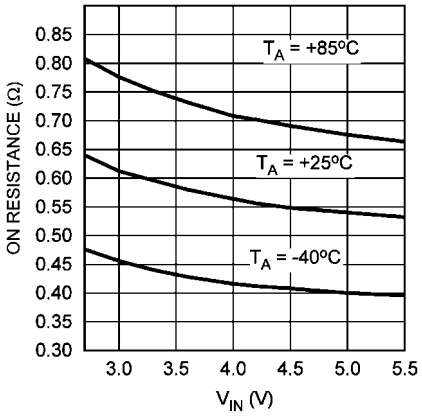
Over Voltage Limit vs. V_{IN}



30004315

Switch On-Resistance vs. V_{IN}



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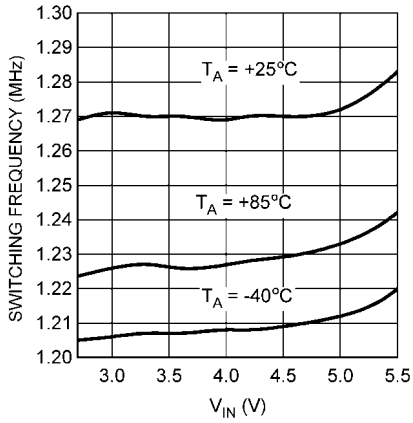
Switching Frequency vs. V_{IN}



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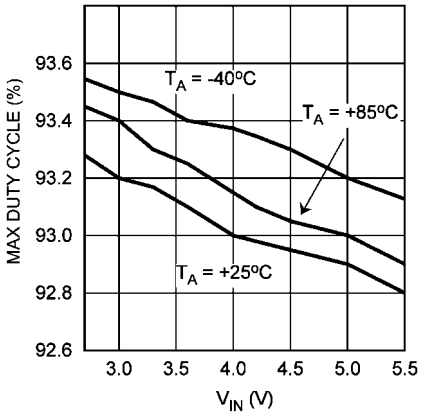
Maximum Duty Cycle vs. V_{IN}



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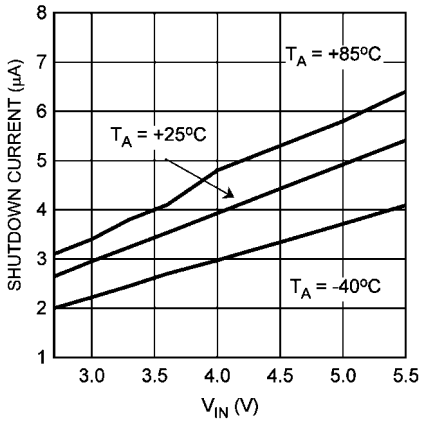
Shutdown Current vs. V_{IN}



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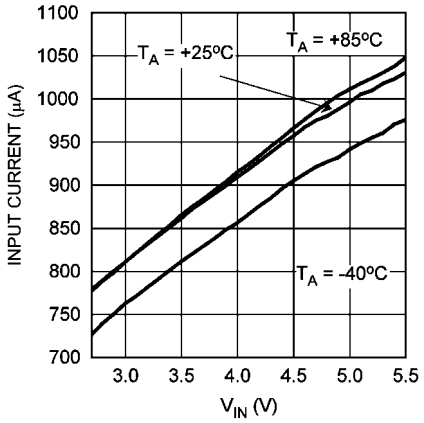
Switching Supply Current vs. V_{IN}



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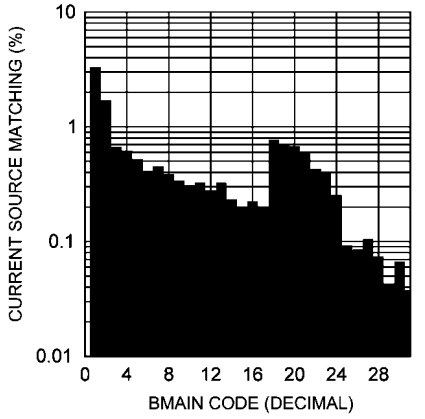
LED Current Matching vs. CODE (Note 11)
(UNI = '1', R_{SET} = 12kΩ, T_A = -40°C to +85°C)



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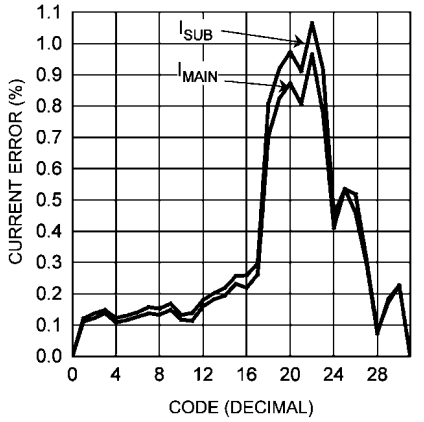
LED Current Accuracy vs CODE
(R_{SET} = 12kΩ±0.05%)



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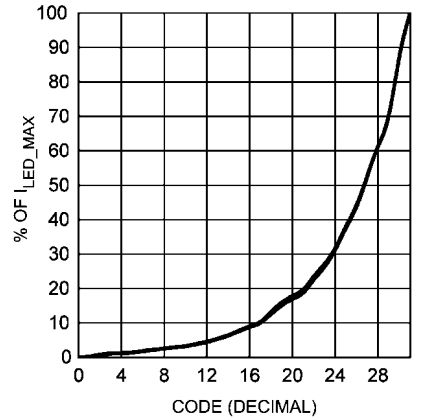
LED Current vs CODE
(I_{MAIN}, I_{SUB}, I_{IDEAL}, R_{SET} = 12kΩ±0.05%)



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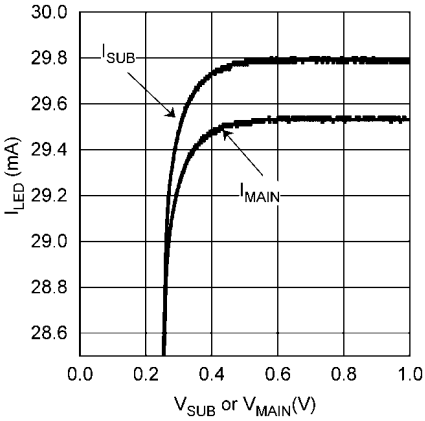
I_{LED} vs Current Source Headroom Voltage
(V_{IN} = 3V, UNI = '0')



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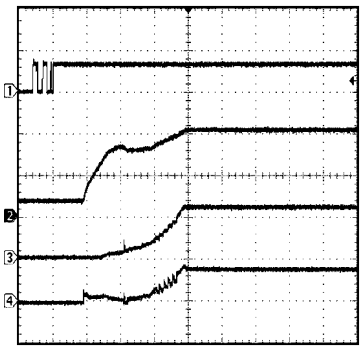
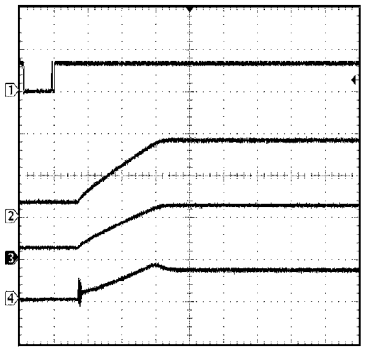
Start-Up Waveform (LED Mode)
(2 × 5 LEDs, 30mA per string)



30004325

Channel 1: SDA (5V/div)
Channel 2: V_{OUT} (10V/div)
Channel 3: I_{LED} (50mA/div)
Channel 4: I_{IN} (500mA/div)
Time Base: 400µs/div

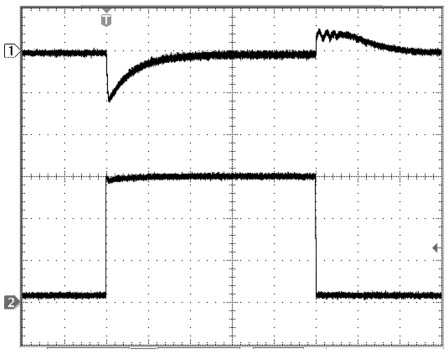
Start-Up Waveform (OLED Mode)
(V_{OUT} = 18V, I_{OUT} = 60mA)



30004327

Channel 1: SDA (5V/div)
Channel 2: V_{OUT} (10V/div)
Channel 3: I_{OUT} (50mA/div)
Channel 4: I_{IN} (500mA/div)
Time Base: 400µs/div

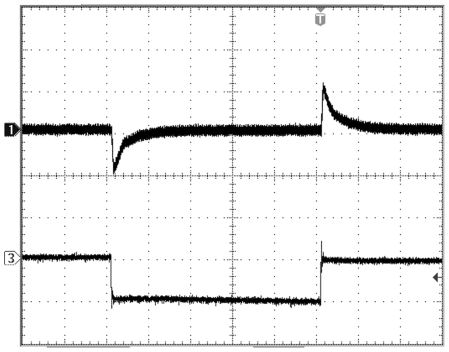
Load Step (OLED Mode)
(V_{OUT} = 18V, C_{OUT} = 2.2µF)



30004326

Channel 1: V_{OUT} (AC Coupled, 500mV/div)
Channel 2: I_{OUT} (20mA/div)
Time Base: 200µs/div

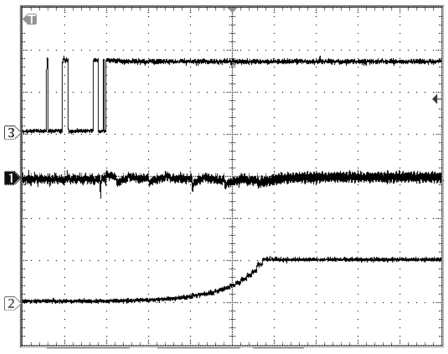
Line Step (LED Mode)
(2 × 5 LEDs, 30mA per String, C_{OUT} = 1µF)



30004354

Channel 1: V_{OUT} (AC Coupled, 500mV/div)
Channel 2: V_{IN} (AC Coupled, 500mV/div)
Time Base: 200µs/div

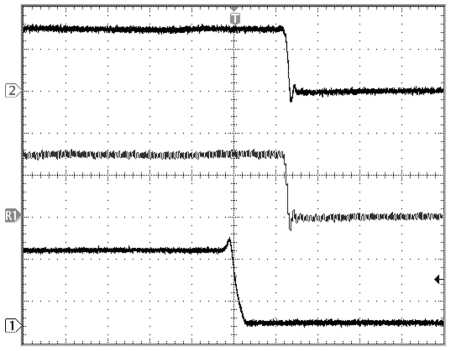
Transition From OLED to OLED + 1 × 4 LED)
(V_{OUT} = 18V, I_{OUT} = 40mA, I_{LED} = 20mA, C_{OUT} = 2.2µF)



30004328

Channel 3: SDA (2V/div)
Channel 1: V_{OUT} (AC Coupled, 200mV/div)
Channel 2: I_{MAIN} (20mA/div)
Time Base: 400µs/div

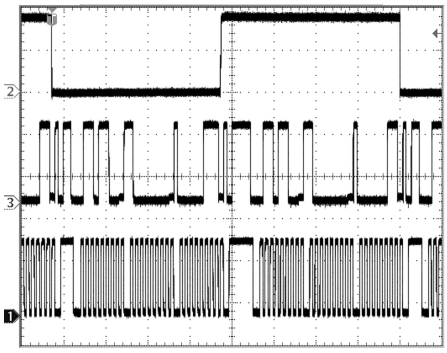
$\overline{\text{RESET}}$ Functionality



30004352

Channel 2: I_{SUB} (20mA/div)
Channel R1: I_{MAIN} (20mA/div)
Channel 1: $\overline{\text{RESET}}$ (2V/div)
Time Base: 200ns/div

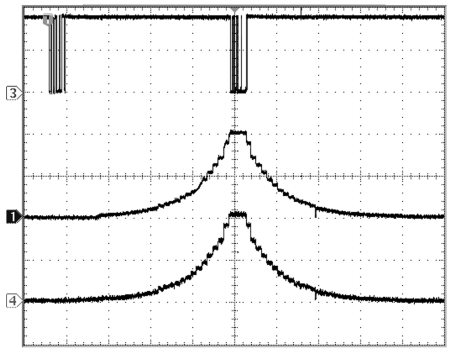
GPIO Functionality
(GPIO Configured as OUTPUT, f_{SCL} = 200kHz)



30004353

Channel 2: GPIO (2V/div)
Channel 3: SDA (2V/div)
Channel 1:SCL (2V/div)
Time Base: 40µs/div

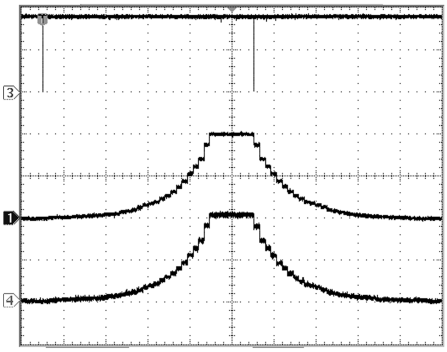
Ramp Rate Functionality
(RMP1, RMP0 = '00')



30004330

Channel 3: SDA (2V/div)
Channel 1: I_{MAIN} (10mA/div)
Channel 4: I_{SUB} (10mA/div)
Time Base: 40µs/div

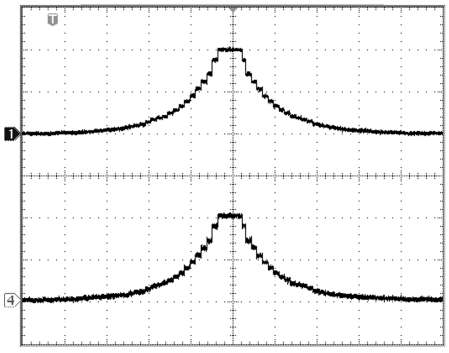
Ramp Rate Functionality
(RMP1, RMP0 = '01')



30004355

Channel 3: SDA (2V/div)
Channel 1: I_{MAIN} (10mA/div)
Channel 4: I_{SUB} (10mA/div)
Time Base: 100ms/div

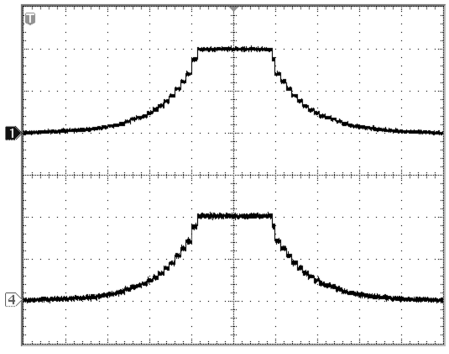
Ramp Rate Functionality
(RMP1, RMP0 = '10')



30004356

Channel 1:I_{MAIN} (10mA/div)
Channel 4: I_{SUB} (10mA/div)
Time Base: 200ms/div

Ramp Rate Functionality
(RMP1, RMP0 = '11')



30004351

Channel 1:I_{MAIN} (10mA/div)
Channel 4: I_{SUB} (10mA/div)
Time Base: 400ms/div

Block Diagram

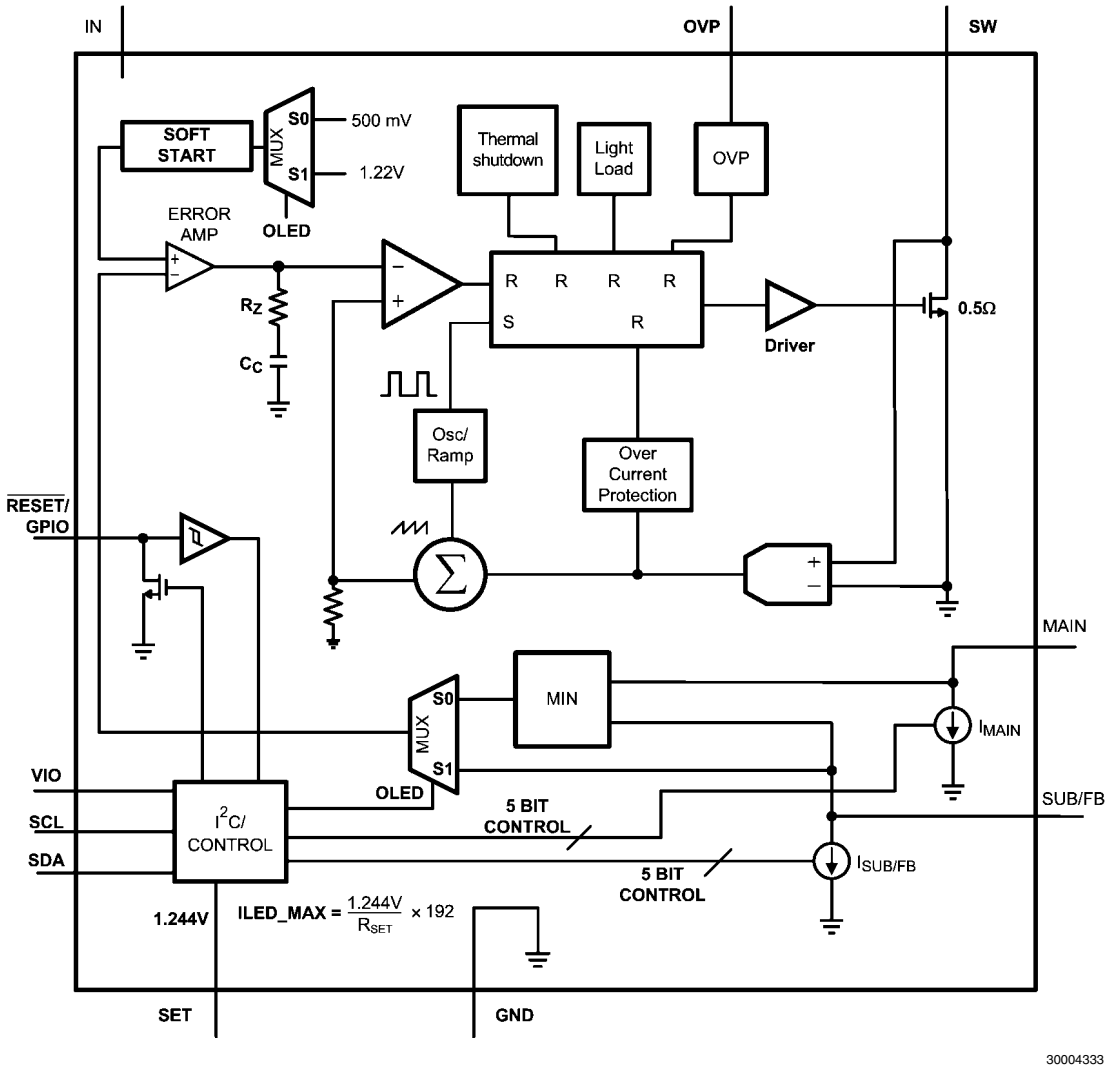


FIGURE 2. LM3509 Block Diagram

Operation Description

The LM3509 Current Mode PWM boost converter operates from a 2.7V to 5.5V input and provides two regulated outputs for White LED and OLED display biasing. The first output, MAIN, provides a constant current of up to 30mA to bias up to 5 series white LED's. The second output, SUB/FB, can be configured as a current source for up to 5 series white LED's at at 30mA, or as a feedback voltage pin to regulate a constant output voltage of up to 21V. When both MAIN and SUB/FB are configured for white LED bias the current for each LED string is controlled independently or in unison via an I²C compatible interface. When MAIN is configured for white LED bias and SUB/FB is configured as a feedback voltage pin, the current into MAIN is controlled via the I²C compatible interface and SUB/FB becomes the middle tap of a resistive divider used to regulate the output voltage of the boost converter.

The core of the LM3509 is a Current Mode Boost converter. Operation is as follows. At the start of each switching cycle the internal oscillator sets the PWM converter. The converter turns the NMOS switch on, allowing the inductor current to ramp while the output capacitor supplies power to the white LED's and/or OLED panel. The error signal at the output of the error amplifier is compared against the sensed inductor current. When the sensed inductor current equals the error signal, or when the maximum duty cycle is reached, the NMOS switch turns off causing the external Schottky diode to pick up the inductor current. This allows the inductor current to ramp down causing its stored energy to charge the output capacitor and supply power to the load. At the end of the clock period the PWM controller is again set and the process repeats itself.

ADAPTIVE REGULATION

When biasing dual white led strings (White LED mode) the LM3509 maximizes efficiency by adaptively regulating the output voltage. In this configuration the 500mV reference is connected to the non-inverting input of the error amplifier via mux S2 (see Figure 2, Block Diagram). The lowest of either V_{MAIN} or $V_{SUB/FB}$ is then applied to the inverting input of the error amplifier via mux S1. This ensures that V_{MAIN} and $V_{SUB/FB}$ are at least 500mV, thus providing enough voltage head-

room at the input to the current sinks for proper current regulation.

In the instance when there are unequal numbers of LEDs or unequal currents from string to string, the string with the highest voltage will be the regulation point.

UNISON/NON-UNISON MODE

Within White LED mode there are two separate modes of operation, Unison and Non-Unison. Non-Unison mode provides for independent current regulation, while Unison mode gives up independent regulation for more accurate matching between LED strings. When in Non-Unison mode the LED currents I_{MAIN} and $I_{SUB/FB}$ are independently controlled via registers BMAIN and BSUB respectively (see Brightness Registers (BMAIN and BSUB) section). When in Unison mode BSUB is disabled and both I_{MAIN} and $I_{SUB/FB}$ are controlled via BMAIN only.

START-UP

The LM3509 features an internal soft-start, preventing large inrush currents during start-up that can cause excessive voltage ripple on the input. For the typical application circuits when the device is brought out of shutdown the average input current ramps from zero to 450mA in 1.2ms. See Start Up Plots in the Typical Performance Characteristics.

OLED MODE

When the LM3509 is configured for a single White LED bias + OLED display bias (OLED mode), the non-inverting input of the error amplifier is connected to the internal 1.21V reference via MUX S2. MUX S1 switches SUB/FB to the inverting input of the error amplifier while disconnecting the internal current sink at SUB/FB. The voltage at MAIN is not regulated in OLED mode so when the application requires white LED + OLED panel biasing, ensure that at least 300mV of headroom is maintained at MAIN to guarantee proper regulation of I_{MAIN}. (see the Typical Performance Characteristics for a plot of I_{LED} vs Current Source Headroom Voltage)

PEAK CURRENT LIMIT

The LM3509's boost converter has a peak current limit for the internal power switch of 770mA typical (650mA minimum). When the peak switch current reaches the current limit the duty cycle is terminated resulting in a limit on the maximum output current and thus the maximum output power the LM3509 can deliver. Calculate the maximum LED current as a function of V_{IN}, V_{OUT}, L and I_{PEAK} as:

$$I_{OUT\_MAX} = \frac{(I_{PEAK} - \Delta I_L) \times \eta \times V_{IN}}{V_{OUT}}$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

f_{SW} = 1.27MHz. Typical values for efficiency and I_{PEAK} can be found in the efficiency and I_{PEAK} curves in the Typical Performance Characteristics.

OVER VOLTAGE PROTECTION

The LM3509's output voltage (V_{OUT}) is limited on the high end by the Output Over-Voltage Protection Threshold (V_{OVP}) of 21.2V. In White LED mode during output open circuit conditions the output voltage will rise to the over voltage protection threshold (V_{OVP} = 21.2V min). When this happens the controller will stop switching causing V_{OUT} to droop. When the output voltage drops below 19.7V (min) the device will resume switching. If the device remains in an over voltage condition the LM3509 will repeat the cycle causing the output to cycle between the high and low OVP thresholds. See waveform for OVP condition in the Typical Performance Characteristics.

OUTPUT CURRENT ACCURACY AND CURRENT MATCHING

The LM3509 provides both precise current accuracy (% error from ideal value) and accurate current matching between the MAIN and SUB/FB current sinks. Two modes of operation affect the current matching between I_{MAIN} and $I_{SUB/FB}$. The first mode (Non-Unison mode) is set by writing a 0 to bit 2 of the General Purpose register (UNI bit). Non-Unison mode allows for independent programming of I_{MAIN} and $I_{SUB/FB}$ via registers BMAIN and BSUB respectively. In this mode typical matching between current sinks is 1%.

Writing a 1 to UNI configures the device for Unison mode. In Unison mode, BSUB is disabled and I_{MAIN} and $I_{SUB/FB}$ are both controlled via register BMAIN. In this mode typical matching is 0.15%.

LIGHT LOAD OPERATION

The LM3509 boost converter operates in three modes; continuous conduction, discontinuous conduction, and skip mode operation. Under heavy loads when the inductor current does not reach zero before the end of the switching period the device switches at a constant frequency. As the output current decreases and the inductor current reaches zero before the end of the switching cycle, the device operates in discontinuous conduction. At very light loads the LM3509 will enter skip mode operation causing the switching period to lengthen and the device to only switch as required to maintain regulation at the output.

ACTIVE LOW RESET/GENERAL PURPOSE I/O ($\overline{\text{RESET}}$ \GPIO)

The $\overline{\text{RESET}}$/GPIO serves as an active low reset input or as a general-purpose logic input/output. Upon power-up of the device $\overline{\text{RESET}}$/GPIO defaults to the active low reset mode. The functionality of $\overline{\text{RESET}}$/GPIO is set via the GPIO register and is detailed in Table 6. When configured as an active low reset input, (Bit 0 = 0), pulling $\overline{\text{RESET}}$/GPIO low automatically programs all registers of the LM3509 with 0x00. Their state cannot be changed until $\overline{\text{RESET}}$/GPIO is pulled high. The General Purpose I/O (GPIO) register is used to enable the GPIO function of the $\overline{\text{RESET}}$/GPIO pin. The GPIO register is an 8-bit register with only the 3 LSB's active. The 5 MSB's are not used. When configured as an output, $\overline{\text{RESET}}$/GPIO is open drain and requires an external pull-up resistor.

THERMAL SHUTDOWN

The LM3509 offers a thermal shutdown protection. When the die temperature reaches +140°C the device will shutdown and not turn on again until the die temperature falls below +120°C.

I²C COMPATIBLE INTERFACE

The LM3509 is controlled via an I²C compatible interface. START and STOP conditions classify the beginning and the end of the I²C session. A START condition is defined as SDA transitioning from HIGH to LOW while SCL is HIGH. A STOP condition is defined as SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always generates START and STOP conditions. The I²C bus is considered busy after a START condition and free after a STOP condition. During data transmission, the I²C master can generate repeated START conditions. A START and a repeated START conditions are equivalent function-wise. The data on SDA must be stable during the HIGH period of the clock signal (SCL). In other words, the state of SDA can only be changed when SCL is LOW.

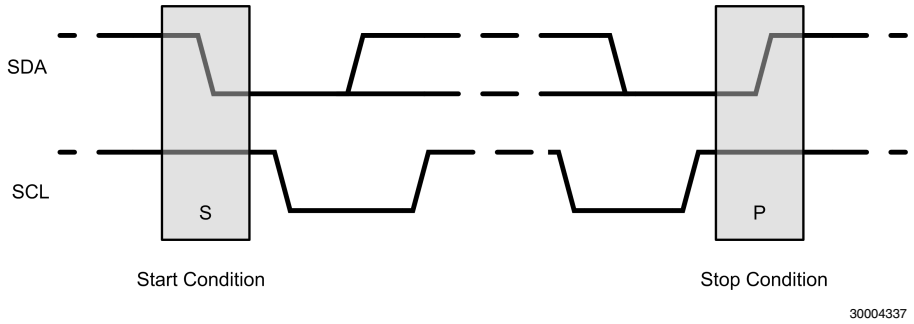


FIGURE 3. Start and Stop Sequences

I²C COMPATIBLE ADDRESS

The chip address for the LM3509 is 0110110 (36h). After the START condition, the I²C master sends the 7-bit chip address followed by a read or write bit (R/W). R/W= 0 indicates a WRITE and R/W = 1 indicates a READ. The second byte following the chip address selects the register address to which the data will be written. The third byte contains the data for the selected register.

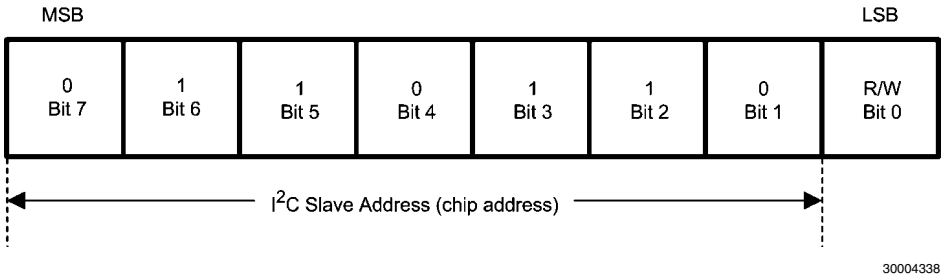


FIGURE 4. Chip Address

TRANSFERRING DATA

Every byte on the SDA line must be eight bits long, with the most significant bit (MSB) transferred first. Each byte of data must be followed by an acknowledge bit (ACK). The acknowledge related clock pulse (9th clock pulse) is generated by the master. The master releases SDA (HIGH) during the 9th clock pulse. The LM3509 pulls down SDA during the 9th clock pulse, signifying an acknowledge. An acknowledge is generated after each byte has been received. Figure 5 is an example of a write sequence to the General Purpose register of the LM3509.

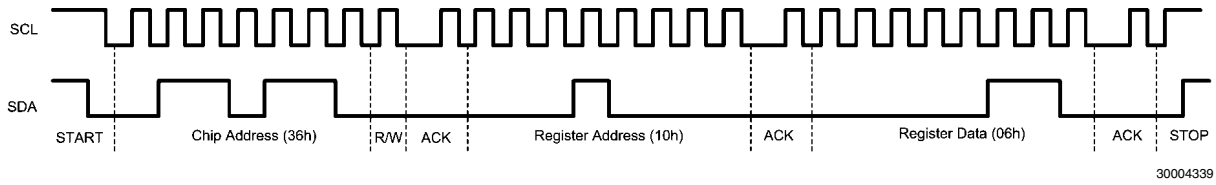


FIGURE 5. Write Sequence to the LM3509

REGISTER DESCRIPTIONS

There are 4, 8 bit registers within the LM3509 as detailed in *Table 1*.

TABLE 1. LM3509 Register Descriptions

Register Name	Hex Address	Power -On-Value
General Purpose (GP)	10	0xC0
Brightness Main (BMAIN)	A0	0xE0
Brightness Sub (BSUB)	B0	0xE0
General Purpose I/O (GPIO)	80	0XF8

GENERAL PURPOSE REGISTER (GP)

The General Purpose register has four functions. It controls the on/off state of MAIN and SUB/FB, it selects between Unison or Non-Unison mode, provides for control over the rate of change of the LED current (see Brightness Rate of Change Description), and selects between White LED and OLED mode. Figure 6 and Table 2 describes each bit available within the General Purpose Register.

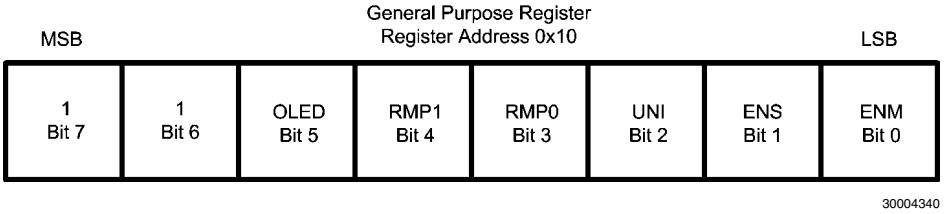


FIGURE 6. General Purpose Register Description

TABLE 2. General Purpose Register Bit Function

Bit	Name	Function	Power-On-Value
0	ENM	Enable MAIN. Writing a 1 to this bit enables the main current sink (MAIN). Writing a 0 to this bit disables the main current sink and forces MAIN high impedance.	0
1	ENS	Enable SUB/FB. Writing a 1 to this bit enables the secondary current sink (SUB/FB). Writing a 0 to this bit disables the secondary current sink and forces SUB/FB high impedance.	0
2	UNI	Unison Mode Select. Writing a 1 to this bit disables the BSUB register and causes the contents of BMAIN to set the current in both the MAIN and SUB/FB current sinks. Writing a 0 to this bit allows the current into MAIN and SUB/FB to be independently controlled via the BMAIN and BSUB registers respectively.	0
3	RMP0	Brightness Rate of Change. Bits RMP0 and RMP1 set the rate of change of the LED current into MAIN and SUB/FB in response to changes in the contents of registers BMAIN and BSUB (see brightness rate of change description).	0
4	RMP1		0
5	OLED	OLED = 0 places the LM3509 in White LED mode. In this mode both the MAIN and SUB/FB current sinks are active. The boost converter ensures there is at least 500mV at V_{MAIN} and $V_{SUB/FB}$. OLED = 1 places the LM3509 in OLED mode. In this mode the boost converter regulates $V_{SUB/FB}$ to 1.25V. V_{MAIN} is unregulated and must be > 400mV for the MAIN current sink to maintain current regulation.	0
6	Don't Care	These are non-functional read only bits. They will always read back as a 1.	1
7			

TABLE 3. Operational Truth Table

UNI	OLED	ENM	ENS	Result
X	0	0	0	LM3509 Disabled
1	0	1	X	MAIN and SUB/FB current sinks enabled. Current levels set by contents of BMAIN.
1	0	0	X	MAIN and SUB/FB Disabled
0	0	0	1	SUB/FB current sink enabled. Current level set by BSUB.
0	0	1	0	MAIN current sink enabled. Current level set by BMAIN.
0	0	1	1	MAIN and SUB/FB current sinks enabled. Current levels set by contents of BMAIN and BSUB respectively.
X	1	1	X	SUB/FB current sink disabled (SUB/FB configured as a feedback pin). MAIN current sink enabled current level set by BMAIN.
X	1	0	X	SUB/FB current sink disabled (SUB/FB configured as a feedback pin). MAIN current sink disabled.

* ENM ,ENS, or OLED high enables analog circuitry.

BRIGHTNESS REGISTERS (BMAIN and BSUB)

With the UNI bit (General Purpose register) set to 0 (Non-Unison mode) both brightness registers (BMAIN and BSUB) independently control the LED currents I_{MAIN} and $I_{SUB/FB}$ respectively. BMAIN and BSUB are both 8 bit, but with only the 5 LSB's controlling the current. The three MSB's are don't cares. The LED current control is designed to approximate an exponentially increasing response of the LED current vs increasing code in either BMAIN or BSUB (see Figure 9). Program I_{LED_MAX} by connecting a resistor (RSET) from SET to GND, where:

$$I_{LED\_MAX} = 192 \times \frac{1.244V}{R_{SET}}$$

. With the UNI bit (General Purpose register) set to 1 (Unison mode), BSUB is disabled and BMAIN sets both I_{MAIN} and $I_{SUB/FB}$. This prevents the independent control of I_{MAIN} and $I_{SUB/FB}$, however matching between current sinks goes from typically 1%(with UNI = 0) to typically 0.15% (with UNI = 1). Figure 7 and Figure 8 show the register descriptions for the Brightness MAIN and Brightness SUB registers. Table 4 and Figure 9 show I_{MAIN} and/or $I_{SUB/FB}$ vs. brightness data as a percentage of I_{LED_MAX}.

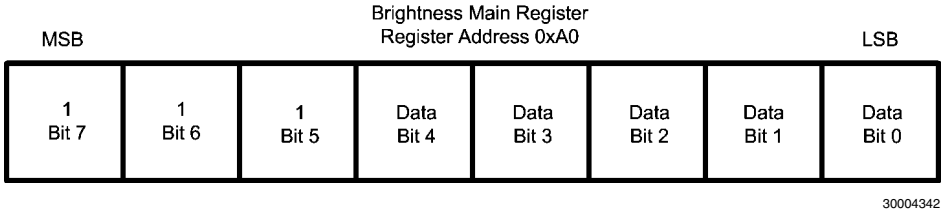


FIGURE 7. Brightness MAIN Register Description

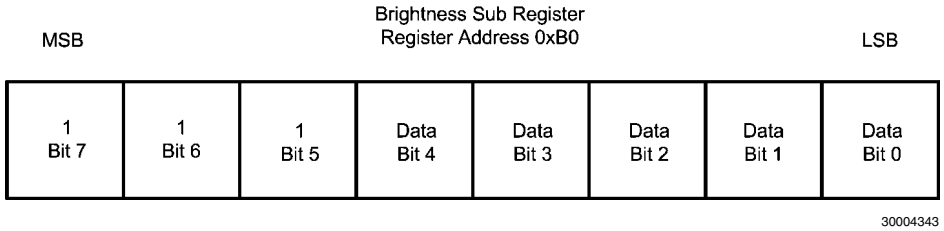


FIGURE 8. Brightness SUB Register Description

TABLE 4. I_{LED} vs. Brightness Register Data

BMAIN or BSUB Brightness Data	% of ILED_MAX	BMAIN or BSUB Brightness Data	% of ILED_MAX
00000	0.000%	10000	8.750%
00001	0.125%	10001	10.000%
00010	0.625%	10010	12.500%
00011	1.000%	10011	15.000%
00100	1.125%	10100	16.875%
00101	1.313%	10101	18.750%
00110	1.688%	10110	22.500%
00111	2.063%	10111	26.250%
01000	2.438%	11000	31.250%
01001	2.813%	11001	37.500%
01010	3.125%	11010	43.750%
01011	3.750%	11011	52.500%
01100	4.375%	11100	61.250%
01101	5.250%	11101	70.000%
01110	6.250%	11110	87.500%
01111	7.500%	11111	100.000%

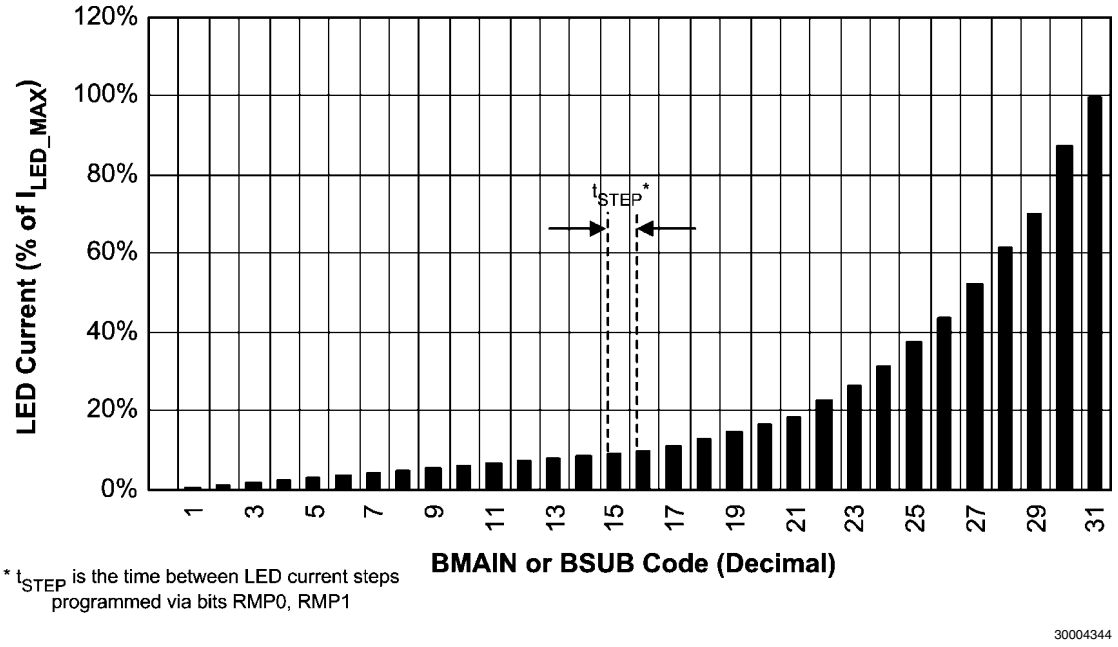


FIGURE 9. I_{MAIN} or I_{SUB} vs BMAIN or BSUB Data

BRIGHTNESS RATE OF CHANGE DESCRIPTION

RMP0 and RMP1 control the rate of change of the LED current I_{MAIN} and $I_{SUB/FB}$ in response to changes in BMAIN and / or BSUB. There are 4 user programmable LED current rates of change settings for the LM3509 (see *Table 5*).

TABLE 5. Rate of Change Bits

RMP0	RMP1	Change Rate (t_{STEP})
0	0	51µs/step
0	1	13ms/step
1	0	26ms/step
1	1	52ms/step

For example, if R_{SET} = 12kΩ then I_{LED_MAX} = 20mA. With the contents of BMAIN set to 0x1F (I_{MAIN} = 20mA), suppose the contents of BMAIN are changed to 0x00 resulting in (I_{MAIN} = 0mA). With RMP0 =1 and RMP1 = 1 (52ms/step), I_{MAIN} will change from 20mA to 0mA in 31 steps with 52ms elapsing between steps, excluding the step from 0x1F to 0x1E, resulting in a full scale current change in 1560ms. The total time to transition from one brightness code to another is:

$$t_{transition} = (|InitialCode - FinalCode| - 1) \times t_{STEP}$$

The following 3 additional examples detail possible scenarios when using the brightness register in conjunction with the rate of change bits and the enable bits.

Example 1:

Step 1: Write to BMAIN a value corresponding to I_{MAIN} = 20-mA.

Step 2: Write 1 to ENM (turning on MAIN)

Step 3: I_{MAIN} ramps to 20mA with a rate set by RMP0 and RMP1. (RMP0 and RMP1 bits set the duration spent at one brightness code before incrementing to the next).

Step 4: ENM is set to 0 before 20mA is reached, thus the LED current fades off at a rate given by RMP0 and RMP1 without I_{MAIN} going up to 20mA.

Example 2:

Step 1: ENM is 1, and BMAIN has been programmed with code 0x01. This results in a small current into MAIN.

Step 2: BMAIN is programmed with 0x1F (full scale current). This causes I_{MAIN} to ramp toward full-scale at the rate selected by RMP0 and RMP1.

Step 3: Before I_{MAIN} reaches full-scale BMAIN is programmed with 0x09. I_{MAIN} will continue to ramp to full scale.

Step 4: When I_{MAIN} has reached full-scale value it will ramp down to the current corresponding to 0x09 at a rate set by RMP0 and RMP1.

Example 3:

Step 1: Write to BMAIN a value corresponding to I_{MAIN} = 20-mA.

Step 2: Write a 1 to both RMP0 and RMP1.

Step 3: Write 1 to ENM (turning on MAIN).

Step 4: I_{MAIN} ramps toward 20mA with a rate set by RMP0 and RMP1. (RMP0 and RMP1 bits set the duration spent at one brightness code before incrementing to the next).

Step 5: After 1.04s I_{MAIN} has ramped to 16.875% of I_{LED_MAX} (0.16875 × 20mA = 3.375mA). Simultaneously, RMP0 and RMP1 are both programmed with 0.

Step 6: I_{MAIN} continues ramping from 3.375mA to 20mA, but at a new ramp rate of 51µs/step.

TABLE 6. GPIO Register Function

Bits 7 – 3	Data (Bit 2)	Mode (Bit 1)	Enable GPIO (Bit 0)	Function
X	X	X	0	$\overline{RESET}$/GPIO is configured as an active low reset input. This is the default power on state.
X	Logic Input	0	1	$\overline{RESET}$/GPIO is configured as a logic input. The logic level applied to $\overline{RESET}$/GPIO can be read via bit 2 of the GPIO register.
X	Logic Output	1	1	$\overline{RESET}$/GPIO is configured as a logic output. A 0 in bit 2 forces $\overline{RESET}$/GPIO low. A 1 in bit 2 forces $\overline{RESET}$/GPIO high impedance.

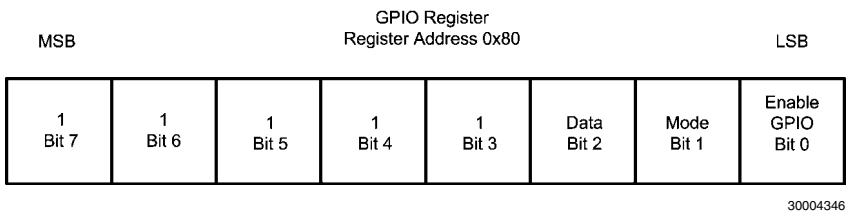


FIGURE 10. GPIO Register Description

SHUTDOWN AND OUTPUT ISOLATION

The LM3509 provides a true shutdown for either MAIN or SUB/FB when configured as a White LED bias supply. Write a 0 to ENM (bit 1) of the General Purpose register to turn off the MAIN current sink and force MAIN high impedance. Write a 0 to ENS (bit 2) of the General Purpose register to turn off the SUB/FB current sink and force SUB/FB high impedance. Writing a 1 to ENM or ENS turns on the MAIN and SUB/FB current sinks respectively. When in shutdown the leakage current into MAIN or SUB/FB is typically 3.6µA. See Typical Performance Plots for start-up responses of the LM3509 using the ENM and ENS bits in White LED and OLED modes.

Application Information

LED CURRENT SETTING/MAXIMUM LED CURRENT

Connect a resistor (R_{SET}) from SET to GND to program the maximum LED current (I_{LED_MAX}) into MAIN or SUB/FB. The R_{SET} to I_{LED_MAX} relationship is:

$$I_{LED\_MAX} = 192 \times \frac{1.244V}{R_{SET}}$$

where SET provides the constant 1.244V output.

OUTPUT VOLTAGE SETTING (OLED MODE)

Connect Feedback resistors from the converters output to SUB/FB to GND to set the output voltage in OLED mode (see R1 and R2 in the Typical Application Circuit (OLED Panel Power Supply). First select R2 < 100kΩ then calculate R1 such that:

$$R1 = R2\left(\frac{V_{OUT}}{1.21V} - 1\right)$$

In OLED mode the MAIN current sink continues to regulate the current through MAIN, however, V_{MAIN} is no longer regulated. To avoid dropout and ensure proper current regulation the application must ensure that V_{MAIN} > 0.3V.

OUTPUT CAPACITOR SELECTION

The LM3509's output capacitor supplies the LED current during the boost converters on time. When the switch turns off the inductor energy is discharged through the diode supplying power to the LED's and restoring charge to the output capacitor. This causes a sag in the output voltage during the on time and a rise in the output voltage during the off time. The output capacitor is therefore chosen to limit the output ripple to an acceptable level depending on LED or OLED panel current requirements and input/output voltage differentials. For proper operation ceramic output capacitors ranging from 1µF to 2.2µF are required.

As with the input capacitor, the output voltage ripple is composed of two parts, the ripple due to capacitor discharge (delta V_Q) and the ripple due to the capacitors ESR (delta V_{ESR}). For continuous conduction mode, the ripple components are found by:

$$\Delta V_Q = \frac{I_{LED} \times (V_{OUT} - V_{IN})}{f_{SW} \times V_{OUT} \times C_{OUT}} \quad \text{and}$$

$$\Delta V_{ESR} = R_{ESR} \times \left(\frac{I_{LED} \times V_{OUT}}{V_{IN}} + \Delta I_L\right)$$

$$\text{where} \quad \Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

INPUT CAPACITOR SELECTION

Choosing the correct size and type of input capacitor helps minimize the input voltage ripple caused by the switching of the LM3509's boost converter. For continuous inductor current operation the input voltage ripple is composed of 2 primary components, the capacitor discharge (delta V_Q) and the capacitor's equivalent series resistance (delta V_{ESR}). These ripple components are found by:

$$\Delta V_Q = \frac{\Delta I_L \text{ x } D}{2 \text{ x } f_{SW} \text{ x } C_{IN}}$$

and

$$\Delta V_{ESR} = 2 \text{ x } \Delta I_L \text{ x } R_{ESR}$$

$$\text{where } \Delta I_L = \frac{V_{IN} \text{ x } (V_{OUT} - V_{IN})}{2 \text{ x } f_{SW} \text{ x } L \text{ x } V_{OUT}}$$

In the typical application circuit a 1µF ceramic input capacitor works well. Since the ESR in ceramic capacitors is typically less than 5mΩ and the capacitance value is usually small, the input voltage ripple is primarily due to the capacitive discharge. With larger value capacitors such as tantalum or aluminum electrolytic the ESR can be greater than 0.5Ω. In this case the input ripple will primarily be due to the ESR.

Table 7 lists different manufacturers for various capacitors and their case sizes that are suitable for use with the LM3509. When configured as a dual output LED driver a 1µF output capacitor is adequate. In OLED mode for output voltages above 12V a 2.2µF output capacitor is required (see Low Output Voltage Operation (OLED) Section).

TABLE 7. Recommended Output Capacitors

Manufacturer	Part Number	Value	Case Size	Voltage Rating
TDK	C1608X5R1E105M	1µF	0603	25V
Murata	GRM39X5R105K25D539	1µF	0603	25V
TDK	C2012X5R1E225M	2.2µF	0805	25V
Murata	GRM219R61E225KA12	2.2µF	0805	25V

INDUCTOR SELECTION

The LM3509 is designed for use with a 10µH inductor, however 22µH are suitable providing the output capacitor is increased 2x's. When selecting the inductor ensure that the saturation current rating (I_{SAT}) for the chosen inductor is high enough and the inductor is large enough such that at the maximum LED current the peak inductor current is less than the LM3509's peak switch current limit. This is done by choosing:

$$I_{SAT} > \frac{I_{LED}}{\eta} \times \frac{V_{OUT}}{V_{IN}} + \Delta I_L \quad \text{where}$$

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}, \text{ and}$$

$$L > \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times V_{OUT} \times \left(I_{PEAK} - \frac{I_{LED\_MAX} \times V_{OUT}}{\eta \times V_{IN}} \right)}$$

Values for I_{PEAK} can be found in the plot of peak current limit vs. V_{IN} in the Typical Performance Characteristics graphs. *Table 8* shows possible inductors, as well as their corresponding case size and their saturation current ratings.

TABLE 8. Recommended Inductors

Manufacturer	Part Number	Value	Dimensions	I_{SAT}	DC Resistance
TDK	VLF3012AT-100MR49	10µH	2.6mm×2.8mm×1mm	490mA	0.36Ω
TDK	VLF4012AT-100MR79	10µH	3.5mm×3.7mm×1.2mm	800mA	0.3Ω
TOKO	A997AS-100M	10µH	3.8mm×3.8mm×1.8mm	580mA	0.18Ω

DIODE SELECTION

The output diode must have a reverse breakdown voltage greater than the maximum output voltage. The diodes average current rating should be high enough to handle the LM3509's output current. Additionally, the diodes peak current rating must be high enough to handle the peak inductor current. Schottky diodes are recommended due to their lower forward voltage drop (0.3V to 0.5V) compared to (0.6V to 0.8V) for PN junction diodes. If a PN junction diode is used, ensure it is the ultra-fast type (trr < 50ns) to prevent excessive loss in the rectifier. For Schottky diodes the B05030WS (or equivalent) work well for most designs. See Table 9 for a list of other Schottky Diodes with similar performance.

TABLE 9. Recommended Schottky Diodes

Manufacturer	Part Number	Package	Reverse Breakdown Voltage	Average Current Rating
Diodes Inc.	B05030WS	SOD-323	30V	0.5A
Philips	BAT760	SOD-323	23V	1A
ON Semiconductor	NSR0320MW2T	SOD-323	30V	1A

OUTPUT CURRENT RANGE (OLED MODE)

The maximum output current the LM3509 can deliver in OLED mode is limited by 4 factors (assuming continuous conduction); the peak current limit of 770mA (typical), the inductor value, the input voltage, and the output voltage. Calculate the maximum output current (I_{OUT_MAX}) using the following equation:

$$I_{OUT\_MAX} = \frac{(I_{PEAK} - \Delta I_L) \times \eta \times V_{IN}}{V_{OUT}}$$

where

$$\Delta I_L = \frac{V_{IN} \times (V_{OUT} - V_{IN})}{2 \times f_{SW} \times L \times V_{OUT}}$$

For the typical application circuit with V_{OUT} = 18V and assuming 70% efficiency, the maximum output current at V_{IN} = 2.7V will be approximately 70mA. At 4.2V due to the shorter on times and lower average input currents the maximum output current (at 70% efficiency) jumps to approximately 105mA. Figure 11 shows a plot of I_{OUT_MAX} vs. V_{IN} using the above equation, assuming 80% efficiency. In reality factors such as current limit and efficiency will vary over V_{IN}, temperature, and component selection. This can cause the actual I_{OUT_MAX} to be higher or lower.

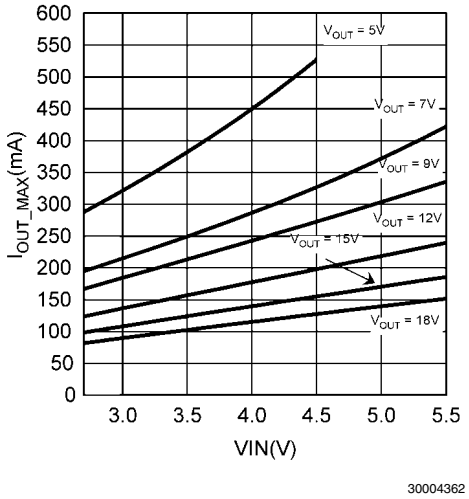


FIGURE 11. Typical Maximum Output Current in OLED Mode

OUTPUT VOLTAGE RANGE (OLED MODE)

The LM3509's output voltage is constrained by 2 factors. On the low end it is limited by the minimum duty cycle of 10% (assuming continuous conduction) and on the high end it is limited by the over voltage protection threshold (V_{OVP}) of 22V (typical). In order to maintain stability when operating at different output voltages the output capacitor and inductor must be changed. Refer to Table 10 for different V_{OUT}, C_{OUT}, and L combinations.

TABLE 10. Component Values for Output Voltage Selection

V_{OUT}	C_{OUT}	L	V_{IN} Range
18V	2.2µF	10µH	2.7V to 5.5V
15V	2.2µF	10µH	2.7V to 5.5V
12V	4.7µF	10µH	2.7V to 5.5V
9V	10µF	10µH	2.7V to 5.5V
7V	10µF	4.7µH	2.7V to 5.5V
5V	22µF	4.7µH	2.7V to 4.5V

LAYOUT CONSIDERATIONS

The LLP is a leadless package with very good thermal properties. This package has an exposed DAP (die attach pad) at the underside center of the package measuring 1.6mm x 2.0mm. The main advantage of this exposed DAP is to offer low thermal resistance when soldered to the thermal ground pad on the PCB. For good PCB layout a 1:1 ratio between the package and the PCB thermal land is recommended. To further enhance thermal conductivity, the PCB thermal ground pad may include vias to a 2nd layer ground plane. For more detailed instructions on mounting LLP packages, please refer to National Semiconductor Application Note AN-1187.

The high switching frequencies and large peak currents make the PCB layout a critical part of the design. The proceeding steps must be followed to ensure stable operation and proper current source regulation.

1, Divide ground into two planes, one for the return terminals of C_{OUT}, C_{IN} and the I^2C Bus, the other for the return terminals of R_{SET} and the feedback network. Connect both planes to the exposed PAD, but nowhere else.

2, Connect the inductor and the anode of D1 as close together as possible and place this connection as close as possible to the SW pin. This reduces the inductance and resistance of the switching node which minimizes ringing and excess voltage drops. This will improve efficiency and decrease noise that can get injected into the current sources.

3, Connect the return terminals of the input capacitor and the output capacitor as close as possible to the exposed PAD and through low impedance traces.

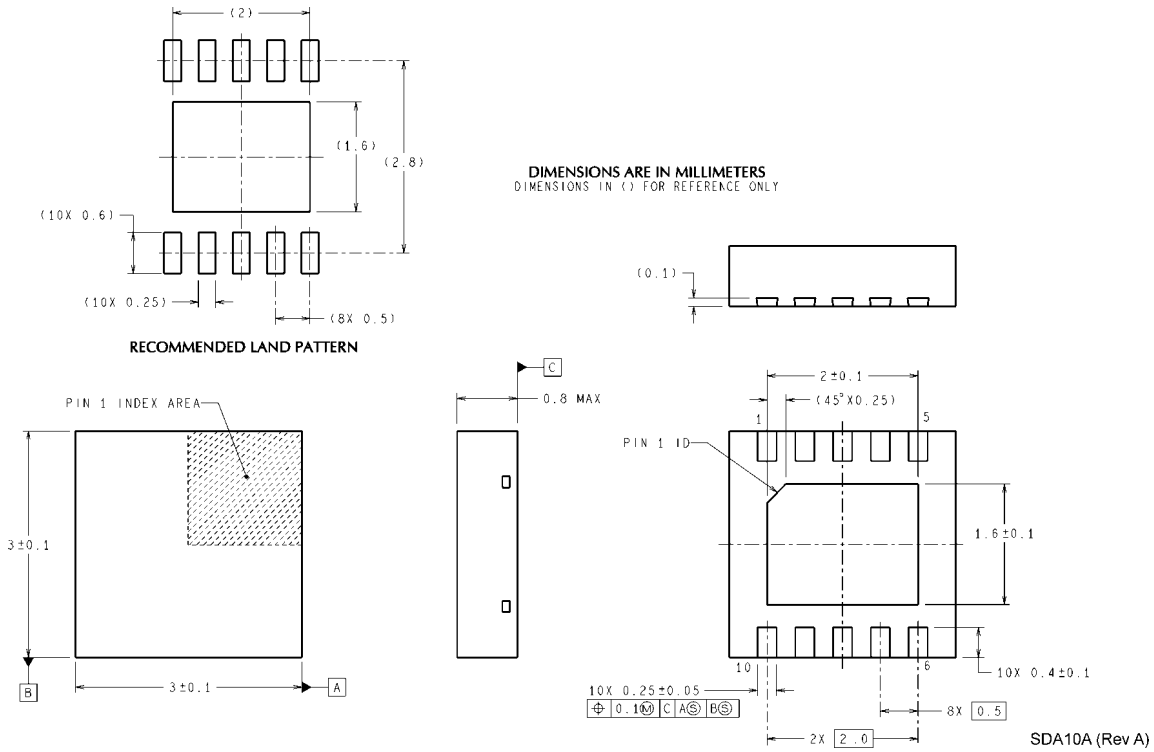
4, Bypass IN with at least a 1µF ceramic capacitor. Connect the positive terminal of this capacitor as close as possible to IN.

5, Connect C_{OUT} as close as possible to the cathode of D1. This reduces the inductance and resistance of the output bypass node which minimizes ringing and the excess voltage drops. This will improving efficiency and decrease noise that can get injected into the current sources.

6, Route the traces for R_{SET} and the feedback divider away from the SW node to minimize noise injection.

7, Do not connect any external capacitance to the SET pin.

Physical Dimensions inches (millimeters) unless otherwise noted



10 Pin LLP
For Ordering, Refer to Ordering Information Table
NS Package Number SDA10A
X1 = 3mm (±0.1mm), X2 = 3mm (±0.1mm), X3 = 0.8mm

Notes

Notes

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Tel: 1-800-272-9959

National Semiconductor Europe Technical Support Center
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National Semiconductor Asia Pacific Technical Support Center
Email: ap.support@nsc.com

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Email: jpn.feedback@nsc.com