

LP3944

RGB/White/Blue 8-LED Fun Light Driver

General Description

LP3944 is an integrated device capable of independently driving 8 LEDs. This device also contains an internal precision oscillator that provides all the necessary timing required for driving each LED. Two prescaler registers along with two PWM registers provide a versatile duty cycle control. The LP3944 contains the ability to dim LEDs in SMBUS/I²C applications where it is required to cut down on bus traffic.

Traditionally, to dim LEDs using a serial shift register such as 74LS594/5 would require a large amount of traffic to be on the serial bus. LP3944 instead requires only the setup of the frequency and duty cycle for each output pin. From then on, only a single command from the host is required to turn each individual open drain output ON, OFF, or to cycle a programmed frequency and duty cycle. Maximum output sink current is 25 mA per pin and 200 mA per package. Any ports not used for controlling the LEDs can be used for general purpose input/output expansion.

Features

- Internal power-on reset
- Active low reset
- Internal precision oscillator
- Variable dim rates (from 6.25 ms to 1.6s; 160 Hz–0.625 Hz)

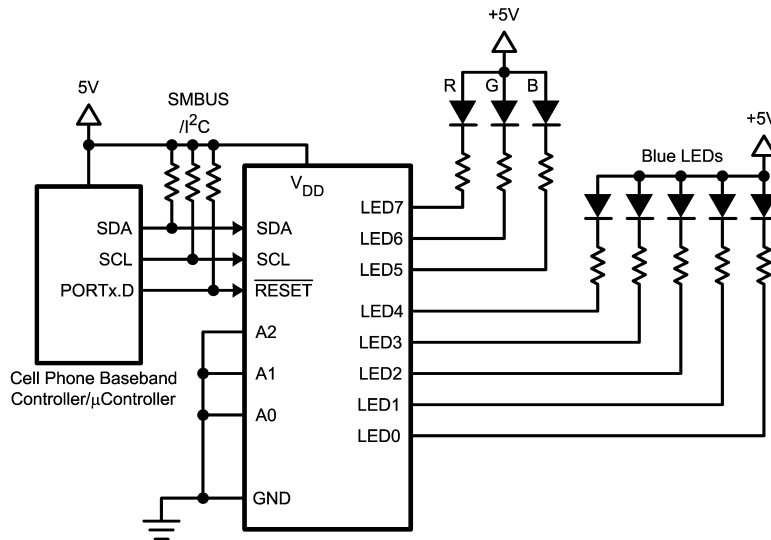
Key Specifications

- 8 LED driver (multiple programmable states—on, off, input, and dimming at a specified rate)
- 8 Open drain outputs capable of driving up to 25 mA per LED

Applications

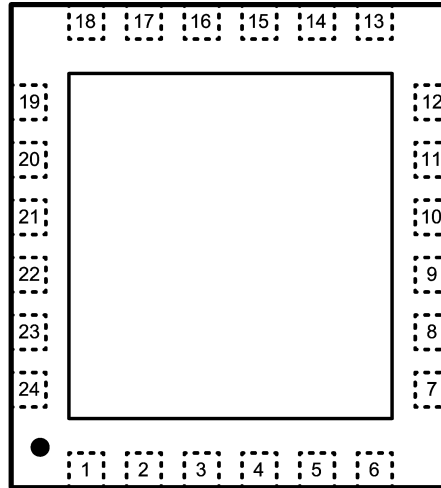
- Customized flashing LED lights for cellular phones
- Portable Applications
- Digital Cameras
- Indicator Lamps
- General purpose I/O expander
- Toys

Typical Application Circuit



20085301

LP3944 Pin Out



20085302

(Top View)
See NS Package Number SQA24A

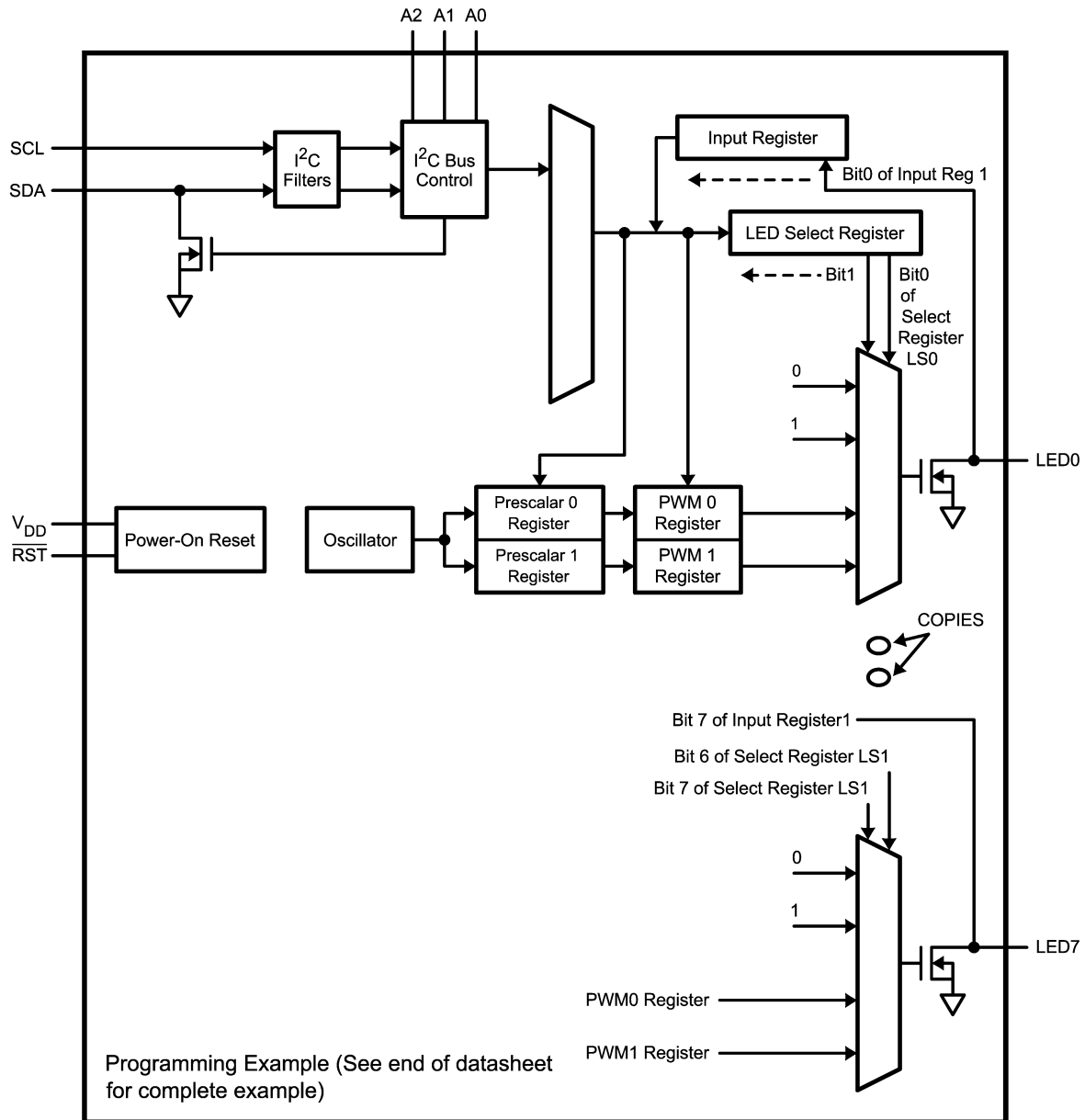
LP3944 Pin Description

| Pin # | Name | Description |
|-------|-------------------------|---|
| 1 | LED0 | Output of LED0 Driver |
| 2 | LED1 | Output of LED1 Driver |
| 3 | LED2 | Output of LED2 Driver |
| 4 | LED3 | Output of LED3 Driver |
| 5 | LED4 | Output of LED4 Driver |
| 6 | LED5 | Output of LED5 Driver |
| 7 | LED6 | Output of LED6 Driver |
| 8 | LED7 | Output of LED7 Driver |
| 9 | GND | Ground |
| 10 | NC | No Connect |
| 11 | NC | No Connect |
| 12 | NC | No Connect |
| 13 | NC | No Connect |
| 14 | NC | No Connect |
| 15 | NC | No Connect |
| 16 | NC | No Connect |
| 17 | NC | No Connect |
| 18 | $\overline{\text{RST}}$ | Active Low Reset Input |
| 19 | SCL | Clock Line for I ² C Interface |
| 20 | SDA | Serial Data Line for I ² C Interface |
| 21 | V _{DD} | Power Supply |
| 22 | A0 | Address Input 0 |
| 23 | A1 | Address Input 1 |
| 24 | A2 | Address Input 2 |

Ordering Information

| | | |
|---|---|-----------------|
| LP3944, Supplied as 1000 Units, Tape and Reel | LP3944, Supplied as 4500 Units, Tape and Reel | Package Marking |
| LP3944ISQ | LP3944ISQX | |

Architectural Block Diagram



20085303

For Explanation of LP3944 Operation, Please Refer to "Theory of Operation" in Application Notes.

Absolute Maximum Ratings (Notes 2,

1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|--|----------------------|
| V_{DD} | -0.5V to 6V |
| A0, A1, A2, SCL, SDA, \overline{RST} (Collectively called digital pins) | 6V |
| Voltage on LED pins | V_{SS} -0.5V to 6V |
| Junction Temperature | 150°C |
| Storage Temperature | -65°C to 150°C |
| Power Dissipation (Note 3) | 1.76W |
| ESD (Note 4) | |

| | |
|---------------------|------|
| Human Body Model | 2 kV |
| Machine Model | 150V |
| Charge Device Model | 1 kV |

Operating Ratings (Notes 1, 2)

| | |
|--------------------------------------|-----------------|
| V_{DD} | 2.3V to 5.5V |
| Junction Temperature | -40°C to +125°C |
| Operating Ambient Temperature | -40°C to +85°C |
| Thermal Resistance (θ_{JA}) | |
| LLP24 (Note 3) | 37°C/W |
| Power Dissipation | 1.08W |

Electrical Characteristics

Unless otherwise noted, $V_{DD} = 5.5V$. Typical values and limits appearing in normal type apply for $T_J = 25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J = -40^\circ C$ to $+125^\circ C$. (Note 5)

| Symbol | Parameter | Conditions | Typical | Limit | | Units |
|--|------------------------------------|---|---------|--------------------------|--------------------------|---------|
| | | | | Min | Max | |
| POWER SUPPLY | | | | | | |
| V_{DD} | Supply Voltage | | 5 | 2.3 | 5.5 | V |
| I_Q | Supply Current | No Load | 350 | | 550 | μA |
| | | Standby | 2.0 | | 5 | |
| ΔI_Q | Additional Standby Current | $V_{DD} = 5.5V$, every LED pin at 4.3V | | | 2 | mA |
| V_{POR} | Power-On Reset Voltage | | 1.8 | | 1.96 | V |
| t_w | Reset Pulse Width | | 10 | | | ns |
| LED | | | | | | |
| V_{IL} | LOW Level Input Voltage | | | -0.5 | 0.8 | V |
| V_{IH} | HIGH Level Input Voltage | | | 2.0 | 5.5 | V |
| I_{OL} | Low Level Output Current (Note 6) | $V_{OL} = 0.4V, V_{DD} = 2.3V$ | | 9 | | mA |
| | | $V_{OL} = 0.4V, V_{DD} = 3.0V$ | | 12 | | |
| | | $V_{OL} = 0.4V, V_{DD} = 5.0V$ | | 15 | | |
| | | $V_{OL} = 0.7V, V_{DD} = 2.3V$ | | 15 | | |
| | | $V_{OL} = 0.7V, V_{DD} = 3.0V$ | | 20 | | |
| | | $V_{OL} = 0.7V, V_{DD} = 5.0V$ | | 25 | | |
| I_{LEAK} | Input Leakage Current | $V_{DD} = 3.6, V_{IN} = 0V$ or V_{DD} | | -1 | 1 | μA |
| $C_{I/O}$ | Input/Output Capacitance | (Note 7) | 2.6 | | 5 | pF |
| ALL DIGITAL PINS (EXCEPT SCL AND SDA PINS) | | | | | | |
| V_{IL} | LOW Level Input Voltage | | | -0.5 | 0.8 | V |
| V_{IH} | HIGH Level Input Voltage | | | 2.0 | 5.5 | V |
| I_{LEAK} | Input Leakage Current | | | -1 | 1 | μA |
| C_{IN} | Input Capacitance | $V_{IN} = 0V$ (Note 7) | 2.3 | | 5 | pF |
| I²C INTERFACE (SCL AND SDA PINS) | | | | | | |
| V_{IL} | LOW Level Input Voltage | | | -0.5 | 0.3V_{DD} | V |
| V_{IH} | HIGH Level Input Voltage | | | 0.7V_{DD} | 5.5 | V |
| V_{OL} | LOW Level Output Voltage | | | 0 | 0.2V_{DD} | V |
| I_{OL} | LOW Level Output Current | $V_{OL} = 0.4V$ | 6.5 | 3 | | mA |
| F_{CLK} | Clock Frequency | (Note 7) | | | 400 | kHz |
| t_{HOLD} | Hold Time Repeated START Condition | (Note 7) | | 0.6 | | μs |

Electrical Characteristics (Continued)

Unless otherwise noted, $V_{DD} = 5.5V$. Typical values and limits appearing in normal type apply for $T_J = 25^\circ C$. Limits appearing in **boldface** type apply over the entire junction temperature range for operation, $T_J = -40^\circ C$ to $+125^\circ C$. (Note 5)

| Symbol | Parameter | Conditions | Typical | Limit | | Units |
|--|--|------------|---------|------------|-----|---------|
| | | | | Min | Max | |
| I²C INTERFACE (SCL AND SDA PINS) | | | | | | |
| t_{CLK-LP} | CLK Low Period | (Note 7) | | 1.3 | | μs |
| t_{CLK-HP} | CLK High Period | (Note 7) | | 0.6 | | μs |
| t_{SU} | Set-Up Time Repeated START Condition | (Note 7) | | 0.6 | | μs |
| $t_{DATA-HOLD}$ | Data Hold Time | (Note 7) | | 300 | | ns |
| $t_{DATA-SU}$ | Data Set-Up Time | (Note 7) | | 100 | | ns |
| t_{SU} | Set-Up Time for STOP Condition | (Note 7) | | 0.6 | | μs |
| t_{TRANS} | Maximum Pulse Width of Spikes that Must Be Suppressed by the Input Filter of Both DATA & CLK Signals | (Note 7) | 50 | | | ns |

Note 1: Absolute Maximum Ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions under which operation of the device is guaranteed. Operating Ratings do not imply guaranteed performance limits. For guaranteed performance limits and associated test conditions, see the Electrical Characteristics tables.

Note 2: All voltages are with respect to the potential at the GND pin.

Note 3: The Absolute Maximum power dissipation depends on the ambient temperature and can be calculated using the formula

$$P = (T_J - T_A) / \theta_{JA} \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance. The 1.76W rating appearing under Absolute Maximum Ratings results from substituting the Absolute Maximum junction temperature, $150^\circ C$, for T_J , $85^\circ C$ for T_A , and $37^\circ C/W$ for θ_{JA} . More power can be dissipated safely at ambient temperature below $85^\circ C$. Less power can be dissipated safely at ambient temperatures above $85^\circ C$. The Absolute Maximum power dissipation can be increased by 27 mW for each degree below $85^\circ C$, and it must be de-rated by 27 mW for each degree above $85^\circ C$. For Operating Ratings maximum power dissipation, $T_J = 125^\circ C$ and $T_A = 85^\circ C$

Note 4: The human-body model is 100 pF discharged through 1.5 k Ω . The machine model is 0 Ω in series with 220 pF.

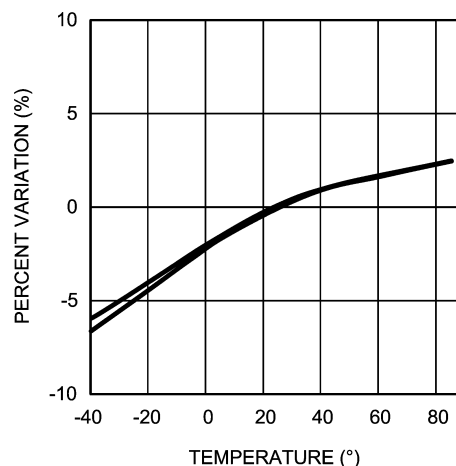
Note 5: Limits are guaranteed. All electrical characteristics having room-temperature limits are tested during production with $T_J = 25^\circ C$. All hot and cold limits are guaranteed by correlating the electrical characteristics to process and temperature variations and applying statistical process control.

Note 6: Each LED pin should not exceed 25 mA and the package should not exceed a total of 200 mA.

Note 7: Guaranteed by design.

Typical Performance Characteristics

Frequency vs. Temp
($T_A = -40^\circ C$ to $+85^\circ C$),
 $V_{DD} = 2.3V$ to $3.0V$



20085317

Application Notes

THEORY OF OPERATION

The LP3944 takes incoming data and feeds them into several registers that control the frequency and the duty cycle of the LEDs. Two prescaler registers and two PWM registers provide two individual rates to dim or blink the LEDs (for more information on these registers, refer to *Table 1. LP3944 REGISTER TABLE*). The baseband controller/microprocessor can program each LED to be in one of four states—on, off, DIM0 rate or DIM1 rate. One read-only register provides status on all 8 LEDs. The LP3944 can be used to drive RGB LEDs and/or single-color LEDs to create a colorful, entertaining, and informative setting. This is particularly suitable for accessory functions in cellular phones and toys. Any LED pins not used to drive LED can be used for General Purpose Parallel Input/Output (GPIO) expansion.

The LP3944 is equipped with Power-On Reset that holds the chip in a reset state until V_{DD} reaches V_{POR} during power up. Once V_{POR} is achieved, the LP3944 comes out of reset and initializes itself to the default state.

To bring the LP3944 into reset, hold the \overline{RST} pin LOW for a period of TW . This will put the chip to its default state. The LP3944 can only be programmed after RST signal is HIGH again.

I²C DATA VALIDITY

The data on SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, state of the data line can only be changed when CLK is LOW.

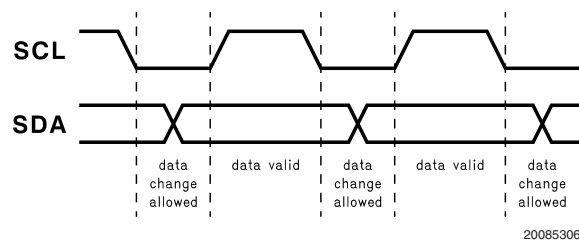


FIGURE 1. I²C Data Validity

I²C START AND STOP CONDITIONS

START and STOP bits classify the beginning and the end of the I²C session. START condition is defined as SDA signal transitioning from HIGH to LOW while SCL line is HIGH. STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The I²C master always

generates START and STOP bits. The I²C bus is considered to be busy after START condition and free after STOP condition. During data transmission, I²C master can generate repeated START conditions. First START and repeated START conditions are equivalent, function-wise.

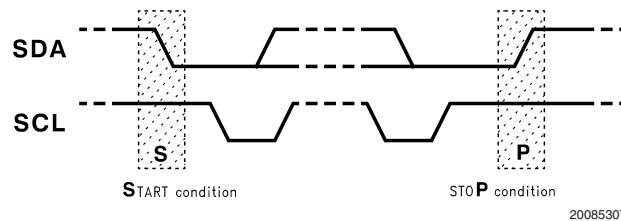


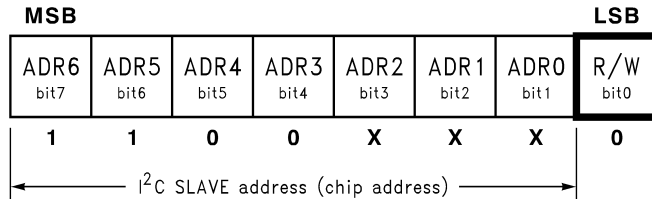
FIGURE 2. I²C START and STOP Conditions

TRANSFERRING DATA

Every byte put on the SDA line must be eight bits long with the most significant bit (MSB) being transferred first. The number of bytes that can be transmitted per transfer is unrestricted. Each byte of data has to be followed by an acknowledge bit. The acknowledge related clock pulse is generated by the master. The transmitter releases the SDA line (HIGH) during the acknowledge clock pulse. The receiver must pull down the SDA line during the 9th clock pulse, signifying an acknowledge. A receiver which has been addressed must generate an acknowledge after each byte has been received.

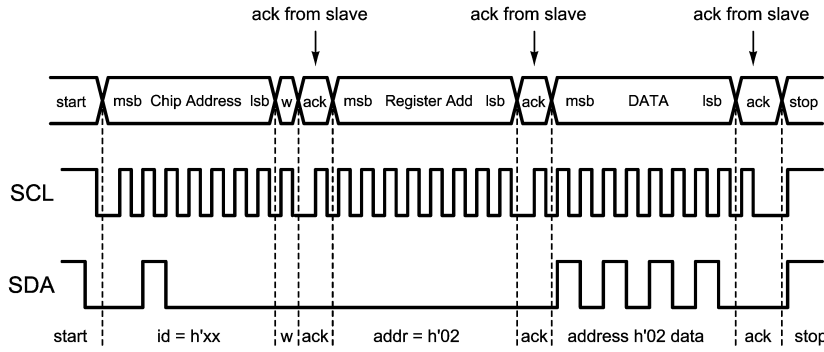
After the START condition, a chip address is sent by the I²C master. This address is seven bits long followed by an eighth bit which is a data direction bit (R/W). The LP3944 hardwires bits 7 to 4 and leaves bits 3 to 1 selectable, as shown in *Figure 3*. For the eighth bit, a "0" indicates a WRITE and a "1" indicates a READ. The LP3944 supports only a WRITE during chip addressing. The second byte selects the register to which the data will be written. The third byte contains data to write to the selected register.

Application Notes (Continued)



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FIGURE 3. Chip Address Byte

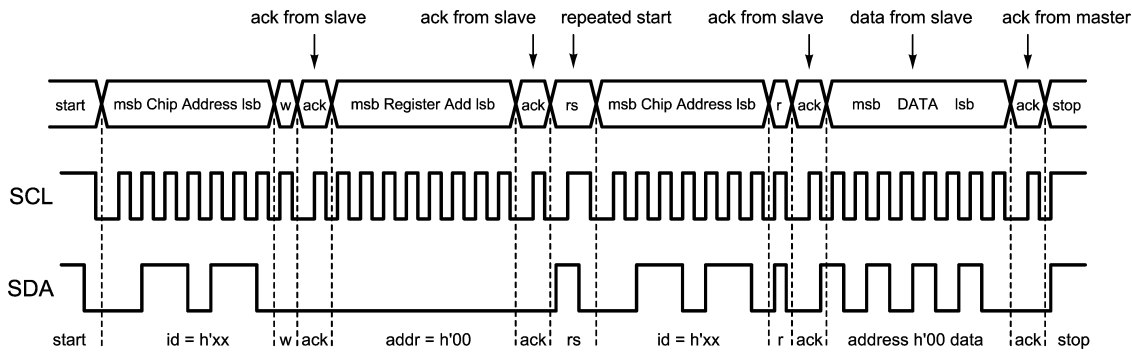


20085309

w = write (SDA = "0")
 r = read (SDA = "1")
 ack = acknowledge (SDA pulled down by either master or slave)
 rs = repeated start
 xx = 60 to 67

FIGURE 4. LP3944 Register Write

However, if a READ function is to be accomplished, a WRITE function must precede the READ function, as shown in *Figure 5*.



20085310

w = write (SDA = "0")
 r = read (SDA = "1")
 ack = acknowledge (SDA pulled down by either master or slave)
 rs = repeated start
 xx = 60 to 67

FIGURE 5. LP3944 Register Read

Application Notes (Continued)

AUTO INCREMENT

Auto increment is a special feature supported by the LP3944 to eliminate repeated chip and register addressing when data are to be written to or read from registers in sequential

order. The auto increment bit is inside the register address byte, as shown in *Figure 6*. Auto increment is enabled when this bit is programmed to “1” and disabled when it is programmed to “0”.

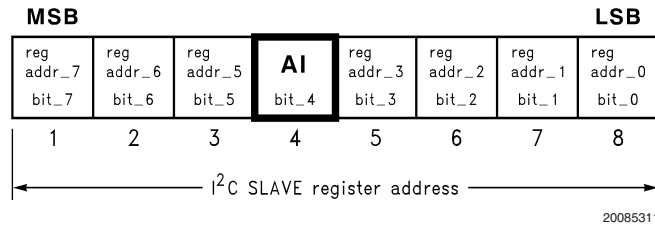


FIGURE 6. Register Address Byte

In the READ mode, when auto increment is enabled, I²C master could receive any number of bytes from LP3944 without selecting chip address and register address again. Every time the I²C master reads a register, the LP3944 will increment the register address and the next data register will be read. When I²C master reaches the last register (09H register), the register address will roll over to 00H.

because the first two registers in LP3944 are read-only registers. It is possible to write to these two registers, and the LP3944 will acknowledge, but the data will be ignored.

In the WRITE mode, when auto increment is enabled, the LP3944 will increment the register address every time I²C master writes to register. When the last register (09H register) is reached, the register address will roll over to 02H,

In the LP3944, registers 0x01, 0x08 and 0x09 are not functional. However, it is still necessary to read from 0x01 and to write to 0x08 and 0x09 in Auto Increment mode. They cannot be skipped.

If auto increment is disabled, and the I²C master does not change register address, it will continue to write data into the same register.

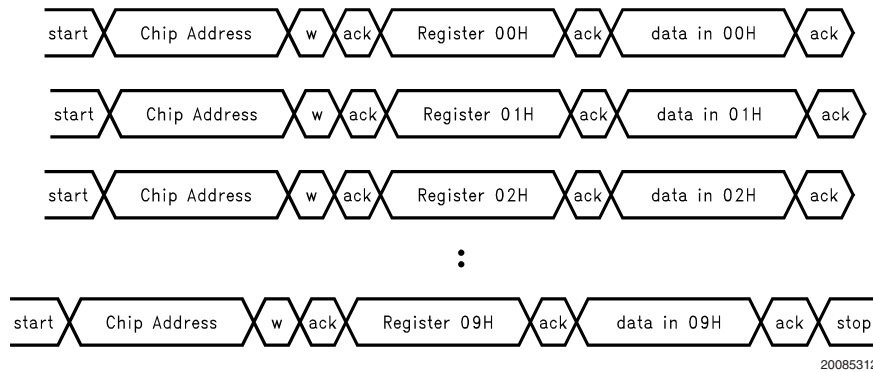


FIGURE 7. Programming with Auto Increment Disabled (in WRITE Mode)

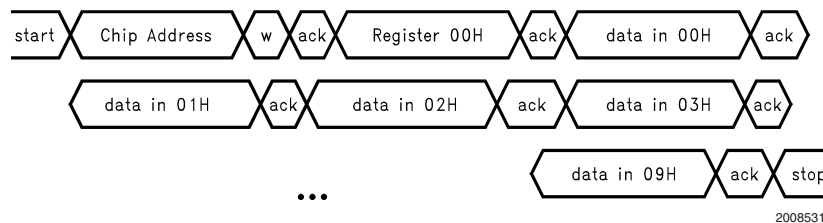


FIGURE 8. Programming with Auto Increment Enabled (in WRITE Mode)

Application Notes (Continued)

TABLE 1. LP3944 REGISTER TABLE

| Address (Hex) | Register Name | Read/Write | Register Function |
|---------------|---------------|------------|-----------------------|
| 0x00 | Input 1 | Read Only | LED0–7 Input Register |
| 0x01 | Register 1 | Read Only | None |
| 0x02 | PSC0 | R/W | Frequency Prescaler 0 |
| 0x03 | PWM0 | R/W | PWM Register 0 |
| 0x04 | PSC1 | R/W | Frequency Prescaler 1 |
| 0x05 | PWM1 | R/W | PWM Register 1 |
| 0x06 | LS0 | R/W | LED0–3 Selector |
| 0x07 | LS1 | R/W | LED4–7 Selector |
| 0x08 | Register 8 | R/W | None |
| 0x09 | Register 9 | R/W | None |

Note: Registers 1, 8 and 9 are empty and non-functional registers. Register 1 is read-only, with all bits hard-wired to zero. Registers 8 and 9 can be written and read, but the content does not have any effect on the operation of the LP3944.

BINARY FOMAT FOR INPUT REGISTERS (READ ONLY)— ADDRESS 0x00 and 0x01
Address 0x00

| | | | | | | | | |
|---------------|------|------|------|------|------|------|------|------|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Default value | X | X | X | X | X | X | X | X |
| | LED7 | LED6 | LED5 | LED4 | LED3 | LED2 | LED1 | LED0 |

X = don't care

BINARY FORMAT FOR FREQUENCY PRESCALER AND PWM REGISTERS — ADDRESS 0x02 to 0x05
Address 0x02 (PSC0)

| | | | | | | | | |
|---------------|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Default value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PSC0 register is used to program the period of DIM0.

$$\text{DIM0} = (\text{PSC0} + 1) / 160$$

The maximum period is 1.6s when PSC0 = 255.

Address 0x03 (PWM0)

| | | | | | | | | |
|---------------|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Default value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PWM0 register determines the duty cycle of DIM0. The LED outputs are LOW (LED on) when the count is less than the value in PWM0 and HIGH (LED off) when it is greater. If PWM0 is programmed with 0x00, LED output is always HIGH (LED off).

The duty cycle of DIM0 is: $\text{PWM0}/256$

Default value is 50% duty cycle.

Address 0x04 (PSC1)

| | | | | | | | | |
|---------------|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Default value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PSC1 register is used to program the period of DIM1.

$$\text{DIM1} = (\text{PSC1} + 1) / 160$$

The maximum period is 1.6s when PSC1 = 255.

Application Notes (Continued)

Address 0x05 (PWM1)

| | | | | | | | | |
|---------------|---|---|---|---|---|---|---|---|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Default value | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PWM1 register determines the duty cycle of DIM1. The LED outputs are LOW (LED on) when the count is less than the value in PWM1 and HIGH (LED off) when it is greater. If PWM1 is programmed with 0x00, LED output is always HIGH (LED off).

The duty cycle of DIM1 is: $PWM1/256$
 Default value is 50% duty cycle.

BINARY FORMAT FOR SELECTOR REGISTERS — ADDRESS 0x06 to 0x07

Address 0x06 (LS0)

| | | | | | | | | |
|---------------|------|----|------|----|------|----|------|----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Default value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | B1 | B0 | B1 | B0 | B1 | B0 | B1 | B0 |
| | LED3 | | LED2 | | LED1 | | LED0 | |

Address 0x07 (LS1)

| | | | | | | | | |
|---------------|------|----|------|----|------|----|------|----|
| Bit # | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Default value | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | B1 | B0 | B1 | B0 | B1 | B0 | B1 | B0 |
| | LED7 | | LED6 | | LED5 | | LED4 | |

LED States With Respect To Values in "B1" and "B0"

| B1 | B0 | Function |
|----|----|----------------------------|
| 0 | 0 | Output Hi-Z (LED off) |
| 0 | 1 | Output LOW (LED on) |
| 1 | 0 | Output dims (DIM0 rate) |
| 1 | 1 | Output dims (DIM1 rate) |

Programming Example:

Dim LEDs 0 to 7 at 1 Hz at 25% duty cycle

Step 1: Set PSC0 to achieve DIM0 of 1s

Step 2: Set PWM0 duty cycle to 25%

Step 3: Set PSC1 to achieve DIM1 of 0.2s

Step 4: Set LEDs 0 to 7 to point to DIM0

| Step | Description | Register Name | Set to (Hex) |
|------|---|---------------|--------------------------|
| 1 | Set DIM0 = 1s $1 = (PSC0 + 1)/160$ PSC0 = 159 | PSC0 | 0x09F |
| 2 | Set duty cycle to 25% Duty Cycle = $PWM0/256$ PWM0 = 64 | PWM0 | 0x40 |
| 3 | Set DIM1 = 0.2s $0.2 = (PSC1 + 1)/160$ PSC1 = 31 | PSC1 | 0x1F |
| 4 | LEDs 0 to 7 Output = DIM0 | LS0, LS1 | LS0 = 0xAA LS1 = 0xAA |

Application Notes (Continued)

REDUCING I_Q WHEN LEDS ARE OFF

In many applications, the LEDs and the LP3944 share the same V_{DD} , as shown in *Section Typical Application Circuit*. When the LEDs are off, the LED pins are at a lower potential

than V_{DD} , causing extra supply current (ΔI_Q). To minimize this current, consider keeping the LED pins at a voltage equal to or greater than V_{DD} .

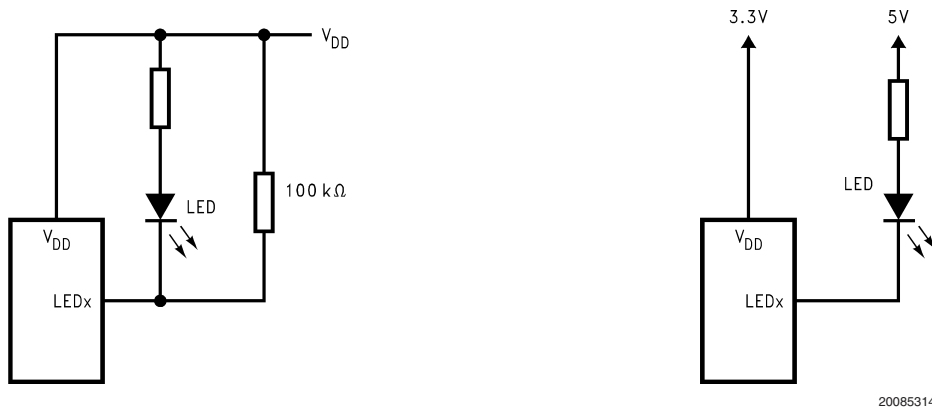
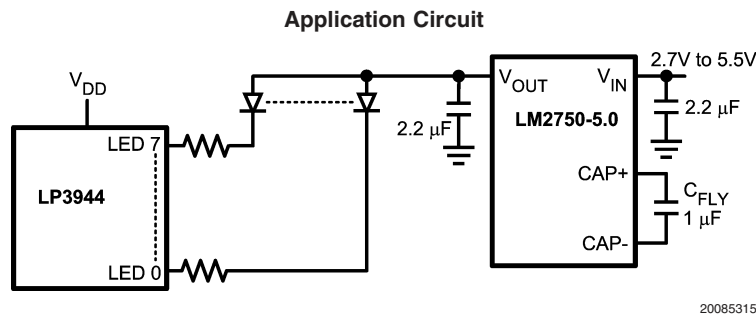
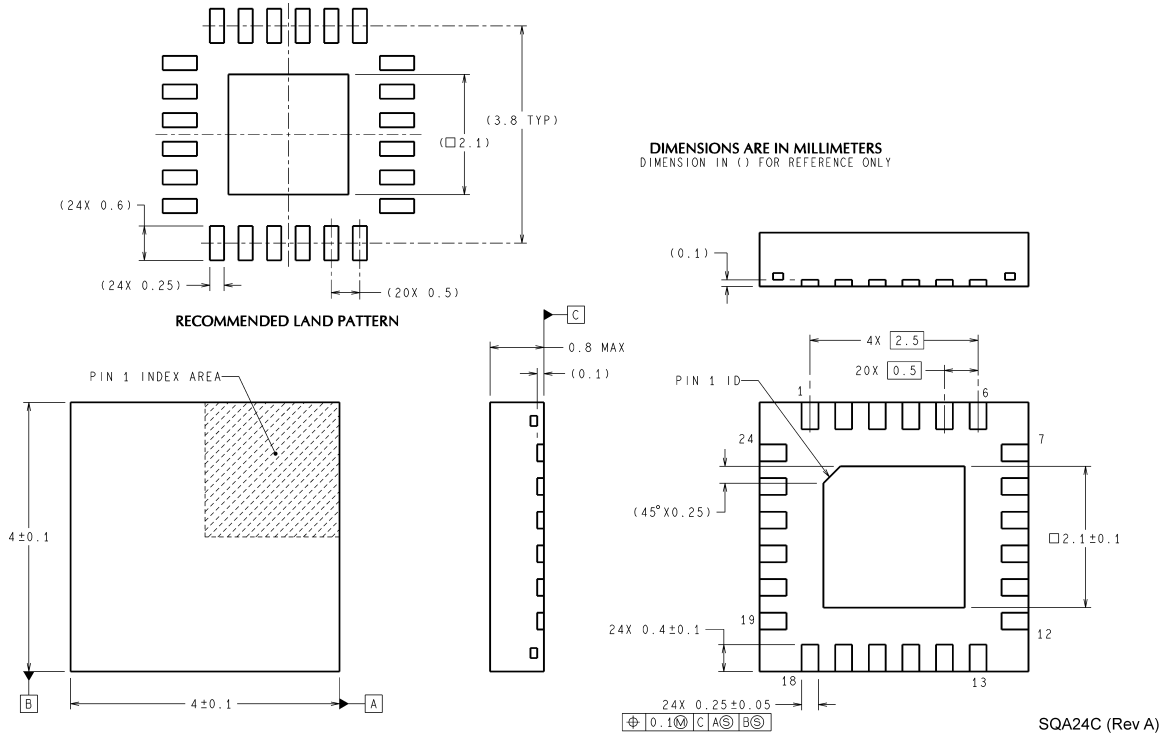


FIGURE 9. Methods to Reduce I_Q When LEDs Are Off



Physical Dimensions inches (millimeters) unless otherwise noted



NOTES: UNLESS OTHERWISE SPECIFIED

1. FOR LEAD FINISH THICKNESS AND COMPOSITION. SEE "SOLDER INFORMATION" IN THE PACKAGING SECTION OF THE NATIONAL SEMICONDUCTOR WEB PAGE (www.national.com).
2. NO JEDEC REGISTRATION AS OF MARCH 2003.

Order Number LP3944ISQ or LP3944ISQX
NS Package Number SQA24C

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