National Semiconductor

LM3409 / LM3409HV
LM3409Q / LM3409QHV

April 12, 2010

PFET Buck Controller for High Power LED Drivers

General Description

The LM3409/09HV are P-channel MosFET (PFET) controllers for step-down (buck) current regulators. They offer wide input voltage range, high-side differential current sense with low adjustable threshold voltage, fast output enable/disable function and a thermally enhanced eMSOP-10 package. These features combine to make the LM3409/09HV ideal for use as constant current sources for driving LEDs where forward currents up to 5A are easily achievable. The LM3409/09Q/09HV/09QHV uses Constant Off-Time (COFT) control to regulate an accurate constant current without the need for external control loop compensation. Analog and PWM dimming are easy to implement and result in a highly linear dimming range with excellent achievable contrast ratios. Programmable UVLO, low-power shutdown, and thermal shutdown complete the feature set.

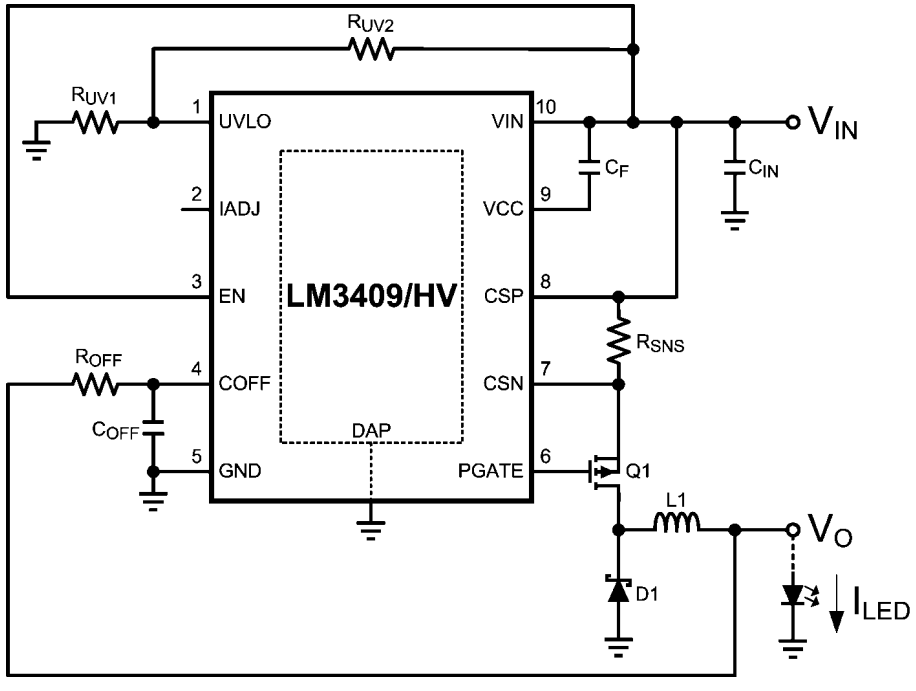
Features

- LM3409Q/LM3409QHV is an Automotive Grade product that is AEC-Q100 grade 1 qualified
- 2Ω, 1A Peak MosFET Gate Drive
- V_{IN} Range: 6V to 42V (LM3409/LM3409Q)
- V_{IN} Range: 6V to 75V (LM3409HV/LM3409QHV)
- Differential, High-side Current Sense
- Cycle-by-Cycle Current Limit
- No Control Loop Compensation Required
- 10,000:1 PWM Dimming Range
- 250:1 Analog Dimming Range
- Supports All-Ceramic Output Capacitors and Capacitorless Outputs
- Low Power Shutdown
- Thermal Shutdown Protection
- Thermally Enhanced eMSOP-10 Package

Applications

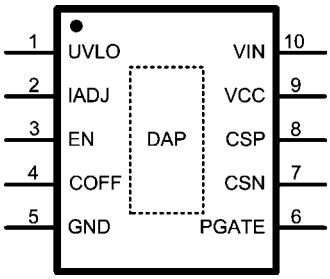
- LED Driver
- Constant Current Source
- Automotive Lighting
- General Illumination
- Industrial Lighting

Typical Application



Connection Diagram

LM3409/09Q/09HV/09QHV



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10-Lead Exposed Pad eMSOP Package

Ordering Information

Order Number	NSC Package Drawing	Top Marking	Supplied As	Feature
LM3409MY	MUC10A	SXFB	1000 Units on tape and reel	
LM3409MYX	MUC10A	SXFB	3500 Units on tape and reel	
LM3409HVMY	MUC10A	SYHB	1000 Units on tape and reel	
LM3409HVMYX	MUC10A	SYHB	3500 Units on tape and reel	
LM3409QMY	MUC10A	SZDB	1000 Units on tape and reel	AEC-Q100 Grade 1 qualified. Automotive Grade Production Flow*
LM3409QMYX	MUC10A	SZDB	3500 Units on tape and reel	
LM3409QHVMY	MUC10A	SZEB	1000 Units on tape and reel	
LM3409QHVMYX	MUC10A	SZEB	3500 Units on tape and reel	

*Automotive Grade (Q) product incorporates enhanced manufacturing and support processes for the automotive market, including defect detection methodologies. Reliability qualification is compliant with the requirements and temperature grades defined in the AEC-Q100 standard. Automotive grade products are identified with the letter Q. For more information go to http://www.national.com/automotive.

Pin Descriptions

Pin(s)	Name	Description	Application Information
1	UVLO	Input under-voltage lockout	Connect to a resistor divider from V_{IN} and GND. Turn-on threshold is 1.24V and hysteresis for turn-off is provided by a 22µA current source.
2	IADJ	Analog LED current adjust	Apply a voltage between 0 - 1.24V, connect a resistor to GND, or leave open to set the current sense threshold voltage.
3	EN	Logic level enable / PWM dimming	Apply a voltage >1.74V to enable device, a PWM signal to dim, or a voltage <0.5V for low power shutdown.
4	COFF	Off-time programming	Connect a resistor from V_O, and a capacitor from GND to set the off-time.
5	GND	Ground	Connect to the system ground.
6	PGATE	Gate drive	Connect to the gate of the external PFET.
7	CSN	Negative current sense	Connect to the negative side of the sense resistor.
8	CSP	Positive current sense	Connect to the positive side of the sense resistor (also connected to VIN).
9	VCC	V_{IN}- referenced linear regulator output	Connect at least a 1µF ceramic capacitor to V_{IN}. The regulator provides power for the PFET drive.
10	VIN	Input voltage	Connect to the input voltage.
DAP	DAP	Thermal pad on bottom of IC	Connect to pin 5 (GND). Place 4-6 vias from DAP to bottom layer GND plane.

Absolute Maximum Ratings

LM3409/09Q/09HV/09QHV (*Note 1*)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

VIN, EN, UVLO to GND	-0.3V to 45V (76V LM3409HV/ 09QHV)
VIN to VCC, PGATE	-0.3V to 7V
VIN to PGATE	-2.8V for 100ns 9.5V for 100ns
VIN to CSP, CSN	-0.3V to 0.3V
COFF to GND	-0.3V to 4V
COFF current	±1 mA continuous
IADJ Current	±5 mA continuous
Junction Temperature	150°C
Storage Temp. Range	-65°C to 125°C
ESD Rating (*Note 2*)	
LM3409/09HV	1 kV
LM3409Q/09QHV	2 kV
Soldering Information	
Lead Temperature (Soldering, 10sec)	260°C
Infrared/Convection Reflow (15sec)	260°C

Operating Ratings (LM3409/09Q/ 09HV/09QHV)

(*Note 1*)

VIN	6V to 42V (75V LM3409HV/ 09QHV)
Junction Temperature Range	–40°C to +125°C
Thermal Resistance θ_{JA} (eMSOP-10 Package) (*Note 5*)	50°C/W

Electrical Characteristics

V_{IN} = 24V unless otherwise indicated. Typicals and limits appearing in plain type apply for $T_A = T_J$ = +25°C (*Note 3*). Limits appearing in **boldface type** apply over full Operating Temperature Range. Datasheet min/ max specification limits are guaranteed by design, test, or statistical analysis.

LM3409/09Q/09HV/09QHV

Symbol	Parameter	Conditions	Min (*Note 4*)	Typ (*Note 3*)	Max (*Note 4*)	Units
PEAK CURRENT COMPARATOR						
V_{CST}	$V_{CSP} – V_{CSN}$ average peak current threshold (*Note 6*)	V_{ADJ} = 1.0V	**188**	198	**208**	mV
		$V_{ADJ} = V_{ADJ-OC}$	**231**	246	**261**	
A_{ADJ}	V_{ADJ} to $V_{CSP} – V_{CSN}$ threshold gain	0.1 < V_{ADJ} < 1.2V $V_{ADJ} = V_{ADJ-OC}$		0.2		V/V
V_{ADJ-OC}	IADJ pin open circuit voltage		**1.189**	1.243	**1.297**	V
I_{ADJ}	IADJ pin current		**3.8**	5	**6.4**	µA
t_{DEL}	CSN pin falling delay	CSN fall - PGATE rise		38		ns
SYSTEM CURRENTS						
I_{IN}	Operating current	Not switching		2		mA
I_{SD}	Shutdown hysteresis current	EN = 0V		110		µA
PFET DRIVER						
R_{PGATE}	Driver output resistance	Sourcing 50 mA		2		Ω
		Sinking 50 mA		2		
VCC REGULATOR						
V_{CC}	VIN pin voltage - VCC pin voltage	V_{IN} > 9V 0 < I_{CC} < 20 mA	**5.5**	6	**6.5**	V
$V_{CC-UVLO}$	V_{CC} under voltage lockout threshold	V_{CC} increasing		3.73		V
V_{CC-HYS}	V_{CC} UVLO hysteresis	V_{CC} decreasing		283		mV
I_{CC-LIM}	V_{CC} regulator current limit		**30**	45		mA

Symbol	Parameter	Conditions	Min (Note 4)	Typ (Note 3)	Max (Note 4)	Units
OFF-TIMER AND ON-TIMER						
V_{OFT}	Off-time threshold		**1.122**	1.243	**1.364**	V
t_{D-OFF}	COFF threshold to PGATE falling delay			25		ns
t_{ON-MIN}	Minimum on-time			115	**211**	ns
$t_{OFF-MAX}$	Maximum off-time			300		µs
UNDER VOLTAGE LOCKOUT						
I_{UVLO}	UVLO pin current	V_{UVLO} = 1V		10		nA
V_{UVLO-R}	Rising UVLO threshold		**1.175**	1.243	**1.311**	V
$I_{UVLO-HYS}$	UVLO hysteresis current			22		µA
ENABLE						
I_{EN}	EN pin current			10		nA
V_{EN-TH}	EN pin threshold	V_{EN} rising			**1.74**	V
		V_{EN} falling	**.5**			
V_{EN-HYS}	EN pin hysteresis			420		mV
t_{EN-R}	EN pin rising delay	EN rise - PGATE fall		42		ns
t_{EN-F}	EN pin falling delay	EN fall - PGATE rise		21		ns
THERMAL RESISTANCE						
θ_{JA}	Junction to Ambient	eMSOP-10 Package (Note 5)		50		°C/W

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Operating Ratings is not implied. The recommended Operating Ratings indicate conditions at which the device is functional and the device should not be operated beyond such conditions.

Note 2: The human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin.

Note 3: Typical values represent most likely parametric norms at the conditions specified and are not guaranteed.

Note 4: Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

Note 5: θ_{JA} of 50°C/W with DAP soldered to a minimum of 2 square inches of 1oz. copper on the top or bottom PCB layer. Actual value will be different depending upon the application enviroment.

Note 6: The current sense threshold limits are calculated by averaging the results from the two polarities of the high-side differential amplifier.

Note 7: The measurements were made using the Bill of Materials from Design #3.

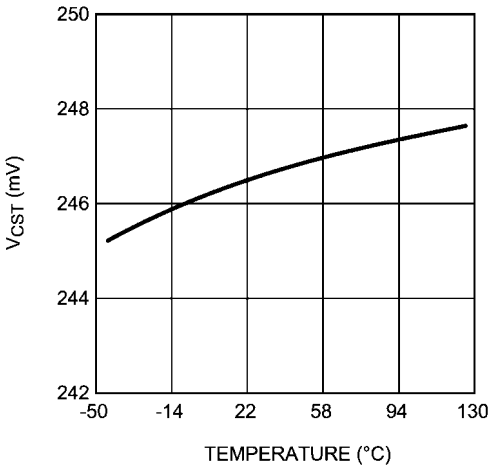
Note 8: The measurements were made using the Bill of Materials from Design #3 except the LM3409 was substituted for the LM3409HV.

Note 9: The waveforms were acquired using the standard evaluation board from AN-1953.

Typical Performance Characteristics

T_A = +25°C, V_{IN} = 24V, and characteristics are identical for LM3409 and LM3409HV unless otherwise specified.

V_{CST} vs. Junction Temperature



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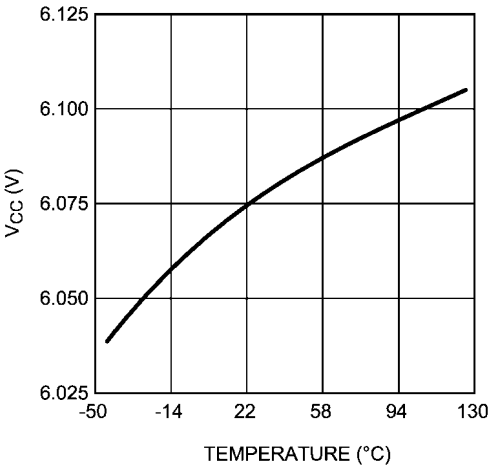
V_{CC} vs. Junction Temperature



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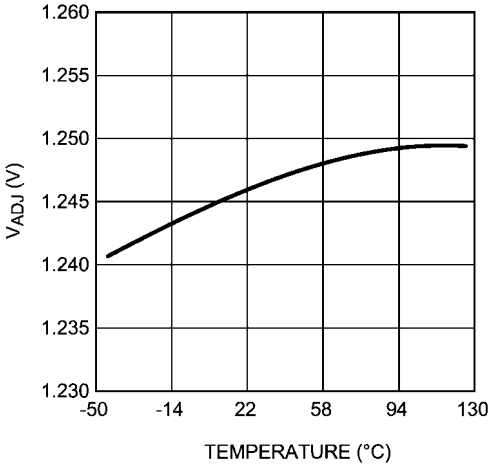
V_{ADJ} vs. Junction Temperature



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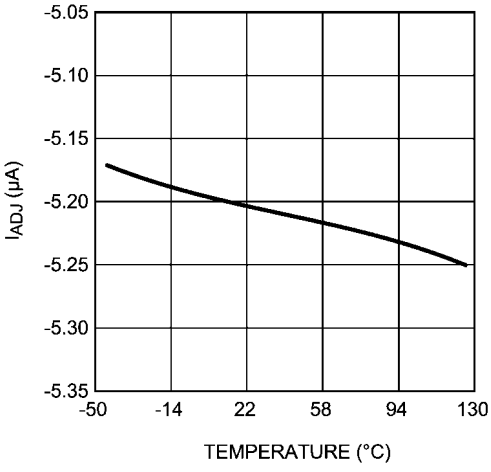
I_{ADJ} vs. Junction Temperature



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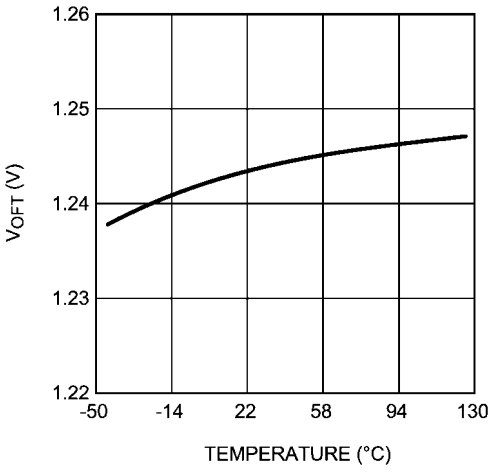
V_{OFT} vs. Junction Temperature



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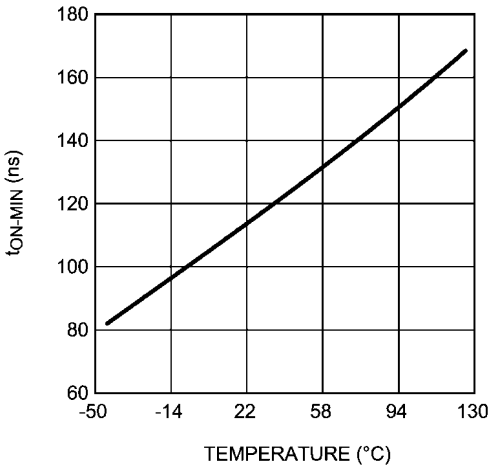
t_{ON-MIN} vs. Junction Temperature



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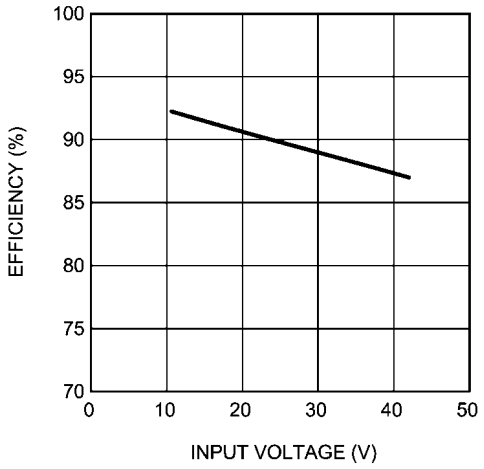
LM3409 Efficiency vs. Input Voltage
V_O = 17V (5 LEDs); I_{LED} = 2A (*Note 8*)



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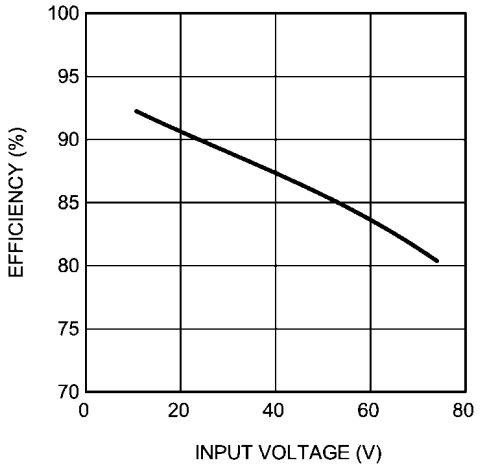
LM3409HV Efficiency vs. Input Voltage
V_O = 17V (5 LEDs); I_{LED} = 2A (*Note 7*)



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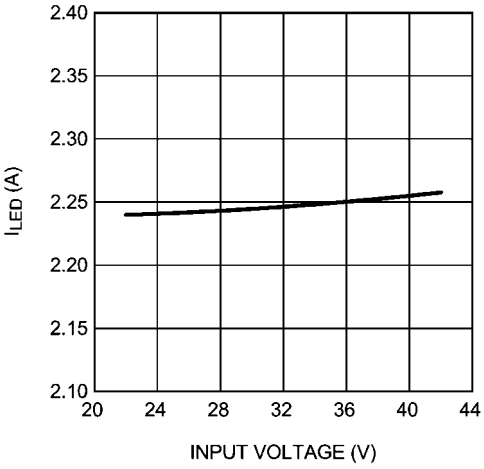
LM3409 LED Current vs. Input Voltage
V_O = 17V (5 LEDs) (*Note 8*)



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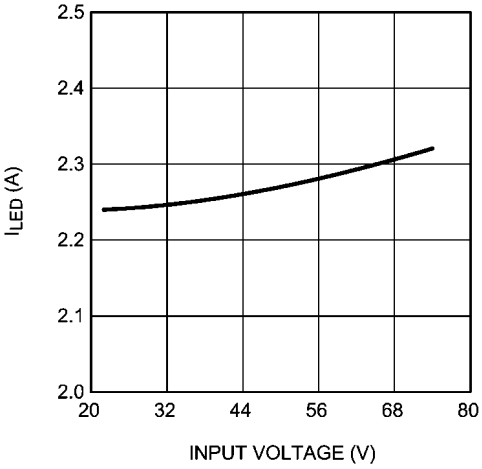
LM3409HV LED Current vs. Input Voltage
V_O = 17V (5 LEDs) (*Note 7*)



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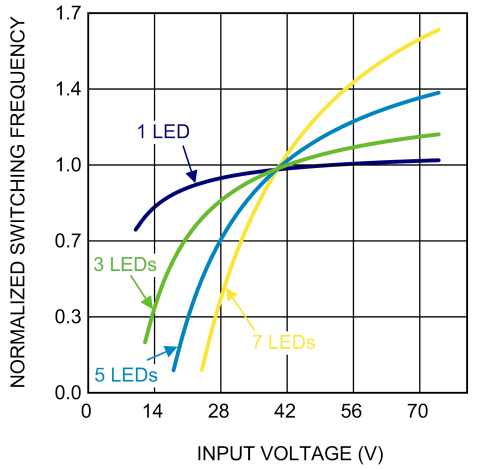
Normalized Switching Frequency vs. Input Voltage



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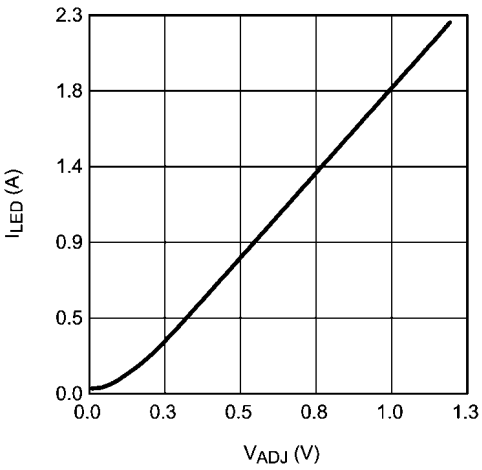
Amplitude Dimming Using IADJ Pin
V_O = 17V (5 LEDs); V_{IN} = 24V



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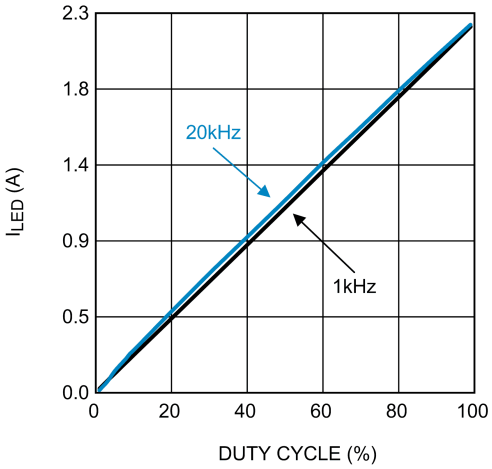
Internal EN Pin PWM Dimming
V_O = 17V (5 LEDs); V_{IN} = 24V



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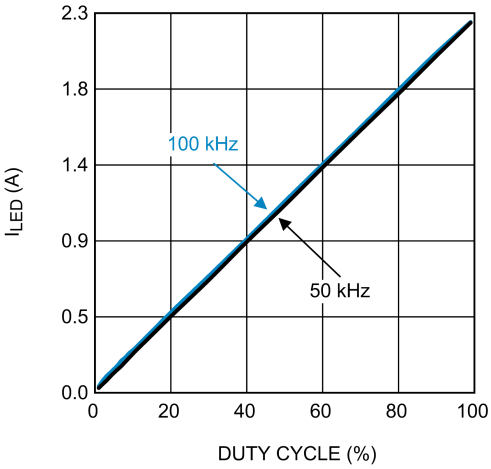
External Parallel FET PWM Dimming
V_O = 17V (5 LEDs); V_{IN} = 24V



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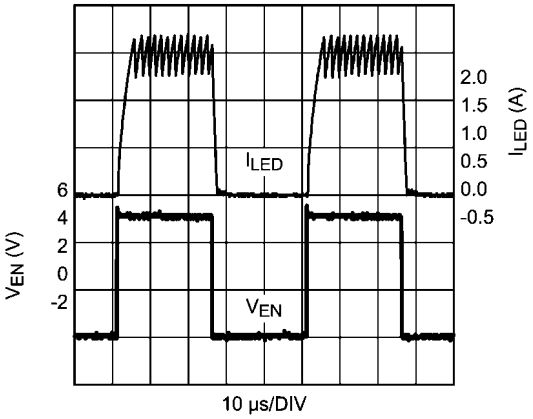
20kHz 50% EN pin PWM dimming
V_O = 42V (12 LEDs); V_{IN} = 48V (*Note 9*)



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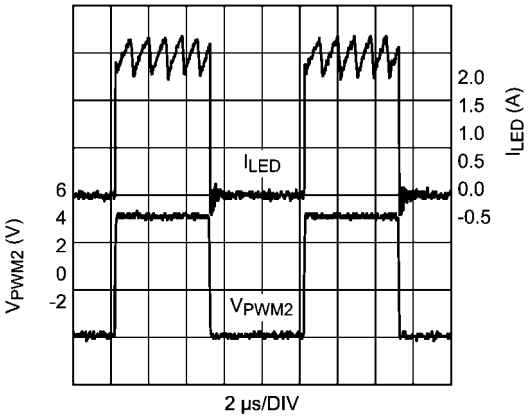
100kHz 50% External FET PWM dimming
V_O = 42V (12 LEDs); V_{IN} = 48V (*Note 9*)



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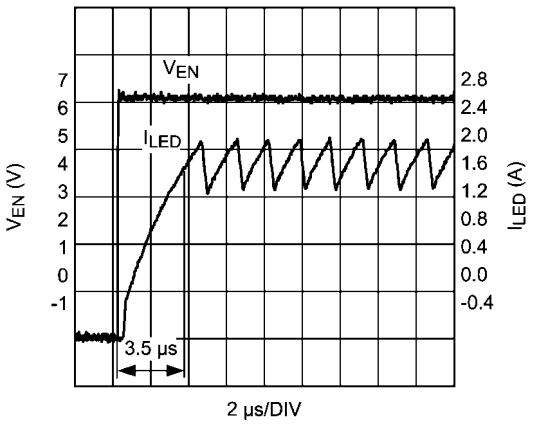
20kHz 50% EN pin PWM dimming (rising edge)
V_O = 42V (12 LEDs); V_{IN} = 48V (*Note 9*)



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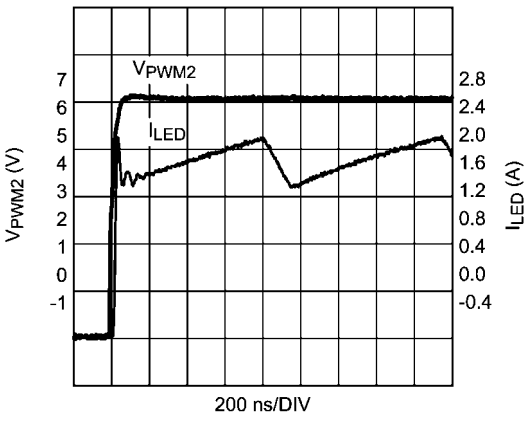
100kHz 50% External FET PWM dimming (rising edge)
V_O = 42V (12 LEDs); V_{IN} = 48V (*Note 9*)



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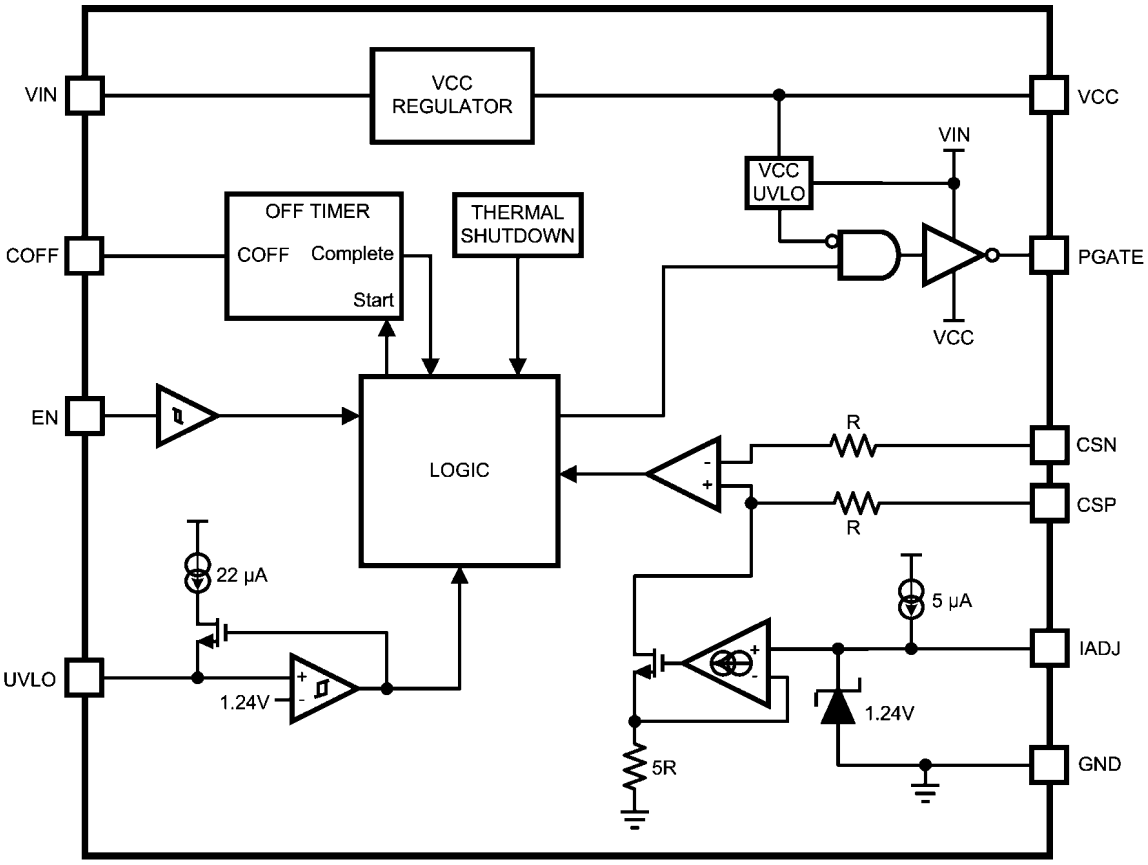
Block Diagram



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Theory of Operation

The LM3409/09HV are P-channel MosFET (PFET) controllers for step-down (buck) current regulators which are ideal for driving LED loads. They have wide input voltage range allowing for regulation of a variety of LED loads. The high-side differential current sense, with low adjustable threshold voltage, provides an excellent method for regulating output current while maintaining high system efficiency. The LM3409/09HV uses a Controlled Off-Time (COFT) architecture that allows the converter to be operated in both continuous conduction mode (CCM) and discontinuous conduction mode (DCM) with no external control loop compensation, while providing an inherent cycle-by-cycle current limit. The adjustable current sense threshold provides the capability to amplitude (analog) dim the LED current over the full range and the fast output enable/disable function allows for high frequency PWM dimming using no external components. When designing, the maximum attainable LED current is not internally limited because the LM3409/09HV is a controller. Instead it is a function of the system operating point, component choices, and switching frequency allowing the LM3409/09HV to easily provide constant currents up to 5A. This simple controller contains all the features necessary to implement a high efficiency versatile LED driver.

BUCK CURRENT REGULATORS

The buck regulator is unique among non-isolated topologies due to the direct connection of the inductor to the load during the entire switching cycle. An inductor will control the rate of change of current that flows through it, therefore a direct connection to the load is excellent for current regulation. A buck current regulator, using the LM3409/09HV, is shown in the *Typical Application* section on the first page of this datasheet. During the time that the PFET (Q1) is turned on (t_{ON}), the input voltage charges up the inductor (L1). When Q1 is turned off (t_{OFF}), the re-circulating diode (D1) becomes forward biased and L1 discharges. During both intervals, the current is supplied to the load keeping the LEDs forward biased. *Figure 1* shows the inductor current ($i_L(t)$) waveform for a buck converter operating in CCM.

The average inductor current (I_L) is equal to the average output LED current (I_{LED}), therefore if I_L is tightly controlled, I_{LED} will be well regulated. As the system changes input voltage or output voltage, duty cycle (D) is varied to regulate I_L and ultimately I_{LED}. For any buck regulator, D is simply the conversion ratio divided by the efficiency (η):

$$D = \frac{V_O}{\eta \times V_{IN}}$$

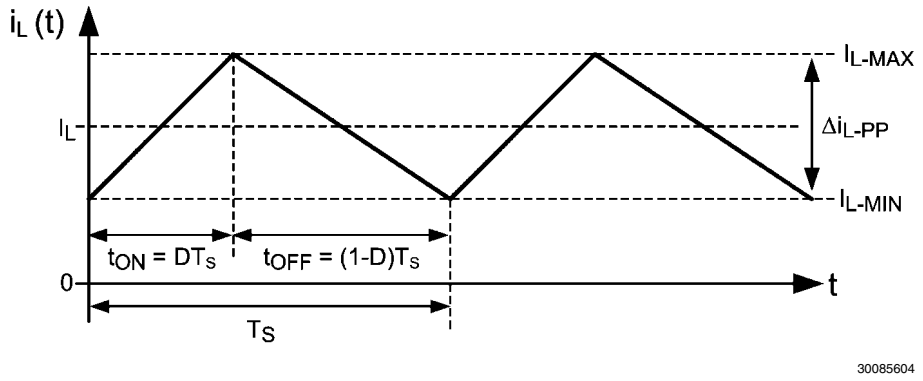


FIGURE 1. Ideal CCM Buck Converter Inductor Current $i_L(t)$

CONTROLLED OFF-TIME (COFT) ARCHITECTURE

The COFT architecture is used by the LM3409/09HV to control I_{LED}. It is a combination of peak current detection and a one-shot off-timer that varies with output voltage. D is indirectly controlled by changes in both t_{OFF} and t_{ON}, which vary depending on the operating point. This creates a variable switching frequency over the entire operating range. This type of hysteretic control eliminates the need for control loop compensation necessary in many switching regulators, simplifying the design process and providing fast transient response.

Adjustable Peak Current Control

At the beginning of a switching period, PFET Q1 is turned on and inductor current increases. Once peak current is detected, Q1 is turned off, the diode D1 forward biases, and inductor current decreases. *Figure 2* shows how peak current detection is accomplished using the differential voltage signal created as current flows through the current setting resistor (R_{SNS}). The voltage across R_{SNS} (V_{SNS}) is compared to the adjustable current sense threshold (V_{CST}) and Q1 is turned off when V_{SNS} exceeds V_{CST}, providing that t_{ON} is greater than the minimum possible t_{ON} (typically 115ns).

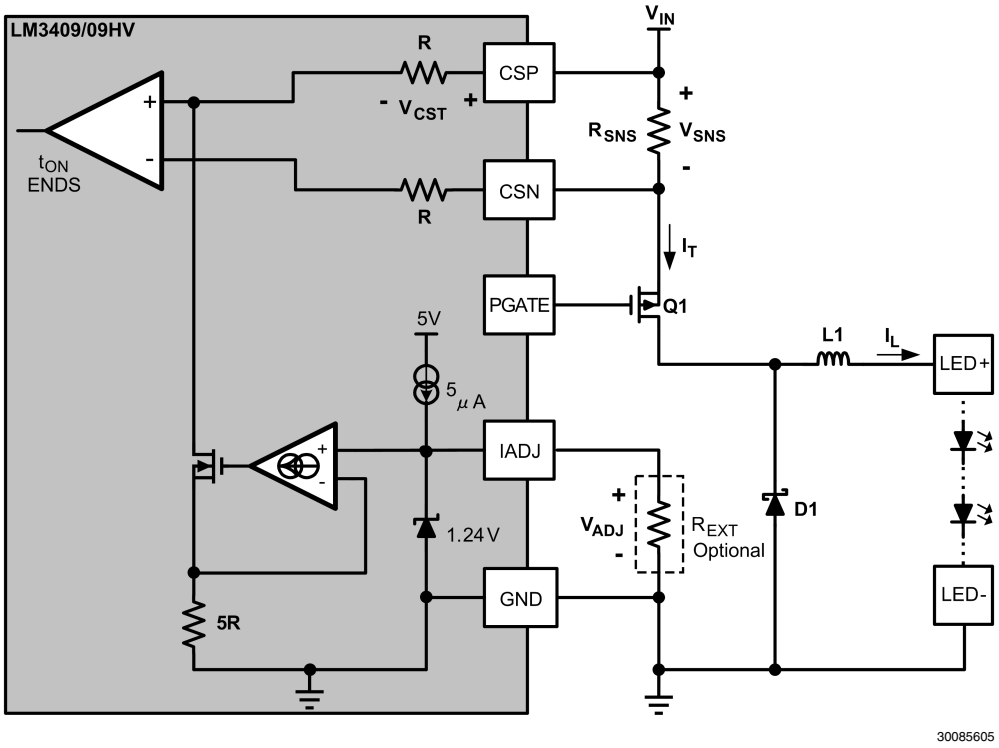


FIGURE 2. Peak Current Control Circuit

There are three different methods to set the current sense threshold (V_{CST}) using the multi-function IADJ pin:

1. IADJ pin left open: 5µA internal current source biases the Zener diode and clamps the IADJ pin voltage (V_{ADJ}) at 1.24V causing the maximum threshold voltage:

$$V_{CST} = \frac{V_{ADJ}}{5 \times R} \times R = \frac{V_{ADJ}}{5} = \frac{1.24V}{5} = 248\ mV$$

2. External voltage (V_{ADJ}) of 0V to 1.24V: Apply to the IADJ pin to adjust V_{CST} from 0V to 248mV. If the V_{ADJ} voltage is adjustable, analog dimming can be achieved.
3. External resistor (R_{EXT}) placed from IADJ pin to ground: 5µA current source sets the V_{ADJ} voltage and corresponding threshold voltage:

$$V_{CST} = \frac{V_{ADJ}}{5} = \frac{5\,\mu A \times R_{EXT}}{5} = 1\,\mu A \times R_{EXT}$$

Controlled Off-Time

Once Q1 is turned off, it remains off for a constant time (t_{OFF}) which is preset by an external resistor (R_{OFF}), an external capacitor (C_{OFF}), and the output voltage (V_O) as shown in *Figure 3*. Since I_{LED} is tightly regulated, V_O will remain nearly constant over widely varying input voltage and temperature yielding a nearly constant t_{OFF}.

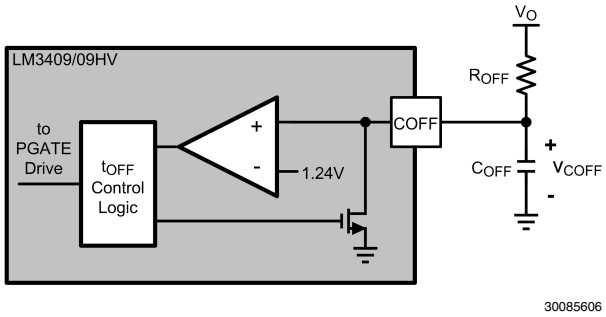


FIGURE 3. Off-Time Control Circuit

At the start of t_{OFF}, the voltage across C_{OFF} ($v_{COFF}(t)$) is zero and the capacitor begins charging according to the time constant provided by R_{OFF} and C_{OFF}. When $v_{COFF}(t)$ reaches the off-time threshold (V_{OFT} = 1.24V), then the off-time is terminated and $v_{COFF}(t)$ is reset to zero. t_{OFF} is calculated as follows:

$$t_{OFF} = -R_{OFF} \times (C_{OFF} + 20\ pF) \times \ln\left(1 - \frac{1.24V}{V_O}\right)$$

In reality, there is typically 20 pF parasitic capacitance at the off-timer pin in parallel with C_{OFF}, which is accounted for in the calculation of t_{OFF}. Also, it should be noted that the t_{OFF} equation has a preceding negative sign because the result of the logarithm should be negative for a properly designed circuit. The resulting t_{OFF} is a positive value as long as V_O > 1.24V. If V_O < 1.24V, the off-timer cannot reach V_{OFT} and an internally limited maximum off-time (typically 300µs) will occur.

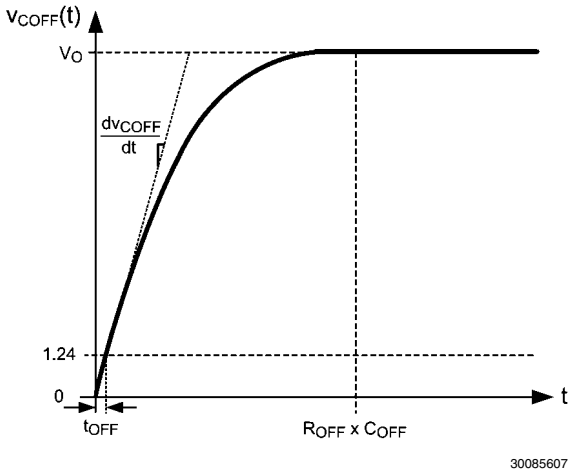


FIGURE 4. Exponential Charging Function $v_{COFF}(t)$

Although the t_{OFF} equation is non-linear, t_{OFF} is actually very linear in most applications. Ignoring the 20pF parasitic capacitance at the COFF pin, $v_{COFF}(t)$ is plotted in *Figure 4*. The time derivative of $v_{COFF}(t)$ can be calculated to find a linear approximation to the t_{OFF} equation:

$$\frac{dv_{COFF}(t)}{dt} = \frac{V_O}{R_{OFF} \times C_{OFF}}\, e^{-\left(\frac{t_{OFF}}{R_{OFF} \times C_{OFF}}\right)}$$

When $t_{OFF} << R_{OFF} \times C_{OFF}$ (equivalent to when $V_O >> 1.24V$), the slope of the function is essentially linear and t_{OFF} can be approximated as a current source charging C_{OFF}:

$$t_{OFF} \approx \frac{1.24V \times R_{OFF} \times C_{OFF}}{V_O}$$

Using the actual t_{OFF} equation, the inductor current ripple ($\Delta i_{L\text{-}PP}$) of a buck current regulator operating in CCM is:

$$\Delta i_{L\text{-}PP} = \frac{-V_O \times R_{OFF} \times (C_{OFF} + 20\ pF) \times \ln\left(1 - \frac{1.24V}{V_O}\right)}{L1}$$

Using the t_{OFF} approximation, the equation is reduced to:

$$\Delta i_{L\text{-}PP} \approx \frac{1.24 \times R_{OFF} \times C_{OFF}}{L1}$$

$\Delta i_{L\text{-}PP}$ is independent of both V_{IN} and V_O when in CCM!
The $\Delta i_{L\text{-}PP}$ approximation only depends on R_{OFF}, C_{OFF}, and L1, therefore the ripple is essentially constant over the operating range as long as $V_O >> 1.24V$ (when the t_{OFF} approximation is valid). An exception to the t_{OFF} approximation occurs if the IADJ pin is used to analog dim. As the LED/inductor current decreases, the converter will eventually enter DCM and the ripple will decrease with the peak current threshold. The approximation shows how the LM3409/09HV achieves constant ripple over a wide operating range, however t_{OFF} should be calculated using the actual equation first presented.

AVERAGE LED CURRENT

For a buck converter, the average LED current is simply the average inductor current.

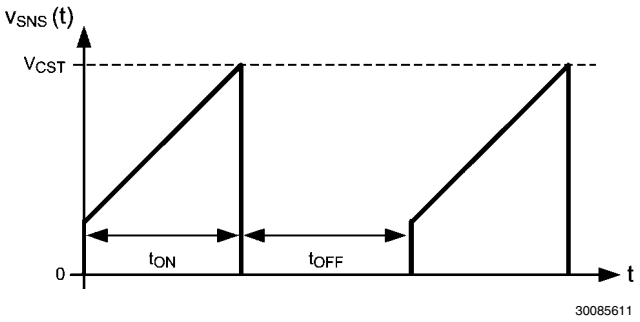


FIGURE 5. Sense Voltage $v_{SNS}(t)$

Using the COFT architecture, the peak transistor current ($I_{T\text{-}MAX}$) is sensed as shown in *Figure 5*, which is equal to the peak inductor current ($I_{L\text{-}MAX}$) given by the following equation:

$$I_{L\text{-}MAX} = I_{T\text{-}MAX} = \frac{V_{CST}}{R_{SNS}} = \frac{V_{ADJ}}{5 \times R_{SNS}}$$

Because $I_{L\text{-}MAX}$ is set using peak current control and $\Delta i_{L\text{-}PP}$ is set using the controlled off-timer, I_L and correspondingly I_{LED} can be calculated as follows:

$$I_{LED} = I_L = I_{L\text{-}MAX} - \frac{\Delta i_{L\text{-}PP}}{2} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{V_O \times t_{OFF}}{2 \times L1}$$

The threshold voltage V_{CST} seen by the high-side sense comparator is affected by the comparator's input offset voltage, which causes an error in the calculation of $I_{L\text{-}MAX}$ and ultimately I_{LED}. To mitigate this problem, the polarity of the comparator inputs is swapped every cycle, which causes the actual $I_{L\text{-}MAX}$ to alternate between two peak values ($I_{L\text{-}MAXH}$ and $I_{L\text{-}MAXL}$), equidistant from the theoretical $I_{L\text{-}MAX}$ as shown in *Figure 6*. I_{LED} remains accurate through this averaging.

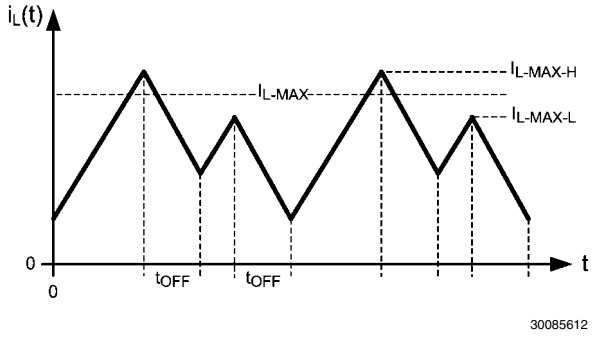


FIGURE 6. Inductor Current $i_L(t)$ Showing $I_{L\text{-}MAX}$ Offset

INDUCTOR CURRENT RIPPLE

Because the LM3409/09HV swaps the polarity of the differential current sense comparator every cycle, a minimum inductor current ripple ($\Delta i_{L\text{-}PP}$) is necessary to maintain accurate I_{LED} regulation. Referring to *Figure 6*, the first t_{ON} is terminated at the higher of the two polarity-swapped thresholds (corresponding to $I_{L\text{-}MAXH}$). During the following t_{OFF}, i_L decreases until the second t_{ON} begins. If t_{OFF} is too short, then as the second t_{ON} begins, i_L will still be above the lower peak current threshold (corresponding to $I_{L\text{-}MAXL}$) and a minimum t_{ON} pulse will follow. This will result in degraded I_{LED} regulation. The minimum inductor current ripple ($\Delta i_{L\text{-}PP\text{-}MIN}$) should adhere to the following equation in order to ensure accurate I_{LED} regulation:

$$\Delta i_{L\text{-}PP\text{-}MIN} > \frac{24\ mV}{R_{SNS}}$$

SWITCHING FREQUENCY

The switching frequency is dependent upon the actual operating point (V_{IN} and V_O). V_O will remain relatively constant for a given application, therefore the switching frequency will vary with V_{IN} (frequency increases as V_{IN} increases). The target switching frequency (f_{SW}) at the nominal operating point is selected based on the tradeoffs between efficiency (better at low frequency) and solution size/cost (smaller at high frequency). The off-time of the LM3409/09HV can be programmed for switching frequencies up to 5 MHz (theoretical limit imposed by minimum t_{ON}). In practice, switching frequencies higher than 1MHz may be difficult to obtain due to gate drive limitations, high input voltage, and thermal considerations.

At CCM operating points, f_{SW} is defined as:

$$f_{SW} = \frac{1 - D}{t_{OFF}} = \frac{1 - \left(\frac{V_O}{\eta \times V_{IN}}\right)}{t_{OFF}}$$

At DCM operating points, f_{SW} is defined as:

$$f_{SW} = \frac{1}{t_{ON} + t_{OFF}} = \frac{1}{\left(\frac{I_{L\text{-}MAX} \times L_1}{V_{IN} - V_O}\right) + t_{OFF}}$$

In the CCM equation, it is apparent that the efficiency (η) factors into the switching frequency calculation. Efficiency is hard to estimate and, since switching frequency varies with input voltage, accuracy in setting the nominal switching frequency is not critical. Therefore, a general rule of thumb for the LM3409/09HV is to assume an efficiency between 85% and 100%. When approximating efficiency to target a nominal switching frequency, the following condition must be met:

$$\eta > \frac{V_O}{V_{IN}}$$

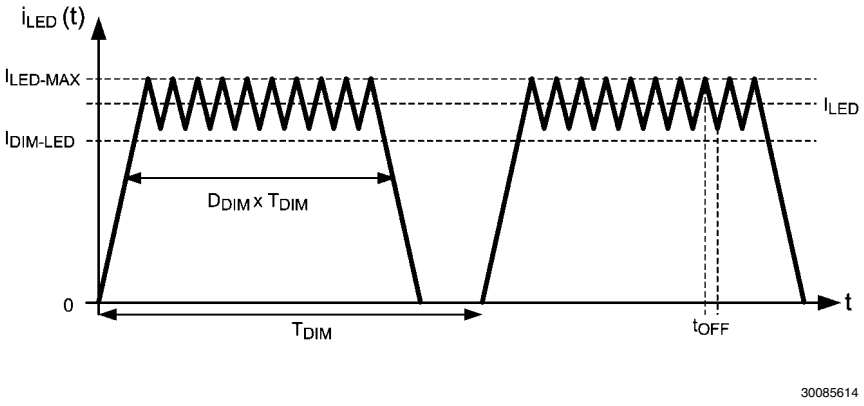


FIGURE 7. LED Current $i_{LED}(t)$ During EN Pin PWM Dimming

PWM DIMMING USING THE EN PIN

The enable pin (EN) is a TTL compatible input for PWM dimming of the LED. A logic low (below 0.5V) at EN will disable the internal driver and shut off the current flow to the LED array. While the EN pin is in a logic low state the support circuitry (driver, bandgap, V_{CC} regulator) remains active in order to minimize the time needed to turn the LED array back on when the EN pin sees a logic high (above 1.74V).

Figure 7 shows the LED current ($i_{LED}(t)$) during PWM dimming where duty cycle (D_{DIM}) is the percentage of the dimming period (T_{DIM}) that the PFET is switching. For the remainder of T_{DIM}, the PFET is disabled. The resulting dimmed average LED current ($I_{DIM-LED}$) is:

$$I_{DIM-LED} = D_{DIM} \times I_{LED}$$

The LED current rise and fall times (which are limited by the slew rate of the inductor as well as the delay from activation of the EN pin to the response of the external PFET) limit the achievable T_{DIM} and D_{DIM}. In general, dimming frequency should be at least one order of magnitude lower than the steady state switching frequency in order to prevent aliasing. However, for good linear response across the entire dimming range, the dimming frequency may need to be even lower.

HIGH VOLTAGE NEGATIVE BIAS REGULATOR

The LM3409/09HV contains an internal linear regulator where the steady state VCC pin voltage is typically 6.2V below the voltage at the VIN pin. The VCC pin should be bypassed to the VIN pin with at least 1µF of ceramic capacitance connected as close as possible to the IC.

INPUT UNDER-VOLTAGE LOCKOUT (UVLO)

Under-voltage lockout is set with a resistor divider from V_{IN} to GND and is compared against a 1.24V threshold as shown in *Figure 8*. Once the input voltage is above the preset UVLO rising threshold (and assuming the part is enabled), the internal circuitry becomes active and a 22µA current source at the UVLO pin is turned on. This extra current provides hysteresis to create a lower UVLO falling threshold. The resistor divider is chosen to set both the UVLO rising and falling thresholds.

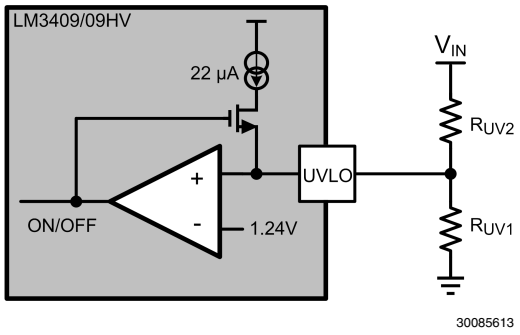


FIGURE 8. UVLO Circuit

The turn-on threshold ($V_{TURN-ON}$) is defined as follows:

$$V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

The hysteresis (V_{HYS}) is defined as follows:

$$V_{HYS} = R_{UV2} \times 22\,\mu A$$

LOW POWER SHUTDOWN

The LM3409/09HV can be placed into a low power shutdown (typically 110µA) by grounding the EN terminal (any voltage below 0.5V) until V_{CC} drops below the V_{CC} UVLO threshold (typically 3.73V). During normal operation this terminal should be tied to a voltage above 1.74V and below absolute maximum input voltage rating.

THERMAL SHUTDOWN

Internal thermal shutdown circuitry is provided to protect the IC in the event that the maximum junction temperature is exceeded. The threshold for thermal shutdown is 160°C with 15°C of hysteresis (both values typical). During thermal shutdown the PFET and driver are disabled.

Design Considerations

OPERATION NEAR DROPOUT

Because the power MosFET is a PFET, the LM3409/09HV can be operated into dropout which occurs when the input voltage is approximately equal to output voltage. Once the input voltage drops below the nominal output voltage, the switch remains constantly on (D=1) causing the output voltage to decrease with the input voltage. In normal operation, the average LED current is regulated to the peak current threshold minus half of the ripple. As the converter goes into dropout, the LED current is exactly at the peak current threshold because it is no longer switching. This causes the LED current to increase by half of the set ripple current as it makes the transition into dropout. Therefore, the inductor current ripple should be kept as small as possible (while remaining above the previously established minimum) and output capacitance should be added to help maintain good line regulation when approaching dropout.

LED RIPPLE CURRENT

Selection of the ripple current through the LED array is analogous to the selection of output ripple voltage in a standard voltage regulator. Where the output voltage ripple in a voltage regulator is commonly ±1% to ±5% of the DC output voltage, LED manufacturers generally recommend values for Δi_{LED-PP} ranging from ±5% to ±20% of I_{LED}. For a nominal system operating point, a larger Δi_{LED-PP} specification can reduce the necessary inductor size and/or allow for smaller output capacitors (or no output capacitors at all) which helps to minimize the total solution size and cost. On the other hand, a smaller Δi_{LED-PP} specification would require more output inductance, a higher switching frequency, or additional output capacitance.

BUCK CONVERTERS W/O OUTPUT CAPACITORS

Because current is being regulated, not voltage, a buck current regulator is free of load current transients, therefore output capacitance is not needed to supply the load and maintain output voltage. This is very helpful when high frequency PWM dimming the LED load. When no output capacitor is used, the same design equations that govern Δi_{L-PP} also apply to Δi_{LED-PP}.

BUCK CONVERTERS WITH OUTPUT CAPACITORS

A capacitor placed in parallel with the LED load can be used to reduce Δi_{LED-PP} while keeping the same average current through both the inductor and the LED array. With an output capacitor, the inductance can be lowered, making the magnetics smaller and less expensive. Alternatively, the circuit can be run at lower frequency with the same inductor value, improving the efficiency and increasing the maximum allowable average output voltage. A parallel output capacitor is also useful in applications where the inductor or input voltage tolerance is poor. Adding a capacitor that reduces Δi_{LED-PP} to well below the target provides headroom for changes in inductance or V_{IN} that might otherwise push the maximum Δi_{LED-PP} too high.

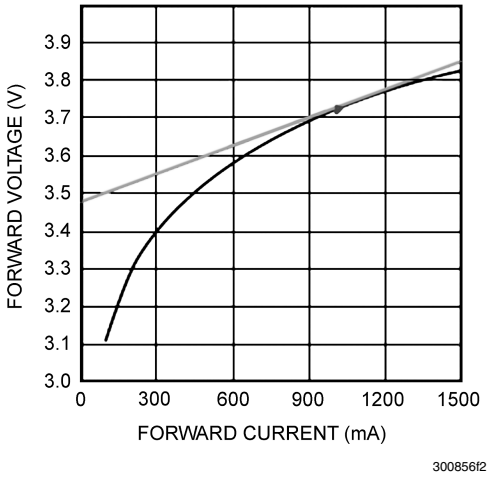


FIGURE 9. Calculating Dynamic Resistance r_D

Output capacitance (C_O) is determined knowing the desired Δi_{LED-PP} and the LED dynamic resistance (r_D). r_D can be calculated as the slope of the LED's exponential DC characteristic at the nominal operating point as shown in *Figure 9*. Simply dividing the forward voltage by the forward current at the nominal operating point will give an incorrect value that is 5x to 10x too high. Total dynamic resistance for a string of n LEDs connected in series can be calculated as the r_D of one device multiplied by n. The following equations can then be used to estimate Δi_{LED-PP} when using a parallel capacitor:

$$\Delta i_{LED-PP} = \frac{\Delta i_{L-PP}}{1 + \frac{r_D}{Z_C}}$$

$$Z_C = \frac{1}{2 \times \pi \times f_{SW} \times C_O}$$

In general, Z_C should be at least half of r_D to effectively reduce the ripple. Ceramic capacitors are the best choice for the output capacitors due to their high ripple current rating, low ESR, low cost, and small size compared to other types. When selecting a ceramic capacitor, special attention must be paid to the operating conditions of the application. Ceramic capacitors can lose one-half or more of their capacitance at their rated DC voltage bias and also lose capacitance with extremes in temperature. Make sure to check any recommended deratings and also verify if there is any significant change in capacitance at the operating voltage and temperature.

OUTPUT OVER-VOLTAGE PROTECTION

Because the LM3409/09HV controls a buck current regulator, there is no inherent need to provide output over-voltage protection. If the LED load is opened, the output voltage will only rise as high as the input voltage plus any ringing due to the parasitic inductance and capacitance present at the output node. If a ceramic output capacitor is used in the application, it should have a minimum rating equal to the input voltage. Ringing seen at the output node should not damage most ceramic capacitors, due to their high ripple current rating.

INPUT CAPACITORS

Input capacitors are selected using requirements for minimum capacitance and RMS ripple current. The PFET current during t_{ON} is approximately I_{LED}, therefore the input capacitors discharge the difference between I_{LED} and the average input current (I_{IN}) during t_{ON}. During t_{OFF}, the input voltage source charges up the input capacitors with I_{IN}. The minimum input capacitance (C_{IN-MIN}) is selected using the maximum input voltage ripple (Δv_{IN-MAX}) which can be tolerated. Δv_{IN-MAX} is equal to the change in voltage across C_{IN} during t_{ON} when it supplies the load current. A good starting point for selection of C_{IN} is to use Δv_{IN-MAX} of 2% to 10% of V_{IN}. C_{IN-MIN} can be selected as follows:

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta v_{IN-MAX}} = \frac{I_{LED} \times \left(\frac{1}{f_{SW}} - t_{OFF}\right)}{\Delta v_{IN-MAX}}$$

An input capacitance at least 75% greater than the calculated C_{IN-MIN} value is recommended. To determine the RMS input current rating (I_{IN-RMS}) the following approximation can be used:

$$I_{IN-RMS} = I_{LED} \times \sqrt{D \times (1 - D)} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

Since this approximation assumes there is no inductor ripple current, the value should be increased by 10-30% depending on the amount of ripple that is expected. Ceramic capacitors are the best choice for input capacitors for the same reasons mentioned in the *Buck Converters with Output Capacitors* section. Careful selection of the capacitor requires checking capacitance ratings at the nominal operating voltage and temperature.

P-CHANNEL MosFET (PFET)

The LM3409/09HV requires an external PFET (Q1) as the main power MosFET for the switching regulator. Q1 should have a voltage rating at least 15% higher than the maximum input voltage to ensure safe operation during the ringing of the switch node. In practice all switching converters have some ringing at the switch node due to the diode parasitic capacitance and the lead inductance. The PFET should also have a current rating at least 10% higher than the average transistor current (I_T):

$$I_T = D \times I_{LED}$$

The power rating is verified by calculating the power loss (P_T) using the RMS transistor current (I_{T-RMS}) and the PFET on-resistance (R_{DS-ON}):

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left(1 + \frac{1}{12} \times \left(\frac{\Delta i_{L-PP}}{I_{LED}}\right)^2\right)}$$

$$P_T = I_{T-RMS}^2 \times R_{DSON}$$

It is important to consider the gate charge of Q1. As the input voltage increases from a nominal voltage to its maximum input voltage, the COFT architecture will naturally increase the switching frequency. The dominant switching losses are determined by input voltage, switching frequency, and PFET total gate charge (Q_g). The LM3409/09HV has to provide and remove charge Q_g from the input capacitance of Q1 in order to turn it on and off. This occurs more often at higher switching frequencies which requires more current from the internal regulator, thereby increasing internal power dissipation and eventually causing the LM3409/09HV to thermally cycle. For a given range of operating points the only effective way to reduce these switching losses is to minimize Q_g.

A good rule of thumb is to limit Q_g < 30nC (if the switching frequency remains below 300kHz for the entire operating range then a larger Q_g can be considered). If a PFET with small R_{DS-ON} and a high voltage rating is required, there may be no choice but to use a PFET with Q_g > 30nC.

When using a PFET with Q_g > 30nC, the bypass capacitor (C_F) should not be connected to the VIN pin. This will ensure that peak current detection through R_{SNS} is not affected by the charging of the PFET input capacitance during switching, which can cause false triggering of the peak detection comparator. Instead, C_F should be connected from the VCC pin to the CSN pin which will cause a small DC offset in V_{CST} and ultimately I_{LED}, however it avoids the problematic false triggering.

In general, the PFET should be chosen to meet the Q_g specification whenever possible, while minimizing R_{DS-ON}. This will minimize power losses while ensuring the part functions correctly over the full operating range.

RE-CIRCULATING DIODE

A re-circulating diode (D1) is required to carry the inductor current during t_{OFF}. The most efficient choice for D1 is a Schottky diode due to low forward voltage drop and near-zero reverse recovery time. Similar to Q1, D1 must have a voltage rating at least 15% higher than the maximum input voltage to ensure safe operation during the ringing of the switch node and a current rating at least 10% higher than the average diode current (I_D):

$$I_D = (1 - D) \times I_{LED}$$

The power rating is verified by calculating the power loss through the diode. This is accomplished by checking the typical diode forward voltage (V_D) from the I-V curve on the product datasheet and calculating as follows:

$$P_D = I_D \times V_D$$

In general, higher current diodes have a lower V_D and come in better performing packages minimizing both power losses and temperature rise.

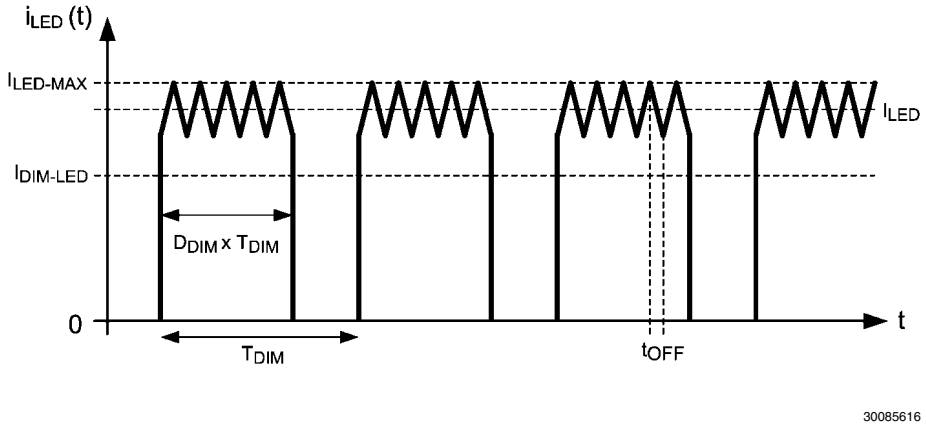


FIGURE 10. Ideal LED Current $i_{LED}(t)$ During Parallel FET Dimming

EXTERNAL PARALLEL FET PWM DIMMING

Any buck topology LED driver is a good candidate for parallel FET dimming because high slew rates are achievable, due to the fact that no output capacitance is required. This allows for much higher dimming frequencies than are achievable using the EN pin. When using external parallel FET dimming, a situation can arise where maximum off-time occurs due to a shorted output. To mitigate this situation, capacitive coupling to the enable pin can be employed.

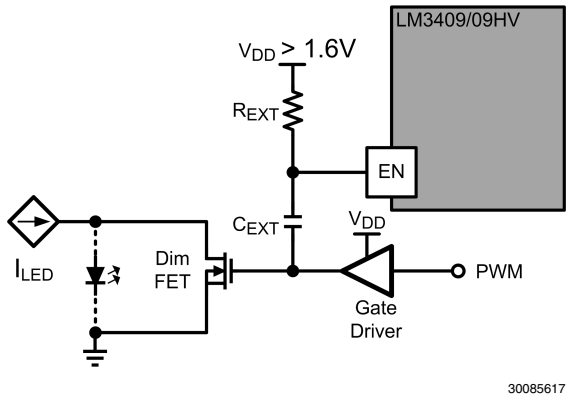


FIGURE 11. External Parallel FET Dimming Circuit

As shown in *Figure 11*, a small capacitor (C_{EXT}) is connected from the gate drive signal of the parallel Dim FET to the EN pin and a pull-up resistor (R_{EXT}) is placed from the EN pin to the external V_{DD} supply for the Dim FET gate driver. This forces the on-timer to restart corresponding to every rising edge of the LED voltage, ensuring that the unwanted maximum off-time condition does not occur. With this type of dimming, the EN pin does not control the dimming; it simply resets the controller. A good design choice is to size R_{EXT} and C_{EXT} to give a time constant smaller than t_{OFF}:

$$t_{OFF} > R_{EXT} \times C_{EXT}$$

The ideal LED current waveform $i_{LED}(t)$ during parallel FET PWM dimming is very similar to the EN pin PWM dimming shown previously. The LED current does not rise and fall infinitely fast as shown in *Figure 10* however with this method, only the speed of the parallel Dim FET ultimately limits the dimming frequency and dimming duty cycle. This allows for much faster PWM dimming than can be attained with the EN pin.

CIRCUIT LAYOUT

The performance of any switching converter depends as much upon the layout of the PCB as the component selection. Following a few simple guidelines will maximimize noise rejection and minimize the generation of EMI within the circuit.

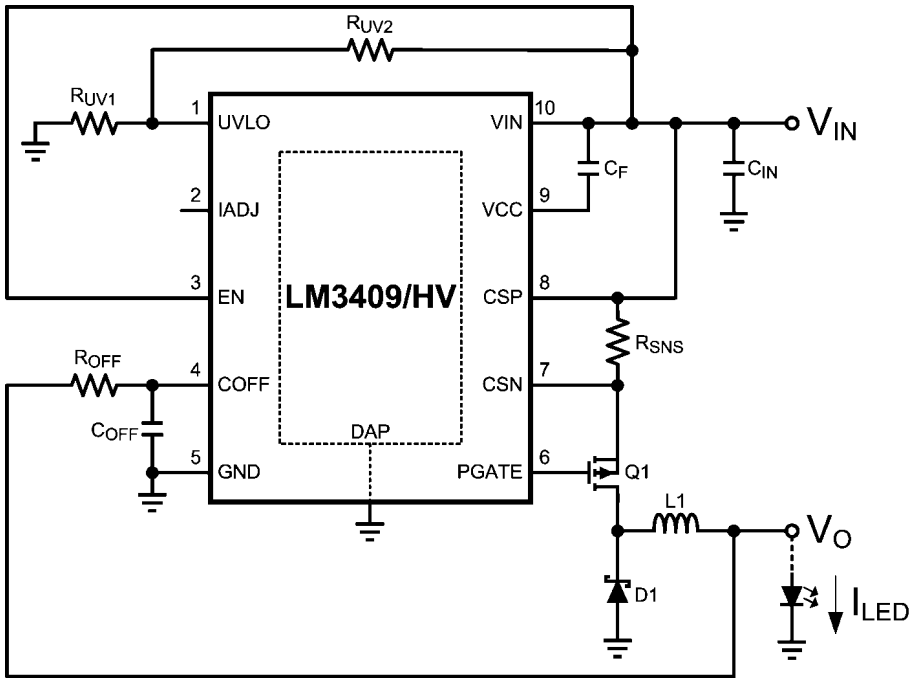
Discontinuous currents are the most likely to generate EMI, therefore care should be taken when routing these paths. The main path for discontinuous current in the LM3409/09HV buck converter contains the input capacitor (C_{IN}), the recirculating diode (D1), the P-channel MosFET (Q1), and the sense resistor (R_{SNS}). This loop should be kept as small as possible and the connections between all three components should be short and thick to minimize parasitic inductance. In particular, the switch node (where L1, D1 and Q1 connect) should be just large enough to connect the components without excessive heating from the current it carries.

The IADJ, COFF, CSN and CSP pins are all high-impedance control inputs which couple external noise easily, therefore the loops containing these high impedance nodes should be minimized. The most sensitive loop contains the sense resistor (R_{SNS}) which should be placed as close as possible to the CSN and CSP pins to maximize noise rejection. The off-time capacitor (C_{OFF}) should be placed close to the COFF and GND pins for the same reason. Finally, if an external resistor (R_{EXT}) is used to bias the IADJ pin, it should be placed close to the IADJ and GND pins, also.

In some applications the LED or LED array can be far away (several inches or more) from the LM3409/09HV, or on a separate PCB connected by a wiring harness. When an output capacitor is used and the LED array is large or separated from the rest of the converter, the output capacitor should be placed close to the LEDs to reduce the effects of parasitic inductance on the AC impedance of the capacitor.

Design Guide

TYPICAL APPLICATION



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SPECIFICATIONS

Nominal input voltage: V_{IN}
Maximum input voltage: V_{IN-MAX}
Nominal output voltage (# of LEDs x forward voltage): V_O
LED string dynamic resistance: r_D
Switching frequency (at nominal V_{IN}, V_O): f_{SW}
Average LED current: I_{LED}
Inductor current ripple: Δi_{L-PP}
LED current ripple: Δi_{LED-PP}
Input voltage ripple: Δv_{IN-PP}
UVLO characteristics: $V_{TURN-ON}$ and V_{HYS}
Expected efficiency: η

1. NOMINAL SWITCHING FREQUENCY

Calculate switching frequency (f_{SW}) at the nominal operating point (V_{IN} and V_O). Assume a C_{OFF} value (between 470pF and 1nF) and a system efficiency (η). Solve for R_{OFF}:

$$R_{OFF} = \frac{-\left(1 - \frac{V_O}{\eta \times V_{IN}}\right)}{(C_{OFF} + 20\ pF) \times f_{SW} \times \ln\left(1 - \frac{1.24V}{V_O}\right)}$$

2. INDUCTOR RIPPLE CURRENT

Set the inductor ripple current (Δi_{L-PP}) by solving for the appropriate inductor (L1):

$$L1 = \frac{V_O \times t_{OFF}}{\Delta i_{L-PP}}$$

3. AVERAGE LED CURRENT

Set the average LED current (I_{LED}) by first solving for the peak inductor current (I_{L-MAX}):

$$I_{L-MAX} = I_{LED} + \frac{\Delta i_{L-PP}}{2}$$

Peak inductor current is detected across the sense resistor (R_{SNS}). In most cases, assume the maximum value (V_{ADJ} = 1.24V) at the IADJ pin and solve for R_{SNS}:

$$R_{SNS} = \frac{V_{ADJ}}{5 \times I_{L-MAX}}$$

If the calculated R_{SNS} is far from a standard value, the beginning of the process can be iterated to choose a new R_{OFF}, L1, and R_{SNS} value that is a closer fit. The easiest way to approach the iterative process is to change the nominal f_{SW} target knowing that the switching frequency varies with operating conditions anyways.

Another method for finding a standard R_{SNS} value is to change the V_{ADJ} value. However, this would require an external voltage source or a resistor from the IADJ pin to GND as explained in the *Theory of Operation* section of this datasheet.

4. OUTPUT CAPACITANCE

A minimum output capacitance (C_{O-MIN}) may be necessary to reduce Δi_{LED-PP} below Δi_{L-PP}. With the specified Δi_{LED-PP} and the known dynamic resistance (r_D) of the LED string, solve for the required impedance (Z_C) for C_{O-MIN}:

$$Z_C = \frac{r_D \times \Delta i_{LED-PP}}{\Delta i_{L-PP} - \Delta i_{LED-PP}}$$

Solve for C_{O-MIN}:

$$C_{O-MIN} = \frac{1}{2 \times \pi \times f_{SW} \times Z_C}$$

5. INPUT CAPACITANCE

Set the input voltage ripple (Δv_{IN-PP}) by solving for the required minimum capacitance (C_{IN-MIN}):

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta v_{IN-PP}} = \frac{I_{LED} \times \left(\frac{1}{f_{SW}} - t_{OFF}\right)}{\Delta v_{IN-PP}}$$

The necessary RMS input current rating (I_{IN-RMS}) is:

$$I_{IN-RMS} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

6. PFET

The PFET voltage rating should be at least 15% higher than the maximum input voltage (V_{IN-MAX}) and current rating should be at least 10% higher than the average PFET current (I_T):

$$I_T = D \times I_{LED}$$

Given a PFET with on-resistance (R_{DS-ON}), solve for the RMS transistor current (I_{T-RMS}) and power dissipation (P_T):

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left(1 + \frac{1}{12} \times \left(\frac{\Delta i_{L-PP}}{I_{LED}}\right)^2\right)}$$

$$P_T = I_{T-RMS}^2 \times R_{DSON}$$

7. DIODE

The Schottky diode needs a voltage rating similar to the PFET. Higher current diodes with a lower forward voltage are suggested. Given a diode with forward voltage (V_D), solve for the average diode current (I_D) and power dissipation (P_D):

$$I_D = (1 - D) \times I_{LED}$$

$$P_D = I_D \times V_D$$

8. INPUT UVLO

Input UVLO is set with the turn-on threshold voltage ($V_{TURN-ON}$) and the desired hysteresis (V_{HYS}). To set V_{HYS}, solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{22\,\mu A}$$

To set $V_{TURN-ON}$, solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V}$$

9. IADJ CONNECTION METHOD

The IADJ pin controls the high-side current sense threshold in three ways outlined in the *Theory of Operation* section.

Method #1: Leave IADJ pin open and I_{LED} is calculated as in the *Average LED Current* section of the *Design Guide*.

Method #2: Apply an external voltage (V_{ADJ}) to the IADJ pin between 0 and 1.24V to analog dim or to reduce I_{LED} as follows:

$$I_{LED} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{\Delta i_{L-PP}}{2}$$

Keep in mind that analog dimming will eventually push the converter in to DCM and the inductor current ripple will no longer be constant causing a divergence from linear dimming at low levels.

A 0.1µF capacitor connected from the IADJ pin to GND is recommended when using this method. It may also be necessary to have a 1kΩ series resistor with the capacitor to create an RC filter. The filter will help remove high frequency noise created by other connected circuitry.

Method #3: Connect an external resistor or potentiometer to GND (R_{EXT}) and the internal 5µA current source will set the voltage. Again, a 0.1µF capacitor connected from the IADJ pin to GND is recommended. To set I_{LED}, solve for R_{EXT}:

$$R_{EXT} = \frac{\left(I_{LED} + \frac{\Delta i_{L-PP}}{2}\right) \times R_{SNS}}{1\,\mu A}$$

10. PWM DIMMING METHOD

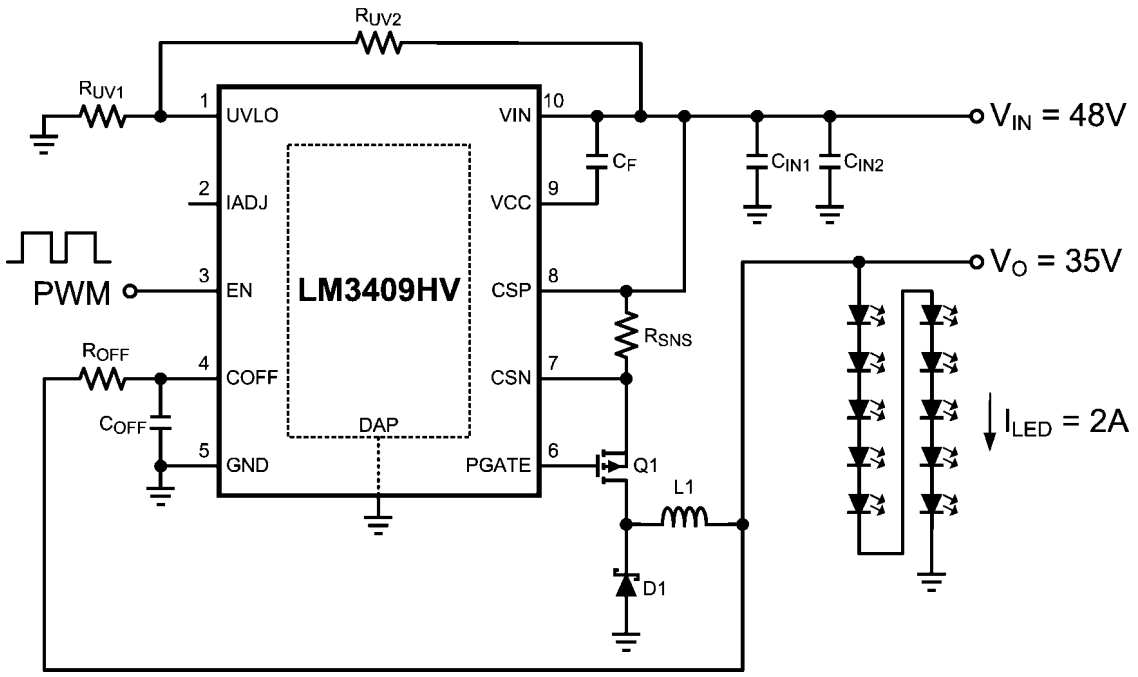
There are two methods to PWM dim using the LM3409/09HV:

Method #1: Apply an external PWM signal to the EN terminal.

Method #2: Perform external parallel FET shunt dimming as detailed in the *External Parallel FET PWM Dimming* section.

Design Example #1

EN PIN PWM DIMMING APPLICATION FOR 10 LEDS



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SPECIFICATIONS

f_{SW} = 525kHz
V_{IN} = 48V; V_{IN-MAX} = 75V
V_O = 35V
I_{LED} = 2A
$\Delta i_{LED-PP} = \Delta i_{L-PP}$ = 1A
Δv_{IN-PP} = 1.44V
$V_{TURN-ON}$ = 10V; V_{HYS} = 1.1V
η = 0.95

1. NOMINAL SWITCHING FREQUENCY

Assume C_{OFF} = 470pF and η = 0.95. Solve for R_{OFF}:

$$R_{OFF} = \frac{-\left(1-\frac{V_O}{\eta \times V_{IN}}\right)}{(C_{OFF} + 20\ pF) \times f_{SW} \times \ln\left(1-\frac{1.24V}{V_O}\right)}$$

$$R_{OFF} = \frac{-\left(1-\frac{35V}{0.95 \times 48V}\right)}{490\ pF \times 525\ kHz \times \ln\left(1-\frac{1.24V}{35V}\right)} = 25.1\ k\Omega$$

The closest 1% tolerance resistor is 24.9 kΩ therefore the actual t_{OFF} and target f_{SW} are:

$$t_{OFF} = -(C_{OFF} + 20\ pF) \times R_{OFF} \times \ln\left(1-\frac{1.24V}{V_O}\right)$$

$$t_{OFF} = -490\ pF \times 24.9\ k\Omega \times \ln\left(1-\frac{1.24V}{35V}\right) = 440\ ns$$

$$f_{SW} = \frac{1-\left(\frac{V_O}{\eta \times V_{IN}}\right)}{t_{OFF}} = \frac{1-\left(\frac{35V}{0.95 \times 48V}\right)}{440\ ns} = 528\ kHz$$

The chosen components from step 1 are:

$$C_{OFF} = 470\ pF$$
$$R_{OFF} = 24.9\ k\Omega$$

2. INDUCTOR RIPPLE CURRENT

Solve for L1:

$$L1 = \frac{V_O \times t_{OFF}}{\Delta i_{L-PP}} = \frac{35V \times 440\ ns}{1A} = 15.4\ \mu H$$

The closest standard inductor value is 15 µH therefore the actual Δi_{L-PP} is:

$$\Delta i_{L-PP} = \frac{V_O \times t_{OFF}}{L1} = \frac{35V \times 440\ ns}{15\ \mu H} = 1.027A$$

The chosen component from step 2 is:

$$L1 = 15\ \mu H$$

3. AVERAGE LED CURRENT

Determine I_{L-MAX}:

$$I_{L-MAX} = I_{LED} + \frac{\Delta i_{L-PP}}{2} = 2A + \frac{1.027A}{2} = 2.51A$$

Assume V_{ADJ} = 1.24V and solve for R_{SNS}:

$$R_{SNS} = \frac{V_{ADJ}}{5 \times I_{L-MAX}} = \frac{1.24V}{5 \times 2.51A} = 0.099\Omega$$

The closest 1% tolerance resistor is 0.1 Ω therefore the I_{LED} is:

$$I_{LED} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{\Delta i_{L-PP}}{2}$$

$$I_{LED} = \frac{1.24V}{5 \times 0.099\Omega} - \frac{1.027A}{2} = 1.97A$$

The chosen component from step 3 is:

$$\boxed{R_{SNS} = 0.1\Omega}$$

4. OUTPUT CAPACITANCE

No output capacitance is necessary.

5. INPUT CAPACITANCE

Determine t_{ON}:

$$t_{ON} = \frac{1}{f_{SW}} - t_{OFF} = \frac{1}{528\,kHz} - 440\,ns = 1.45\,\mu s$$

Solve for C_{IN-MIN}:

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta v_{IN-PP}} = \frac{1.97A \times 1.45\,\mu s}{1.44V} = 1.98\,\mu F$$

Choose C_{IN}:

$$C_{IN} = C_{IN-MIN} \times 2 = 3.96\,\mu F$$

Determine I_{IN-RMS}:

$$I_{IN-RMS} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

$$I_{IN-RMS} = 1.97A \times 528\,kHz \times \sqrt{1.45\,\mu s \times 440\,ns} = 831\,mA$$

The chosen components from step 5 are:

$$\boxed{C_{IN1} = C_{IN2} = 2.2\,\mu F}$$

6. PFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_{IN-MAX} = 75V$$

$$I_T = D \times I_{LED} = \frac{V_O \times I_{LED}}{V_{IN} \times \eta} = \frac{35V \times 1.97A}{48V \times 0.95} = 1.51A$$

A 100V, 3.8A PFET is chosen with R_{DS-ON} = 190mΩ and Q_g = 20nC. Determine I_{T-RMS} and P_T:

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left(1 + \frac{1}{12} \times \left(\frac{\Delta i_{L-PP}}{I_{LED}}\right)^2\right)}$$

$$I_{T-RMS} = 1.97A \times \sqrt{\frac{35V}{48V \times 0.95} \times \left(1 + \frac{1}{12} \times \left(\frac{1.027A}{1.97A}\right)^2\right)}$$

$$I_{T-RMS} = 1.74A$$

$$P_T = I_{T-RMS}^2 \times R_{DSON} = 1.74A^2 \times 190\,m\Omega = 577\,mW$$

The chosen component from step 6 is:

$$\boxed{Q1 \rightarrow 3.8A, 100V, DPAK}$$

7. DIODE

Determine minimum D1 voltage rating and current rating:

$$V_{D-MAX} = V_{IN-MAX} = 75V$$

$$I_D = (1-D) \times I_{LED} = \left(1 - \frac{V_O}{V_{IN} \times \eta}\right) \times I_{LED}$$

$$I_D = \left(1 - \frac{35V}{48V \times 0.95}\right) \times 1.97A = 457\,mA$$

A 100V, 3A diode is chosen with V_D = 750mV. Determine P_D:

$$P_D = I_D \times V_D = 457\,mA \times 750\,mV = 343\,mW$$

The chosen component from step 7 is:

$$\boxed{D1 \rightarrow 3A, 100V, SMC}$$

8. INPUT UVLO

Solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{22\,\mu A} = \frac{1.1V}{22\,\mu A} = 50\,k\Omega$$

The closest 1% tolerance resistor is 49.9 kΩ therefore V_{HYS} is:

$$V_{HYS} = R_{UV2} \times 22\,\mu A = 49.9\,k\Omega \times 22\,\mu A = 1.1V$$

Solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN\text{-}ON} - 1.24V} = \frac{1.24V \times 49.9\,k\Omega}{10V - 1.24V} = 7.06\,k\Omega$$

The closest 1% tolerance resistor is 6.98 kΩ therefore $V_{TURN\text{-}ON}$ is:

$$V_{TURN\text{-}ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN\text{-}ON} = \frac{1.24V \times (6.98\,k\Omega + 49.9\,k\Omega)}{6.98\,k\Omega} = 10.1V$$

The chosen components from step 8 are:

$$R_{UV1} = 6.98\,k\Omega$$
$$R_{UV2} = 49.9\,k\Omega$$

9. IADJ CONNECTION METHOD

The IADJ pin is left open forcing V_{ADJ} = 1.24V.

10. PWM DIMMING METHOD

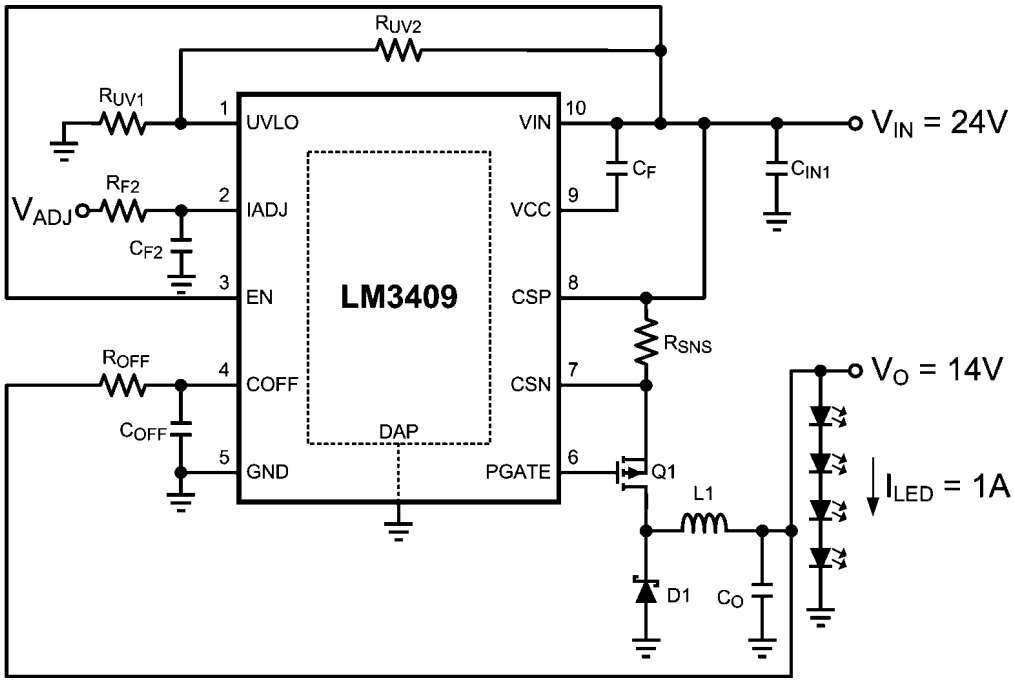
PWM dimming signal pair is applied to the EN pin and GND at f_{DIM} = 1 kHz.

Design #1 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3409HV/ LM3409QHV	Buck controller	NSC	LM3409HVMY/ LM3409QHVMY
2	C_{IN1}, C_{IN2}	2.2µF X7R 10% 100V	MURATA	GRM43ER72A225KA01 L
1	C_F	1.0µF X7R 10% 16V	TDK	C1608X7R1C105K
1	C_{OFF}	470pF X7R 10% 50V	TDK	C1608X7R1H471K
1	Q1	PMOS 100V 3.8A	ZETEX	ZXMP10A18KTC
1	D1	Schottky 100V 3A	VISHAY	SS3H10-E3/57T
1	L1	15 µH 20% 4.2A	TDK	SLF12565T-150M4R2
1	R_{OFF}	24.9kΩ 1%	VISHAY	CRCW060324K9FKEA
1	R_{UV1}	6.98kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R_{UV2}	49.9kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA

Design Example #2

ANALOG DIMMING APPLICATION FOR 4 LEDS



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SPECIFICATIONS

f_{SW} = 500kHz
V_{IN} = 24V; V_{IN-MAX} = 42V
V_O = 14V
I_{LED} = 1A
Δi_{L-PP} = 450mA; Δi_{LED-PP} = 50mA
Δv_{IN-PP} = 1V
$V_{TURN-ON}$ = 10V; V_{HYS} = 1.1V
η = 0.90

1. NOMINAL SWITCHING FREQUENCY

Assume C_{OFF} = 470pF and η = 0.90. Solve for R_{OFF}:

$$R_{OFF} = \frac{-\left(1-\frac{V_O}{\eta \times V_{IN}}\right)}{C_{OFF} + 20\ pF \times f_{SW} \times \ln\left(1-\frac{1.24V}{V_O}\right)}$$

$$R_{OFF} = \frac{-\left(1-\frac{14V}{0.90 \times 24V}\right)}{490\ pF \times 500\ kHz \times \ln\left(1-\frac{1.24V}{14V}\right)} = 15.5\ k\Omega$$

The closest 1% tolerance resistor is 15.4 kΩ therefore the actual t_{OFF} and target f_{SW} are:

$$t_{OFF} = -(C_{OFF} + 20\ pF) \times R_{OFF} \times \ln\left(1-\frac{1.24V}{V_O}\right)$$

$$t_{OFF} = -490\ pF \times 15.4\ k\Omega \times \ln\left(1-\frac{1.24V}{14V}\right) = 700\ ns$$

$$f_{SW} = \frac{1-\left(\frac{V_O}{\eta \times V_{IN}}\right)}{t_{OFF}} = \frac{1-\left(\frac{14V}{0.90 \times 24V}\right)}{700\ ns} = 503\ kHz$$

The chosen components from step 1 are:

$$\boxed{\begin{array}{l} C_{OFF} = 470\ pF \\ R_{OFF} = 15.4\ k\Omega \end{array}}$$

2. INDUCTOR RIPPLE CURRENT

Solve for L1:

$$L1 = \frac{V_O \times t_{OFF}}{\Delta i_{L-PP}} = \frac{14V \times 700\ ns}{450\ mA} = 21.8\ \mu H$$

The closest standard inductor value is 22 µH therefore the actual Δi_{L-PP} is:

$$\Delta i_{L-PP} = \frac{V_O \times t_{OFF}}{L1} = \frac{14V \times 700\ ns}{22\ \mu H} = 445\ mA$$

The chosen component from step 2 is:

$$\boxed{L1 = 22\ \mu H}$$

3. AVERAGE LED CURRENT

Determine I_{L-MAX}:

$$I_{L-MAX} = I_{LED} + \frac{\Delta i_{L-PP}}{2} = 1A + \frac{445\,mA}{2} = 1.22A$$

Assume V_{ADJ} = 1.24V and solve for R_{SNS}:

$$R_{SNS} = \frac{V_{ADJ}}{5 \times I_{L-MAX}} = \frac{1.24V}{5 \times 1.22A} = 0.203\Omega$$

The closest 1% tolerance resistor is 0.2 Ω therefore I_{LED} is:

$$I_{LED} = \frac{V_{ADJ}}{5 \times R_{SNS}} - \frac{\Delta i_{L-PP}}{2} = \frac{1.24V}{5 \times 0.2\Omega} - \frac{445\,mA}{2} = 1.02A$$

The chosen component from step 3 is:

$$\boxed{R_{SNS} = 0.2\Omega}$$

4. OUTPUT CAPACITANCE

Assume r_D = 2 Ω and determine Z_C:

$$Z_C = \frac{r_D \times \Delta i_{LED-PP}}{\Delta i_{L-PP} - \Delta i_{LED-PP}} = \frac{2\Omega \times 50\,mA}{450\,mA - 50\,mA} = 250\,m\Omega$$

Solve for C_{O-MIN} and :

$$C_{O-MIN} = \frac{1}{2 \times \pi \times f_{SW} \times Z_C}$$

$$C_{O-MIN} = \frac{1}{2 \times \pi \times 503\,kHz \times 250\,m\Omega} = 1.27\,\mu F$$

Choose C_O:

$$C_O = C_{O-MIN} \times 1.75 = 2.2\,\mu F$$

The chosen component from step 5 is:

$$\boxed{C_O = 2.2\,\mu F}$$

5. INPUT CAPACITANCE

Determine t_{ON}:

$$t_{ON} = \frac{1}{f_{SW}} - t_{OFF} = \frac{1}{503\,kHz} - 700\,ns = 1.29\,\mu s$$

Solve for C_{IN-MIN}:

$$C_{IN-MIN} = \frac{I_{LED} \times t_{ON}}{\Delta v_{IN-PP}} = \frac{1.02A \times 1.29\,\mu s}{720\,mV} = 1.82\,\mu F$$

Choose C_{IN}:

$$C_{IN} = C_{IN-MIN} \times 2 = 3.64\,\mu F$$

Determine I_{IN-RMS}:

$$I_{IN-RMS} = I_{LED} \times f_{SW} \times \sqrt{t_{ON} \times t_{OFF}}$$

$$I_{IN-RMS} = 1.02A \times 503\,kHz \times \sqrt{1.29\,\mu s \times 700\,ns} = 486\,mA$$

The chosen component from step 5 is:

$$\boxed{C_{IN} = 4.7\,\mu F}$$

6. PFET

Determine minimum Q1 voltage rating and current rating:

$$V_{T-MAX} = V_{IN-MAX} = 42V$$

$$I_T = D \times I_{LED} = \frac{V_O \times I_{LED}}{V_{IN} \times \eta} = \frac{14V \times 1.02A}{24V \times 0.90} = 660\,mA$$

A 70V, 5.7A PFET is chosen with R_{DS-ON} = 190mΩ and Q_g = 20nC. Determine I_{T-RMS} and P_T:

$$I_{T-RMS} = I_{LED} \times \sqrt{D \times \left(1 + \frac{1}{12} \times \left(\frac{\Delta i_{L-PP}}{I_{LED}}\right)^2\right)}$$

$$I_{T-RMS} = 1.02A \times \sqrt{\frac{14V}{24V \times 0.90} \times \left(1 + \frac{1}{12} \times \left(\frac{445\,mA}{1.02A}\right)^2\right)}$$

$$I_{T-RMS} = 830\,mA$$

$$P_T = I_{T-RMS}^2 \times R_{DSON} = 830\,mA^2 \times 190\,m\Omega = 129\,mW$$

The chosen component from step 6 is:

$$\boxed{Q1 \rightarrow 5.7A, 70V, DPAK}$$

7. DIODE

Determine minimum D1 voltage rating and current rating:

$$V_{D-MAX} = V_{IN-MAX} = 42V$$

$$I_D = (1 - D) \times I_{LED} = \left(1 - \frac{V_O}{V_{IN} \times \eta}\right) \times I_{LED}$$

$$I_D = \left(1 - \frac{14V}{24V \times 0.90}\right) \times 1.02A = 358\,mA$$

A 60V, 5A diode is chosen with V_D = 750mV. Determine P_D:

$$P_D = I_D \times V_D = 358\,mA \times 750\,mV = 268\,mW$$

The chosen component from step 7 is:

$$\boxed{D1 \rightarrow 5A, 60V, SMC}$$

8. INPUT UVLO

Solve for R_{UV2}:

$$R_{UV2} = \frac{V_{HYS}}{22\,\mu A} = \frac{1.1V}{22\,\mu A} = 50\,k\Omega$$

The closest 1% tolerance resistor is 49.9 kΩ therefore V_{HYS} is:

$$V_{HYS} = R_{UV2} \times 22\,\mu A = 49.9\,k\Omega \times 22\,\mu A = 1.1V$$

Solve for R_{UV1}:

$$R_{UV1} = \frac{1.24V \times R_{UV2}}{V_{TURN-ON} - 1.24V} = \frac{1.24V \times 49.9\,k\Omega}{10V - 1.24V} = 7.06\,k\Omega$$

The closest 1% tolerance resistor is 6.98 kΩ therefore $V_{TURN-ON}$ is:

$$V_{TURN-ON} = \frac{1.24V \times (R_{UV1} + R_{UV2})}{R_{UV1}}$$

$$V_{TURN-ON} = \frac{1.24V \times (6.98\,k\Omega + 49.9\,k\Omega)}{6.98\,k\Omega} = 10.1V$$

The chosen components from step 8 are:

$$R_{UV1} = 6.98\,k\Omega$$
$$R_{UV2} = 49.9\,k\Omega$$

9. IADJ CONNECTION METHOD

The IADJ pin is connected to an external voltage source and varied from 0 – 1.24V to dim. An RC filter (R_{F2} = 1 kΩ and C_{F2} = 0.1µF) is used as recommended.

10. PWM DIMMING METHOD

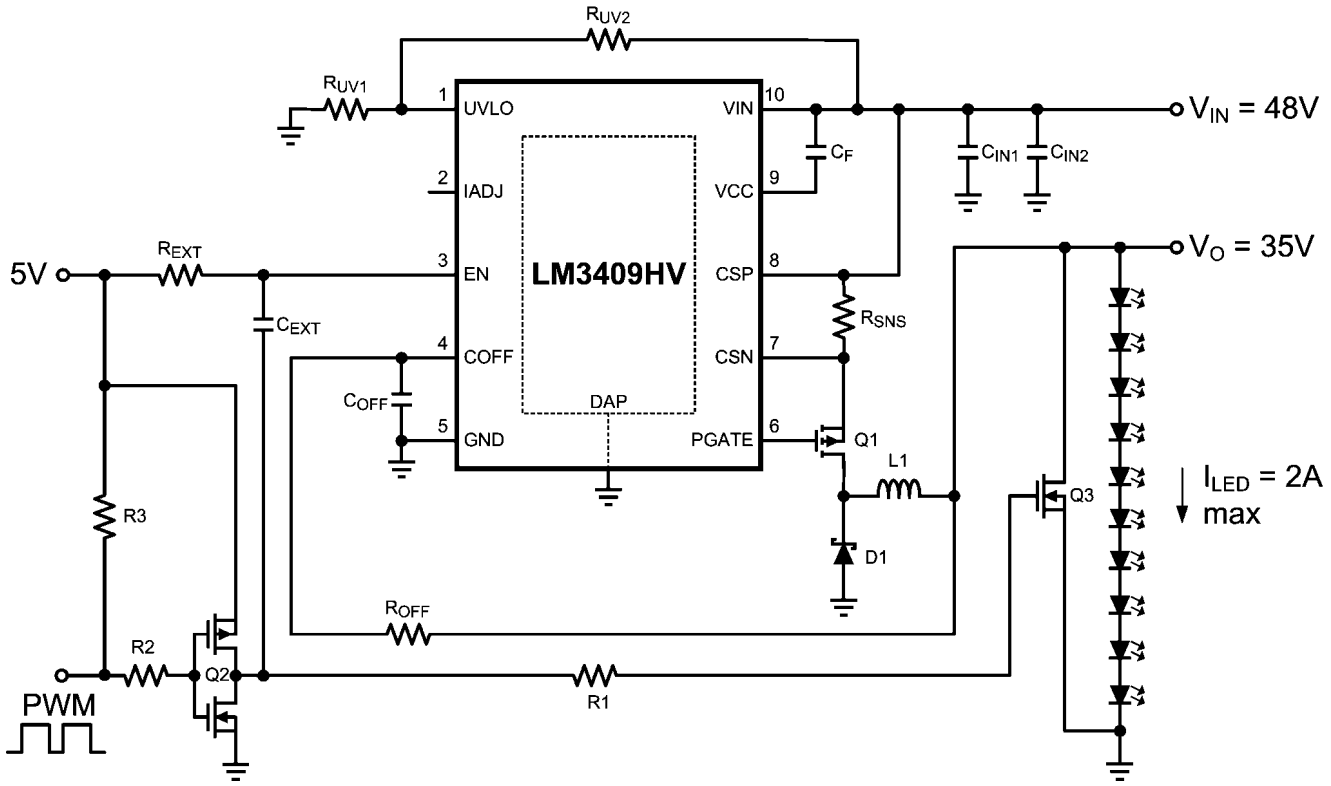
No PWM dimming is necessary.

Design #2 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3409/LM3409Q	Buck controller	NSC	LM3409MY/LM3409QMY
2	C_{IN1}	4.7µF X7R 10% 50V	MURATA	GRM55ER71H475MA01L
1	C_F	1.0µF X7R 10% 16V	TDK	C1608X7R1C105K
1	C_{F2}	0.1µF X7R 10% 16V	TDK	C1608X7R1C104K
1	C_{OFF}	470pF X7R 10% 50V	TDK	C1608X7R1H471K
1	C_O	2.2µF X7R 10% 50V	MURATA	GRM43ER71H225MA01L
1	Q1	PMOS 70V 5.7A	ZETEX	ZXMP7A17KTC
1	D1	Schottky 60V 5A	COMCHIP	CDBC560-G
1	L1	22 µH 20% 4.2A	TDK	SLF12575T-220M4R0
1	R_{F2}	1.0kΩ 1%	VISHAY	CRCW06031K00FKEA
1	R_{OFF}	15.4kΩ 1%	VISHAY	CRCW060315K4FKEA
1	R_{UV1}	6.98kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R_{UV2}	49.9kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R_{SNS}	0.2Ω 1% 1W	VISHAY	WSL2512R2000FEA

Applications Information

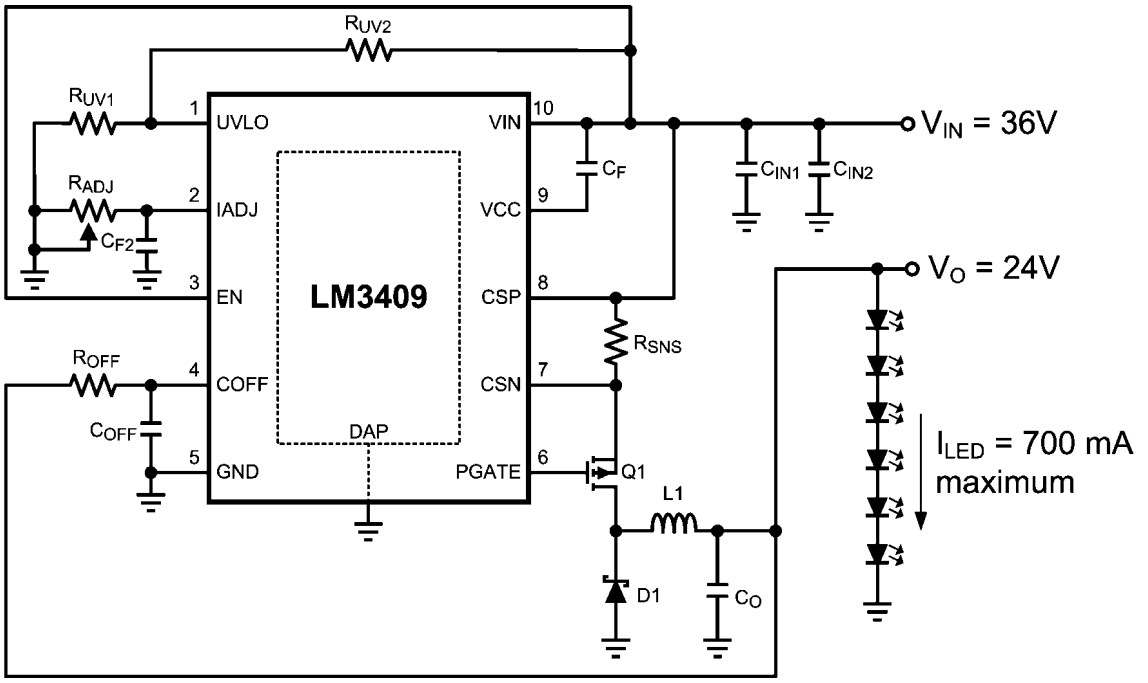
DESIGN #3: EXTERNAL PARALLEL FET PWM DIMMING APPLICATION FOR 10 LEDS



Design #3 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3409HV/ LM3409QHV	Buck controller	NSC	LM3409HVMY/ LM3409QHVMY
2	C_{IN1}, C_{IN2}	2.2µF X7R 10% 100V	MURATA	GRM43ER72A225KA01L
1	C_F	1.0µF X7R 10% 16V	TDK	C1608X7R1C105K
1	C_{OFF}	470pF X7R 10% 50V	TDK	C1608X7R1H471K
1	C1	2200pF X7R 10% 50V	MURATA	GRM188R71H222KA01D
1	Q1	PMOS 100V 3.8A	ZETEX	ZXMP10A18KTC
1	Q2	CMOS 30V 2A	FAIRCHILD	FDC6333C
1	Q3	NMOS 100V 7.5A	FAIRCHILD	FDS3672
1	D1	Schottky 100V 3A	VISHAY	SS3H10-E3/57T
1	L1	15 µH 20% 4.2A	TDK	SLF12565T-150M4R2
2	R1, R2	1Ω 1%	VISHAY	CRCW06031R00FNEA
1	R3	10kΩ 1%	VISHAY	CRCW060310K0FKEA
1	R_{EXT}	100Ω 1%	VISHAY	CRCW0603100RFKEA
1	R_{OFF}	24.9kΩ 1%	VISHAY	CRCW060324K9FKEA
1	R_{UV1}	6.98kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R_{UV2}	49.9kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R_{SNS}	0.1Ω 1% 1W	VISHAY	WSL2512R1000FEA

DESIGN #4: SINGLE POTENTIOMETER ANALOG DIMMING APPLICATION FOR 6 LEDS



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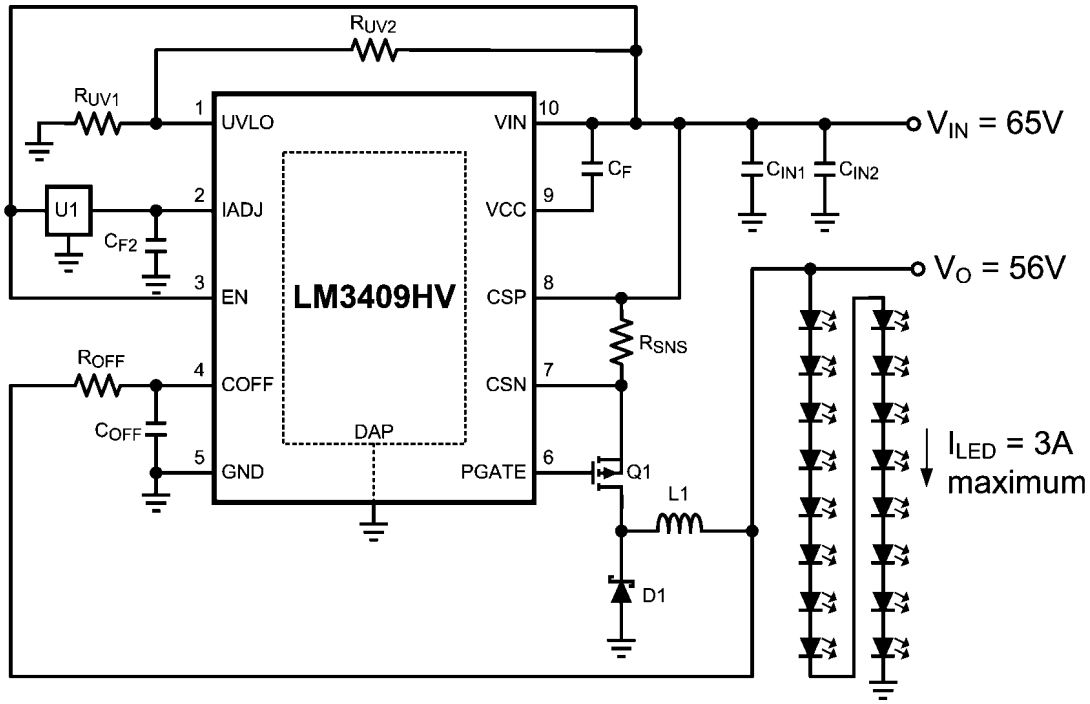
Design #4 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3409/LM3409Q	Buck controller	NSC	LM3409MY/LM3409QMY
2	C_{IN1}, C_{IN2}	2.2µF X7R 10% 50V	MURATA	GRM43ER71H225MA01L
1	C_F	1.0µF X7R 10% 16V	TDK	C1608X7R1C105K
1	C_{F2}	0.1µF X7R 10% 16V	TDK	C1608X7R1C104K
1	C_{OFF}	470pF X7R 10% 50V	TDK	C1608X7R1H471K
1	C_O	1.0µF X7R 10% 50V	MURATA	GRM32RR71H105KA01L
1	Q1	PMOS 60V 3A	ZETEX	ZXMP6A17GTA
1	D1	Schottky 60V 2A	ST-MICRO	STPS2L60A
1	L1	68 µH 20% 2A	TDK	SLF12565T-680M2R0
1	R_{OFF}	25.5kΩ 1%	VISHAY	CRCW060325K5FKEA
1	R_{UV1}	6.98kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R_{UV2}	49.9kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R_{SNS}	0.3Ω 1% 1W	VISHAY	WSL2512R3000FEA
1	R_{ADJ}	250kΩ potentiometer	BOURNS	3352P-1-254

DESIGN #5: 75°C THERMAL FOLDBACK APPLICATION FOR 16 LEDS

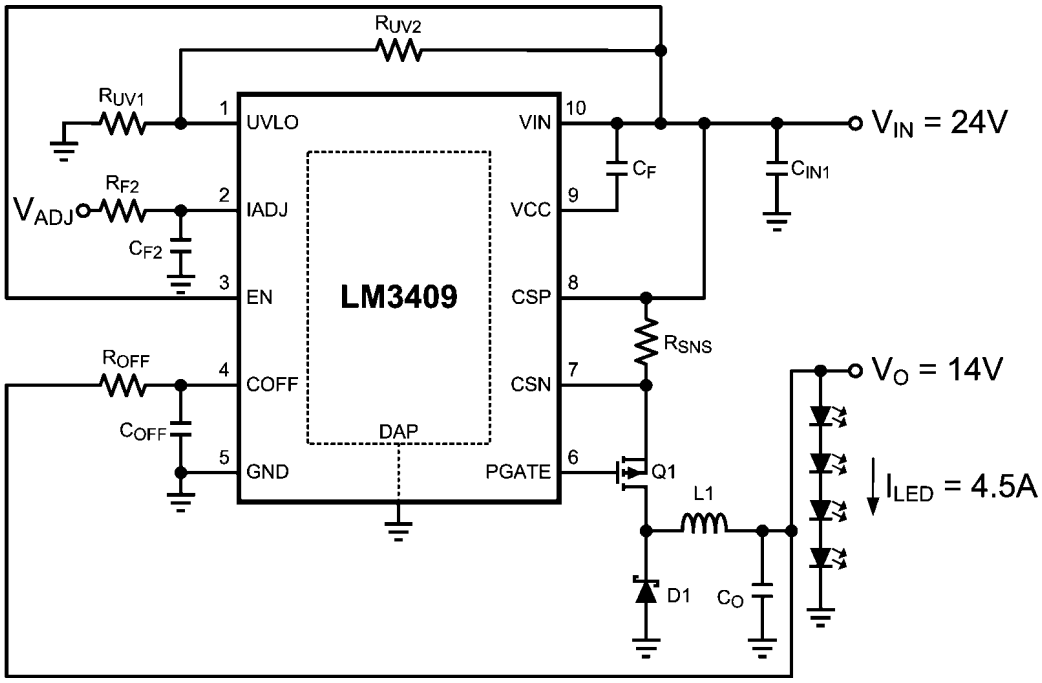


Design #5 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3409HV/ LM3409QHV	Buck controller	NSC	LM3409HVMY/LM3409QHVMY
1	U1	Analog Temperature Sensor	NSC	LM94022
2	C_{IN1}, C_{IN2}	2.2µF X7R 10% 100V	MURATA	GRM43ER72A225KA01L
1	C_F	1.0µF X7R 10% 16V	TDK	C1608X7R1C105K
1	C_{F2}	0.1µF X7R 10% 16V	TDK	C1608X7R1C104K
1	C_{OFF}	470pF X7R 10% 50V	TDK	C1608X7R1H471K
1	Q1	PMOS 100V 3.8A	ZETEX	ZXMP10A18KTC
1	D1	Schottky 100V 3A	COMCHIP	SS3H10-E3/57T
1	L1	15 µH 20% 4.7A	TDK	SLF12575T-150M4R7
1	R_{OFF}	24.9kΩ 1%	VISHAY	CRCW060324K9FKEA
1	R_{UV1}	6.98kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R_{UV2}	49.9kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R_{SNS}	0.07Ω 1% 1W	VISHAY	WSL2512R0700FEA

*U2 could be replaced with a 500kΩ NTC thermistor connected from IADJ to GND.

DESIGN #6: HIGH CURRENT APPLICATION FOR 4 LEDS

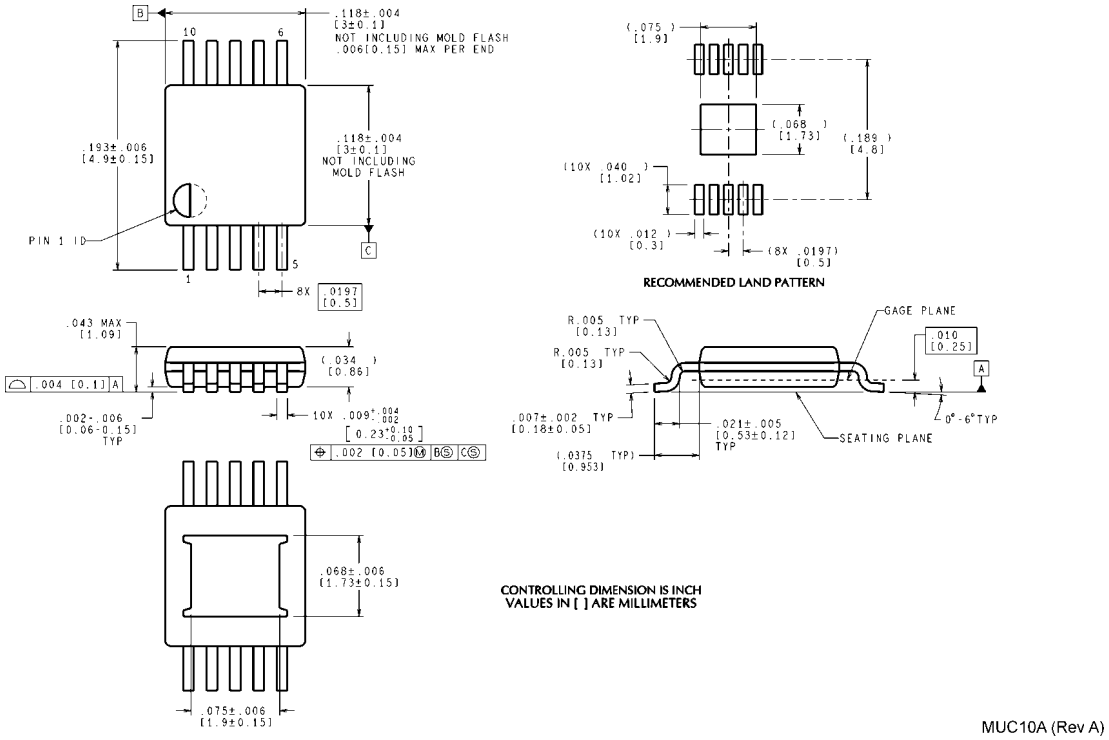


Design #6 Bill of Materials

Qty	Part ID	Part Value	Manufacturer	Part Number
1	LM3409/LM3409Q	Buck controller	NSC	LM3409MY/LM3409QMY
2	C_{IN1}	10µF X7R 10% 50V	TDK	C5750X7R1H106K
1	C_F	1.0µF X7R 10% 16V	TDK	C1608X7R1C105K
1	C_{F2}	0.1µF X7R 10% 16V	TDK	C1608X7R1C104K
1	C_{OFF}	470pF X7R 10% 50V	TDK	C1608X7R1H471K
1	C_O	1.0µF X7R 10% 50V	MURATA	GRM32RR71H105KA01L
1	Q1	PMOS 30V 24A	ST-MICRO	STD30PF03LT4
1	D1	Schottky 30V 5A	VISHAY	SSC53L-E3/57T
1	L1	15 µH 20% 7.5A	COILCRAFT	DO5022P-153ML
1	R_{F2}	1.0kΩ 1%	VISHAY	CRCW06031K00FKEA
1	R_{OFF}	23.2kΩ 1%	VISHAY	CRCW060323K2FKEA
1	R_{UV1}	6.98kΩ 1%	VISHAY	CRCW06036K98FKEA
1	R_{UV2}	49.9kΩ 1%	VISHAY	CRCW060349K9FKEA
1	R_{SNS}	0.05Ω 1% 1W	VISHAY	WSL2512R0500FEA

*U2 could be replaced with a 500kΩ NTC thermistor connected from IADJ to GND.

Physical Dimensions inches (millimeters) unless otherwise noted



MUC10A (Rev A)

10-Lead Exposed Pad Plastic eMSOP Package
NS Package Number MUC10A

Notes

Notes

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