



# STP16DPPS05

## Low voltage 16-bit constant current LED sink driver with output error detection and auto power-saving

### Features

- Low voltage power supply down to 3 V
- 16 constant current output channels
- Adjustable output current through external resistor
- Short and open output error detection
- Serial data IN/parallel data OUT
- Auto power-saving
- 3.3 V MCU-driving capability
- Output current: 3 to 40 mA
- 30 MHz clock frequency
- Available in high thermal efficiency TSSOP exposed pad
- ESD protection: 2 kV HBM, 200 V MM

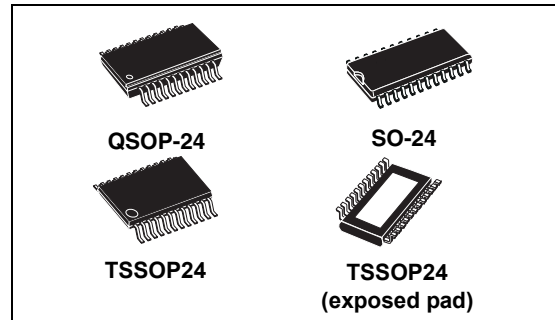
### Description

The STP16DPPS05 is a monolithic, low voltage, low current power 16-bit shift register designed for LED panel displays. The device features a 16-bit serial-in, parallel-out shift register that feeds a 16-bit D-type storage register. In the output stage, sixteen regulated current sources are designed to provide 3 to 40 mA of constant current to drive the LEDs. The STP16DPPS05 features open and short LED detection on the outputs. The detection circuit checks for 3 different conditions that can occur on the output line: short to GND, short to  $V_O$  or open line.

The data detection results are loaded in the shift registers and shifted out via the serial line output.

**Table 1. Device summary**

Order codes	Package	Packaging
STP16DPPS05MTR	SO-24 (tape and reel)	1000 parts per reel
STP16DPPS05TTR	TSSOP24 (tape and reel)	2500 parts per reel
STP16DPPS05XTTR	TSSOP24 exposed pad (tape and reel)	2500 parts per reel
STP16DPPS05PTR	QSOP-24	2500 parts per reel



The detection functionality is implemented without increasing the pin count, through a secondary function of the output enable and latch pin (DM1 and DM2 respectively). A dedicated logic sequence allows the device to enter or exit from detection mode. The STP16DPPS05 output current can be adjusted through an external resistor to control the light intensity of the LEDs. LED brightness is adjustable from 0% to 100% via the OE/DM2 pin.

The auto power-shutdown and auto power-ON feature allows the device to save power with no external intervention.

The STP16DPPS05 guarantees a 20 V output driving capability, allowing users to connect more LEDs in series. The high 30 MHz clock frequency makes the device suitable for high data rate transmission. The 3.3 V supply is well suited for applications which interface a 3.3 V MCU. Compared to a standard TSSOP package, the TSSOP with exposed pad increases heat dissipation capability by a factor of 2.5

# Contents

<b>1</b>	<b>Summary description</b> .....	<b>3</b>
1.1	Pin connection and description .....	3
<b>2</b>	<b>Electrical ratings</b> .....	<b>5</b>
2.1	Absolute maximum ratings .....	5
2.2	Thermal data .....	5
2.3	Recommended operating conditions .....	6
<b>3</b>	<b>Electrical characteristics</b> .....	<b>7</b>
<b>4</b>	<b>Equivalent circuit and outputs</b> .....	<b>9</b>
<b>5</b>	<b>Timing diagrams</b> .....	<b>11</b>
<b>6</b>	<b>Typical characteristics</b> .....	<b>14</b>
<b>7</b>	<b>Error detection mode functionality</b> .....	<b>18</b>
7.1	Phase one: entering error detection mode .....	18
7.2	Phase two: error detection .....	19
7.3	Phase three: resuming normal mode .....	21
7.4	Error detection conditions .....	21
7.5	Auto power-saving .....	23
<b>8</b>	<b>Package mechanical data</b> .....	<b>25</b>
<b>9</b>	<b>Revision history</b> .....	<b>33</b>

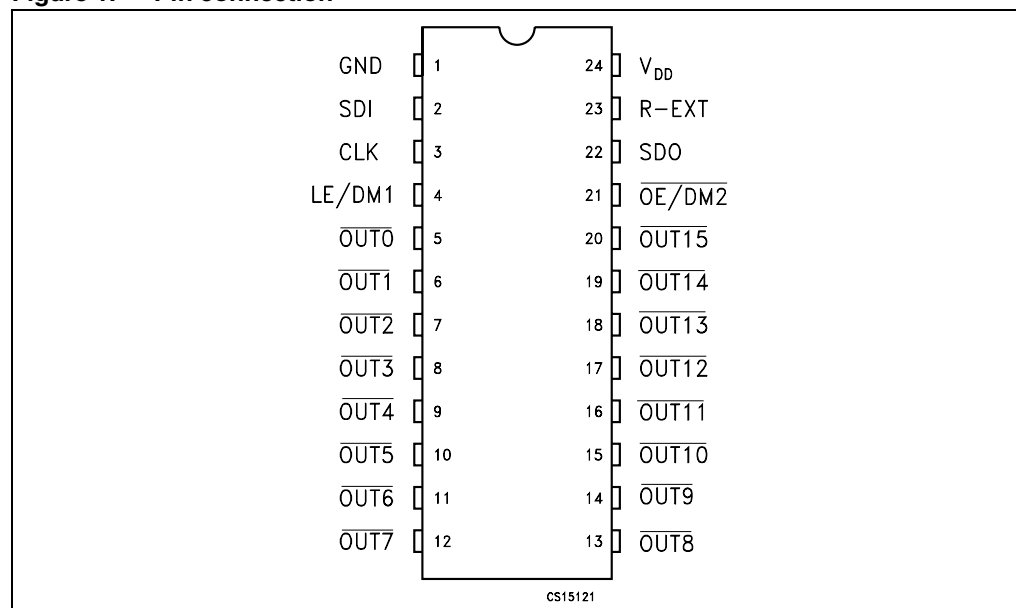
# 1 Summary description

Table 2. Typical current accuracy

Output voltage	Current accuracy		Output current	V <sub>DD</sub>	Temperature
	Between bits	Between ICs			
≥ 1.3 V	± 1%	± 2%	5 to 40 mA	3.3 V to 5 V	25 °C

## 1.1 Pin connection and description

Figure 1. Pin connection



Note: The exposed pad should be electrically connected to a metal land electrically isolated or connected to ground.

Table 3. Pin description

Pin n°	Symbol	Name and function
1	GND	Ground terminal
2	SDI	Serial data input terminal
3	CLK	Clock input terminal
4	LE/DM1	Latch input terminal - detect mode 1 (see operation principle)
5-20	$\overline{\text{OUT 0-15}}$	Output terminal
21	$\overline{\text{OE/DM2}}$	Input terminal of output enable (active low) - detect mode 1 (see operation principle)
22	SDO	Serial data out terminal
23	R-EXT	Input terminal for an external resistor for constant current programming
24	V <sub>DD</sub>	Supply voltage terminal

## 2 Electrical ratings

### 2.1 Absolute maximum ratings

Stressing the device above the ratings listed in the “absolute maximum ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other condition above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**Table 4. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply voltage	0 to 7	V
$V_O$	Output voltage	-0.5 to 20	V
$I_O$	Output current	50	mA
$V_I$	Input voltage	-0.4 to $V_{DD}$	V
$I_{GND}$	GND terminal current	800	mA
$f_{CLK}$	Clock frequency	50	MHz
$T_J$	Junction temperature range <sup>(1)</sup>	-40 to +170	°C

1. Such absolute value is based on the thermal shutdown protection.

### 2.2 Thermal data

**Table 5. Thermal data**

Symbol	Parameter	Value	Unit	
$T_A$	Operating free-air temperature range	-40 to +125	°C	
$T_{J-OPR}$	Operating thermal junction temperature range	-40 to +150	°C	
$T_{STG}$	Storage temperature range	-55 to +150	°C	
$R_{thJA}$	Thermal resistance junction-ambient <sup>(1)</sup>	SO-24	42.7	°C/W
		TSSOP24	55	°C/W
		TSSOP24 <sup>(2)</sup> Exposed Pad	37.5	°C/W
		QSOP-24	55	°C/W

1. According with JEDEC standard 51-7B

2. The exposed pad should be soldered directly to the PCB to obtain the thermal benefits.

## 2.3 Recommended operating conditions

**Table 6. Recommended operating conditions**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{DD}$	Supply voltage		3.0	-	5.5	V
$V_O$	Output voltage			-	20	V
$I_O$	Output current	OUTn	3	-	40	mA
$I_{OH}$	Output current	SERIAL-OUT		-	+1	mA
$I_{OL}$	Output current	SERIAL-OUT		-	-1	mA
$V_{IH}$	Input voltage		$0.7 V_{DD}$	-	$V_{DD}$	V
$V_{IL}$	Input voltage		-0.3	-	$0.3 V_{DD}$	V
$t_{wLAT}$	LE/DM1 pulse width	$V_{DD} = 3.0 \text{ V to } 5.0 \text{ V}$	20	-		ns
$t_{wCLK}$	CLK pulse width		10	-		ns
$t_{wEN}$	$\overline{OE}/DM2$ pulse width		100	-		ns
$t_{SETUP(D)}$	Setup time for DATA		8	-		ns
$t_{HOLD(D)}$	Hold time for DATA		5	-		ns
$t_{SETUP(L)}$	Setup time for LATCH		8	-		ns
$f_{CLK}$	Clock frequency		Cascade operation <sup>(1)</sup>		-	30

1. If the device is connected in cascade, it may not be possible to achieve the maximum data transfer. Please consider the timings carefully.

### 3 Electrical characteristics

$V_{DD} = 3.3 \text{ V to } 5 \text{ V}$ ,  $T_A = 25 \text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 7. Electrical characteristics**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{IH}$	Input voltage high level		$0.7 V_{DD}$		$V_{DD}$	V
$V_{IL}$	Input voltage low level		GND		$0.3 V_{DD}$	V
$I_{OH}$	Output leakage current	$V_{OH} = 20 \text{ V}$			1	$\mu\text{A}$
$V_{OL}$	Output voltage (serial-OUT)	$I_{OL} = 1 \text{ mA}$			0.4	V
$V_{OH}$	Output voltage (serial-OUT)	$I_{OH} = -1 \text{ mA}$	$V_{DD}-0.4\text{V}$			V
$I_{OL1}$	Output current	$V_O = 0.3 \text{ V}$ , $R_{ext} = 4 \text{ k}\Omega$	4.75	5	5.25	mA
$I_{OL2}$		$V_O = 0.3 \text{ V}$ , $R_{ext} = 1 \text{ k}\Omega$	19	20	21	
$I_{OL3}$		$V_O = 1.3 \text{ V}$ , $R_{ext} = 497 \text{ }\Omega$	38	40	42	
$\Delta I_{OL1}$	Output current error between bit (All output ON)	$V_O = 0.3 \text{ V}$ , $I_O = 5 \text{ mA}$ $R_{EXT} = 4 \text{ k}\Omega$		$\pm 1$	$\pm 5$	%
$\Delta I_{OL2}$		$V_O = 0.3 \text{ V}$ , $I_O = 20 \text{ mA}$ $R_{EXT} = 980 \text{ }\Omega$		$\pm 0.5$	$\pm 3$	
$\Delta I_{OL3}$		$V_O = 1.3 \text{ V}$ , $I_O = 40 \text{ mA}$ $R_{EXT} = 490 \text{ }\Omega$		$\pm 0.5$	$\pm 3$	
$R_{SIN(up)}$	Pull-up resistor		150	300	600	$\text{k}\Omega$
$R_{SIN(down)}$	Pull-down resistor		100	200	400	$\text{k}\Omega$
$I_{DD(OFF1)}$	Supply current (OFF)	$R_{EXT} = 1 \text{ k}\Omega$ , $I_{OUT} = 20 \text{ mA}$ , OUT 0 to 15 = OFF		5.4	7.5	mA
$I_{DD(OFF2)}$		$R_{EXT} = 497 \text{ }\Omega$ , $I_{OUT} = 40 \text{ mA}$ OUT 0 to 15 = OFF		8.0	9.5	
$I_{DD(ON1)}$	Supply current (ON)	$R_{EXT} = 1 \text{ k}\Omega$ , $I_{OUT} = 20 \text{ mA}$ , OUT 0 to 15 = ON		5.5	7.5	
$I_{DD(ON2)}$		$R_{EXT} = 497 \text{ }\Omega$ , $I_{OUT} = 40 \text{ mA}$ OUT 0 to 15 = ON		8.1	9.5	
Thermal	Thermal protection			170		$^\circ\text{C}$

$V_{DD} = 3.3 \text{ V to } 5 \text{ V}$ ,  $T_A = 25 \text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 8. Switching characteristics**

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit	
$t_{PLH1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE/DM1 = H, OE/DM2 = L	$V_{IH} = V_{DD}$ $V_{IL} = \text{GND}$ $I_O = 20 \text{ mA}$ $R_{EXT} = 1 \text{ K}\Omega$ $C_L = 10 \text{ pF}$ $V_L = 3.0 \text{ V}$ $R_L = 60 \Omega$	$V_{DD} = 3.3 \text{ V}$		53.5	86.5	ns
			$V_{DD} = 5 \text{ V}$		32	46.5	
$t_{PLH2}$	Propagation delay time, LE/DM1- $\overline{\text{OUTn}}$ , OE/DM2 = L		$V_{DD} = 3.3 \text{ V}$		48	75.5	ns
			$V_{DD} = 5 \text{ V}$		30	43	
$t_{PLH3}$	Propagation delay time, OE/DM2- $\overline{\text{OUTn}}$ , LE = H		$V_{DD} = 3.3 \text{ V}$		71.5	118	ns
			$V_{DD} = 5 \text{ V}$		43	62	
$t_{PLH}$	Propagation delay time, CLK-SDO		$V_{DD} = 3.3 \text{ V}$	15	21	31	ns
			$V_{DD} = 5 \text{ V}$	11	15	21	
$t_{PHL1}$	Propagation delay time, CLK- $\overline{\text{OUTn}}$ , LE/DM1 = H, OE/DM2 = L		$V_{DD} = 3.3 \text{ V}$		27.5	39	ns
			$V_{DD} = 5 \text{ V}$		22	30.5	
$t_{PHL2}$	Propagation delay time, LE/DM1- $\overline{\text{OUTn}}$ , OE/DM2 = L		$V_{DD} = 3.3 \text{ V}$		11.5	17.5	ns
			$V_{DD} = 5 \text{ V}$		8	11.5	
$t_{PHL3}$	Propagation delay time, OE/DM2- $\overline{\text{OUTn}}$ , LE/DM1 = H		$V_{DD} = 3.3 \text{ V}$		24	33.5	ns
			$V_{DD} = 5 \text{ V}$		21	28.5	
$t_{PHL}$	Propagation delay time, CLK-SDO	$V_{DD} = 3.3 \text{ V}$	17.5	24	36	ns	
		$V_{DD} = 5 \text{ V}$	12.5	17	25		
$t_{ON}$	Output rise time 10~90% of voltage waveform	$V_{DD} = 3.3 \text{ V}$		29	54	ns	
		$V_{DD} = 5 \text{ V}$		10	17		
$t_{OFF}$	Output fall time 90~10% of voltage waveform	$V_{DD} = 3.3 \text{ V}$		4.5	6	ns	
		$V_{DD} = 5 \text{ V}$		3.5	5		
$t_r$	CLK rise time <sup>(1)</sup>				5000	ns	
$t_f$	CLK fall time <sup>(1)</sup>				5000	ns	

1. In order to achieve high cascade data transfer, please consider tr/tf timings carefully.



## 4 Equivalent circuit and outputs

Figure 2.  $\overline{\text{OE}}/\text{DM2}$  terminal

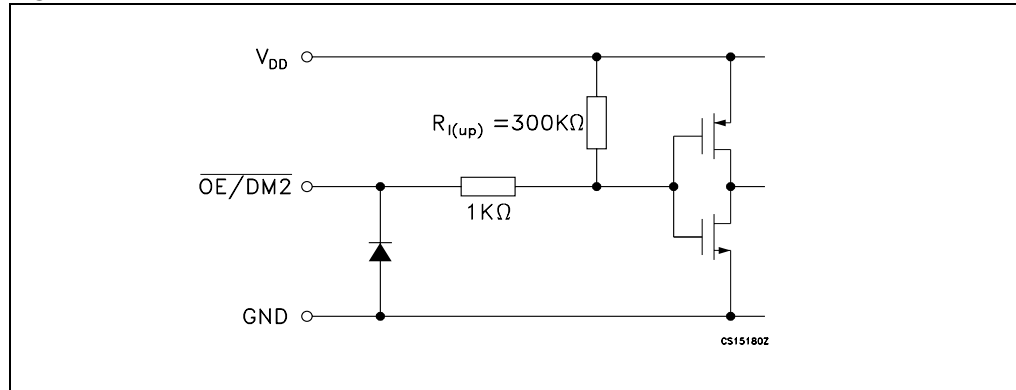


Figure 3.  $\text{LE}/\text{DM1}$  terminal

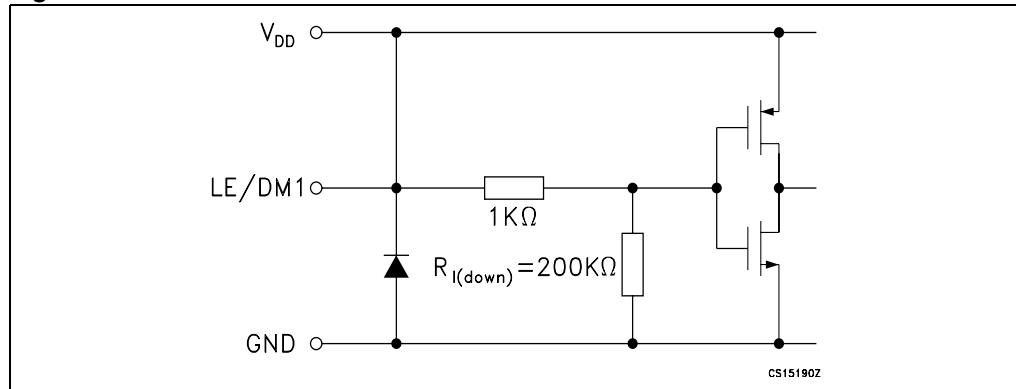


Figure 4.  $\text{CLK}, \text{SDI}$  terminal

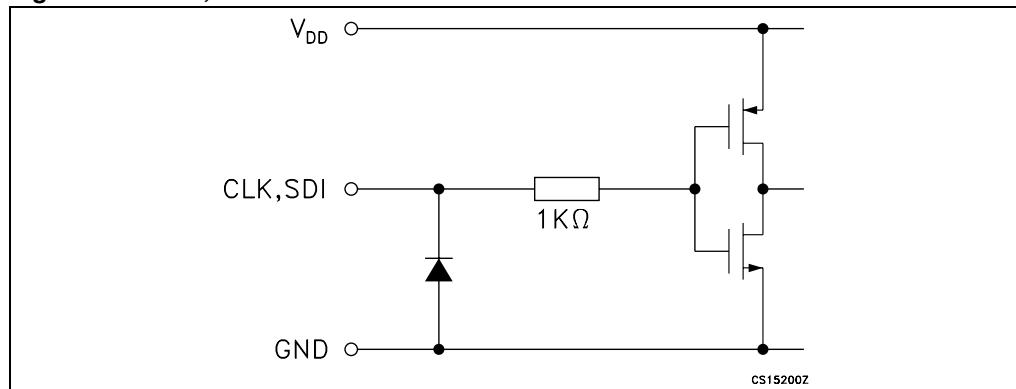


Figure 5. SDO terminal

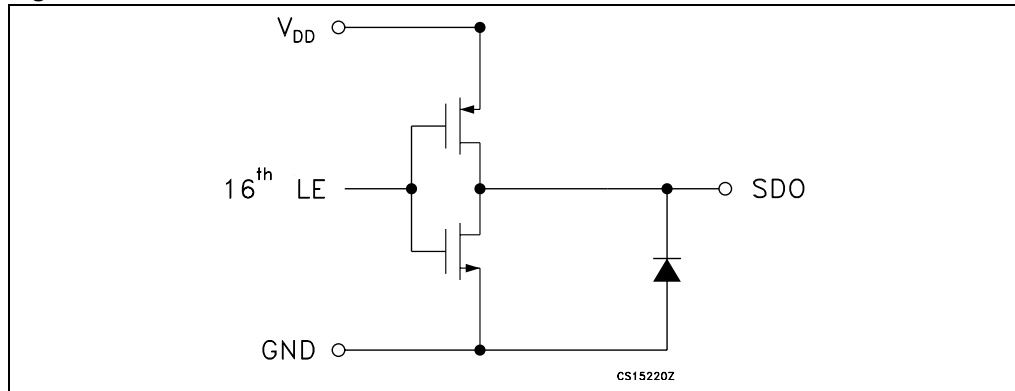
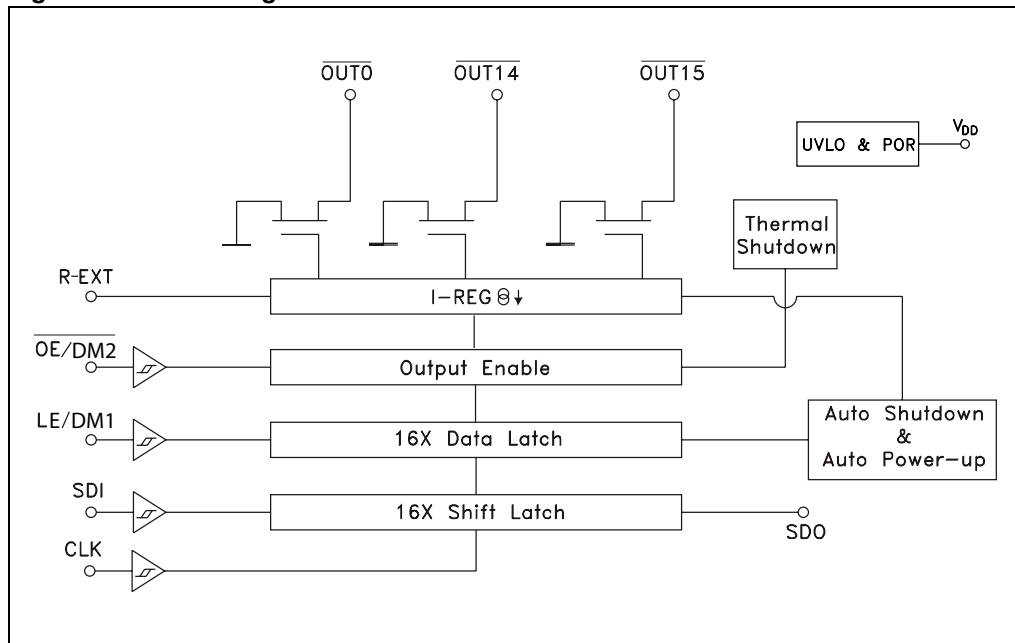


Figure 6. Block diagram



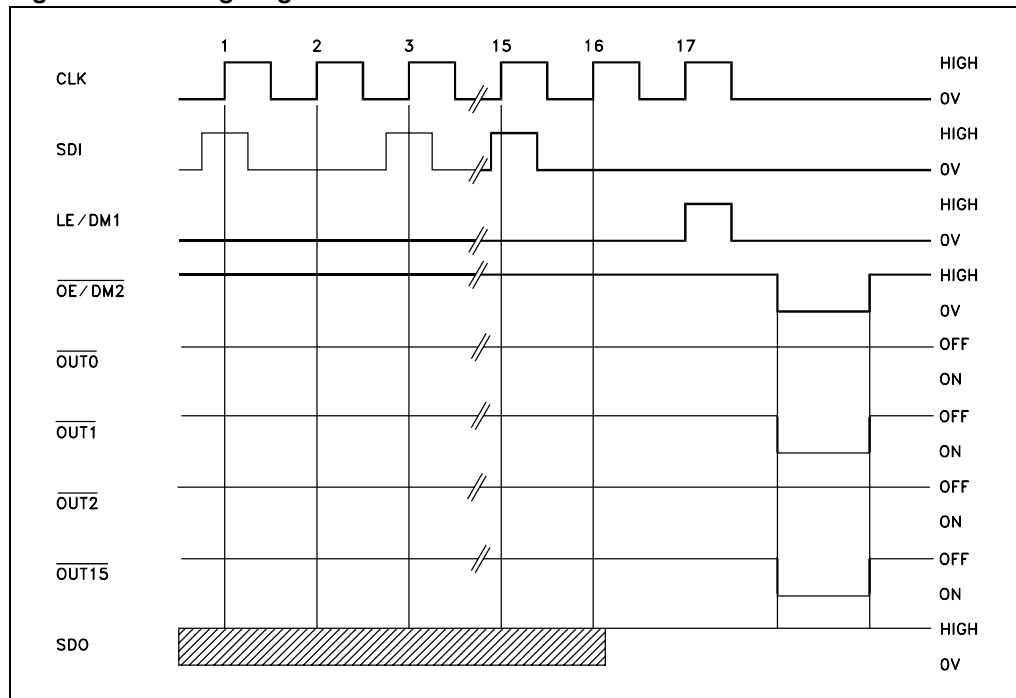
## 5 Timing diagrams

Table 9. Truth table

CLOCK	LE/DM1	OE/DM2	SERIAL-IN	OUT0 ..... OUT7 ..... OUT15	SDO
	H	L	Dn	Dn ..... Dn - 7 ..... Dn - 15	Dn - 15
	L	L	Dn + 1	No change	Dn - 14
	H	L	Dn + 2	Dn + 2 ..... Dn - 5 ..... Dn - 13	Dn - 13
	X	L	Dn + 3	Dn + 2 ..... Dn - 5 ..... Dn - 13	Dn - 13
	X	H	Dn + 3	OFF	Dn - 13

Note:  $OUTn = ON$  when  $Dn = H$   $OUTn = OFF$  when  $Dn = L$

Figure 7. Timing diagram



- Note:
- 1 Latch and output enable terminals are level-sensitive and are not synchronized with rising or falling edge of LE/DM1 signal.
  - 2 When LE/DM1 terminal is low level, the latch circuit holds previous set of data.
  - 3 When LE/DM1 terminal is high level, the latch circuit refreshes new set of data from SDI chain.
  - 4 When OE/DM2 terminal is at low level, the output terminals Out 0 to Out 15 respond to data in the latch circuits, either '1' for ON or '0' for OFF.
  - 5 When OE/DM2 terminal is at high level, all output terminals are switched OFF.

**Table 10. Enable IO: shutdown truth table**

CLOCK	LE/DM1	SDI <sub>0</sub> ..... SDI <sub>7</sub> ..... SDI <sub>15</sub>	SH	Auto Power-up	$\overline{\text{OUTn}}$
	H	All = L	Active	Not active <sup>(1)</sup>	OFF
	L	No change	No change	No change	No change
	H	One or more = H	Not active	Active	X <sup>(2)</sup>

1. At power-up, the device starts in shutdown mode.
2. Undefined.

**Figure 8. Clock, serial-in, serial-out**

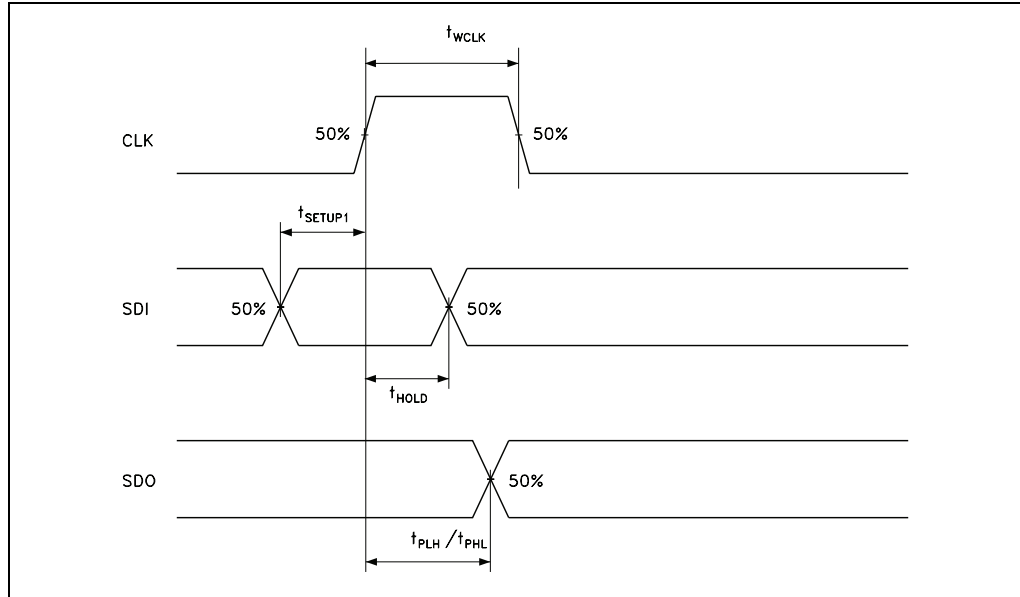


Figure 9. Clock, serial-in, latch, enable, outputs

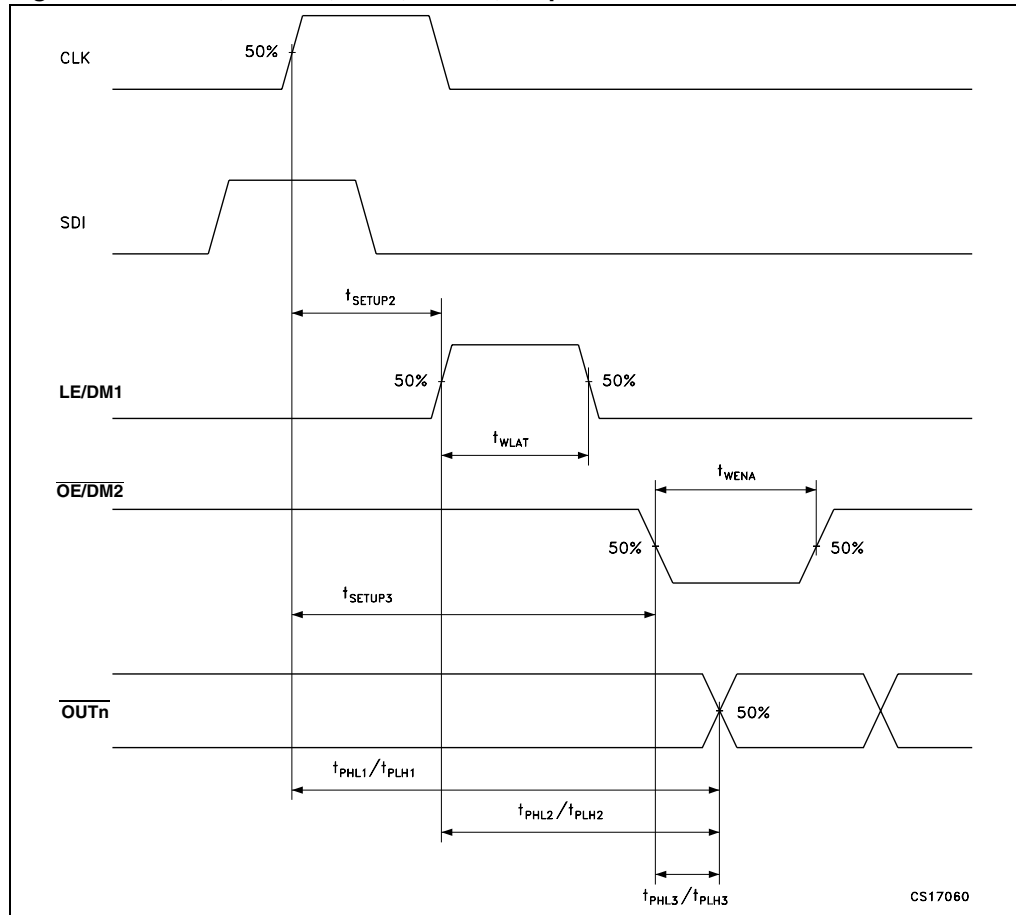
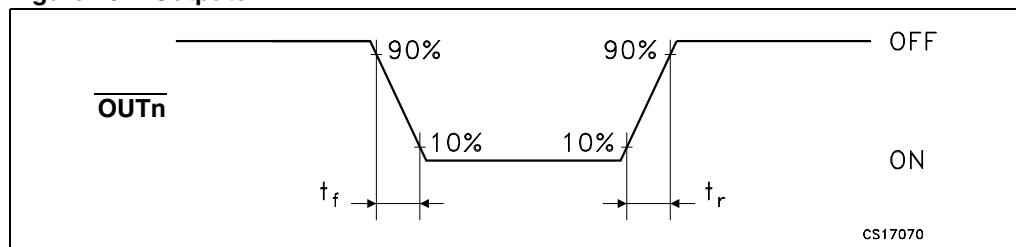


Figure 10. Outputs



## 6 Typical characteristics

Figure 11. Output current vs. R-EXT resistor

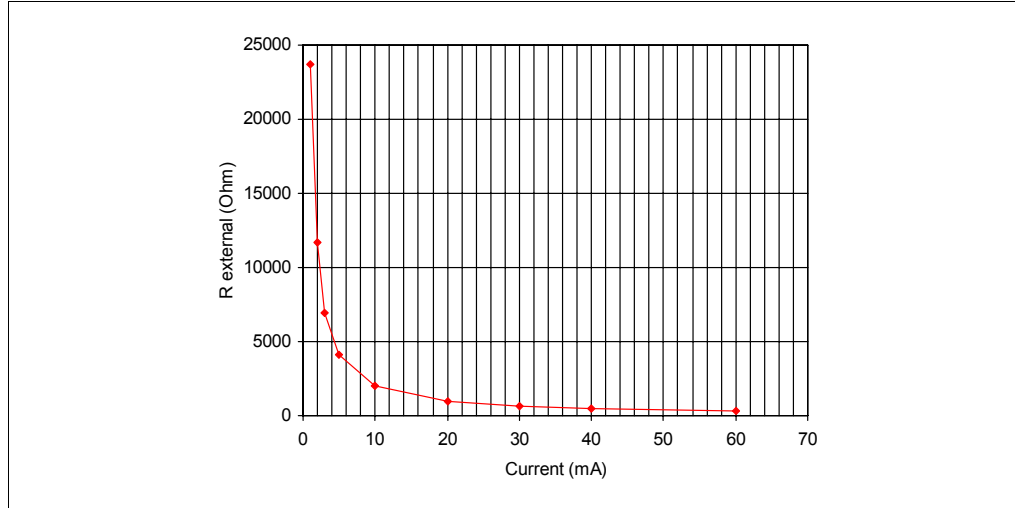


Table 11. Output current vs. R-EXT resistor

R-EXT ( $\Omega$ )	Output current (mA)
23700	1
11730	2
6930	3
4090	5
2025	10
1000	20
667	30
497	40
331	60

Conditions:  
 Temperature = 25 °C,  $V_{DD} = 3.3\text{ V}; 5.0\text{ V}$ ,  $I_{SET} = 3\text{ mA}; 5\text{ mA}; 10\text{ mA}; 20\text{ mA}; 50\text{ mA}; 60\text{ mA}$ .

Figure 12.  $I_{SET}$  vs. dropout voltage ( $V_{drop}$ )

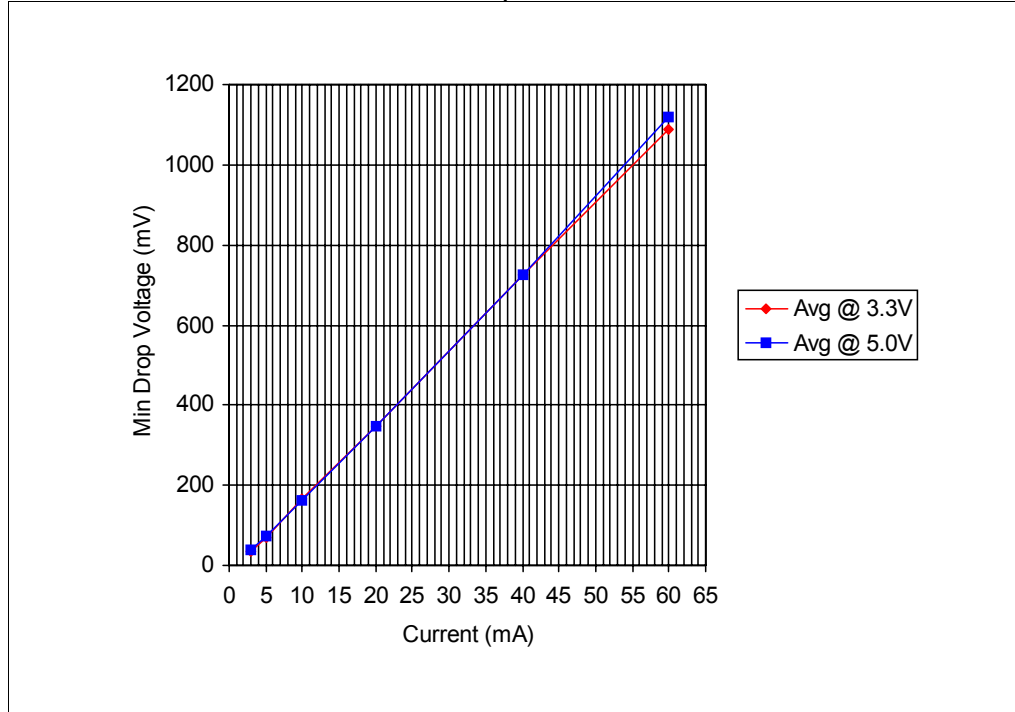


Table 12.  $I_{SET}$  vs. dropout voltage ( $V_{drop}$ )

$I_{out}$ (mA)	Avg (mV) @ 3.3 V	Avg (mV) @ 5.0 V
3	36	37
5	71	72
10	163	163
20	346	347
40	724	726
60	1080	1110

$T_A = 25\text{ }^\circ\text{C}$ ,  $V_{dd} = 3.3\text{ V}; 5\text{ V}$

Figure 13. Output current vs.  $\pm \Delta I_{OL}(\%)$

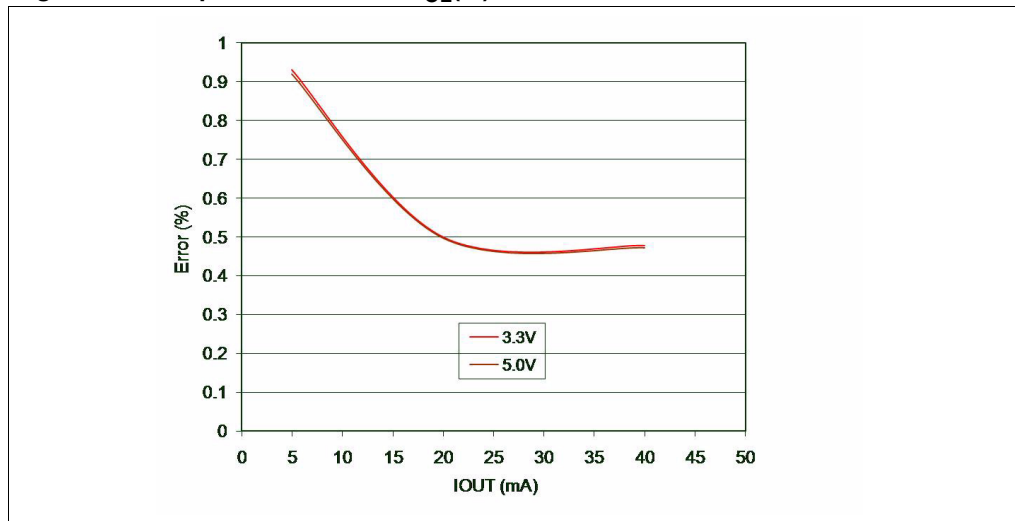


Figure 14. Idd ON/OFF

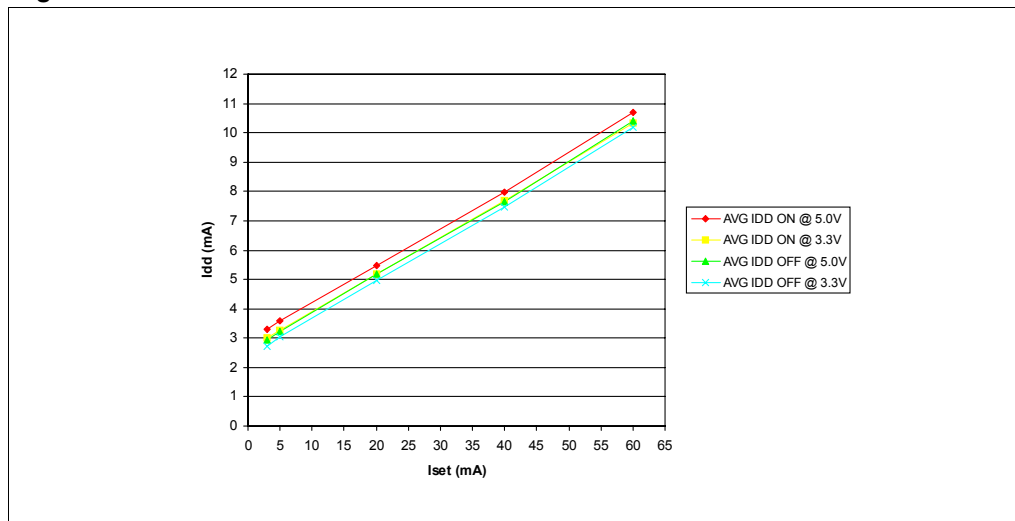
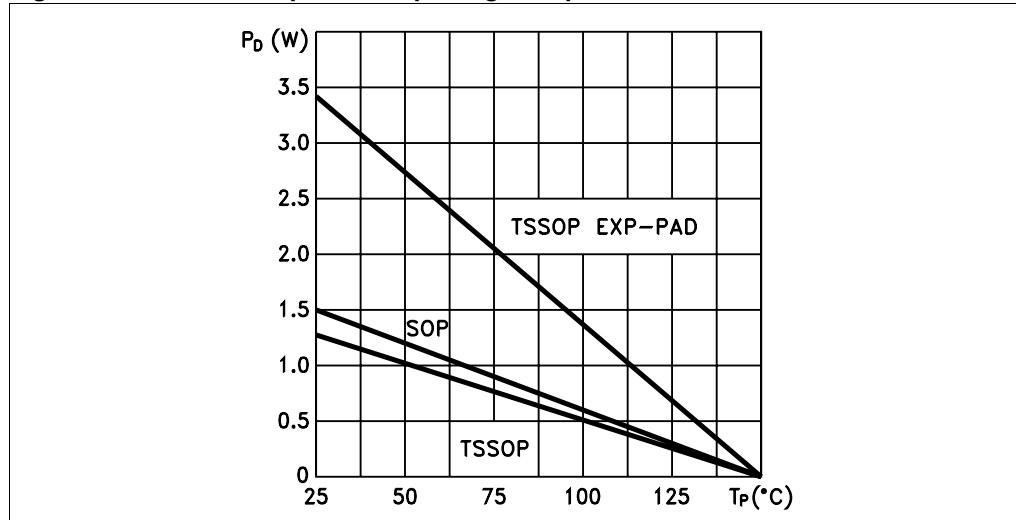




Figure 15. Power dissipation vs. package temperature



Note: The exposed pad should be soldered to the PCB to obtain the thermal benefits.

Figure 16. Turn ON output current characteristics (1)

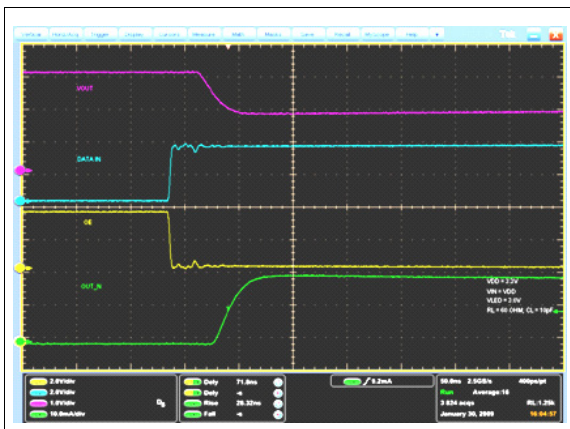
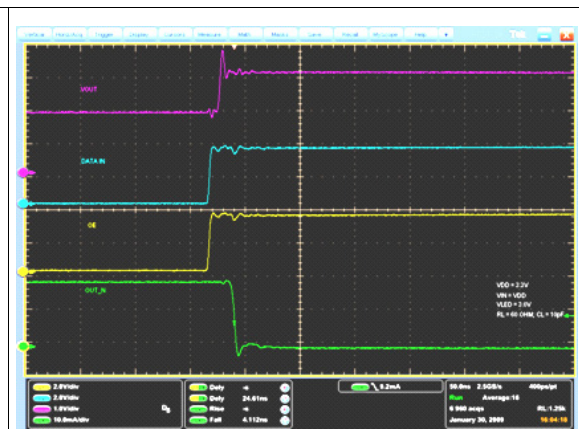


Figure 17. Turn OFF output current characteristics (2)



Electrical conditions:

Vdd = 3.3 V, Vin = Vdd, Vled = 3.0 V, RL = 60 Ω, CL = 10 pF

Ch1 (Yellow) =  $\overline{OE/DM2}$ , Ch2 (Blue) = SDI, Ch3 (Purple) = VOUT, Ch4 (Green) = OUT

1. The reference level for the  $T_{ON}$  characteristics is 50% of  $\overline{OE/DM2}$  signal and 90% of output current
2. The reference level for the  $T_{OFF}$  characteristics is 50% of  $\overline{OE/DM2}$  signal and 10% of output current

## 7 Error detection mode functionality

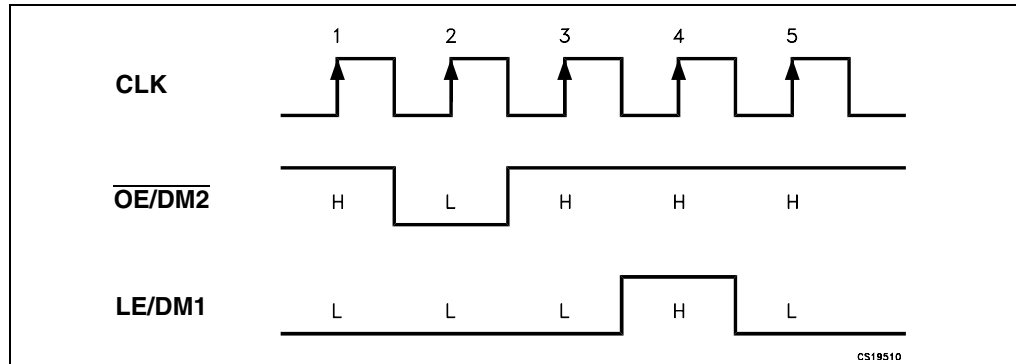
### 7.1 Phase one: entering error detection mode

From the “normal mode” condition the device can switch to “error mode” by a logic sequence on the  $\overline{OE/DM2}$  and LE/DM1 pins, as shown in the following table and diagram:

**Table 13. Entering error detection mode - truth table**

CLK	1°	2°	3°	4°	5°
$\overline{OE/DM2}$	H	L	H	H	H
LE/DM1	L	L	L	H	L

**Figure 18. Entering error detection mode - timing diagram**

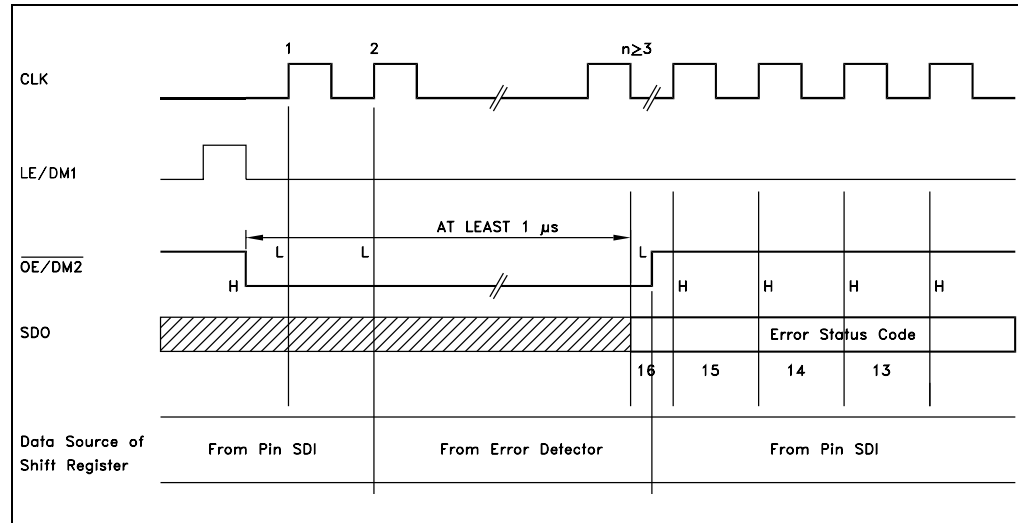


After these five CLK cycles, the device goes into “error detection mode” and at the rising edge of the 6th CLK cycle, the SDI data are ready for sampling.

## 7.2 Phase two: error detection

The 16 data bits must be set to "1" in order for all the outputs to be ON during error detection. The data are latched by LE/DM1, after which the outputs are ready for the detection process. When the microcontroller switches the  $\overline{OE/DM2}$  to LOW, the device drives the LEDs to analyze if an OPEN or SHORT condition has occurred.

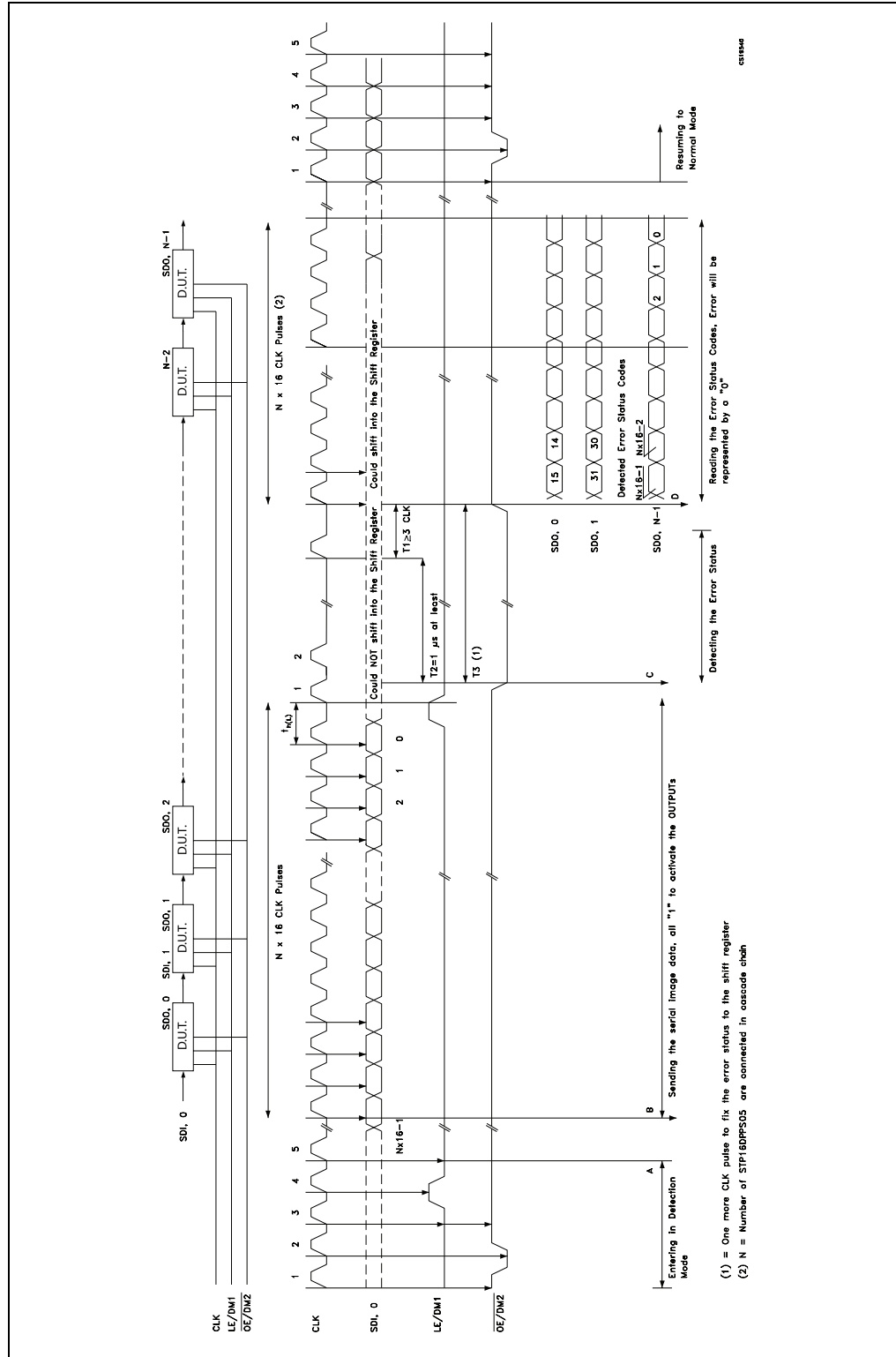
Figure 19. Detection diagram



The status of the LEDs is detected in at least 1 microsecond, and after this period the microcontroller sets  $\overline{OE/DM2}$  to HIGH state and the output data detection result is sent to the microcontroller via SDO.

Error detection mode and normal mode both use the same data format. As soon as all the detection data bits are available on the serial line, the device may return to normal mode of operation. To re-detect the status, the device must first return to normal mode and reenter error detection mode.

Figure 20. Timing example for open and/or short-circuit detection



### 7.3 Phase three: resuming normal mode

The sequence for reentering normal mode is shown in the following table:

Figure 21. Resuming normal mode - timing diagram

CLK	1°	2°	3°	4°	5°
$\overline{\text{OE/DM2}}$	H	L	H	H	H
LE/DM1	L	L	L	L	L

*Note:* For proper device operation, the “entering error detection” sequence must be followed by a “resume mode” sequence, it is not possible to insert consecutive equal sequences.

### 7.4 Error detection conditions

Table 14. Detection conditions ( $V_{DD} = 3.3$  to 5 V, temperature range  $-40$  to  $125$  °C)

Configuration	Detect mode	Detection results		
SW-1 or SW-3b	Open line or output short to GND detected	$\implies I_{ODEC} \leq 0.5 \times I_O$	No error detected	$\implies I_{ODEC} \geq 0.5 \times I_O$
SW-2 or SW-3a	Short on LED or short to V-LED detected	$\implies V_O \geq 2.6$ V	No error detected	$\implies V_O \leq 2.3$ V

*Note:* Where:  $I_O$  = the output current programmed by the *R-EXT*,  $I_{ODEC}$  = the detected output current in detection mode

Figure 22. Detection circuit

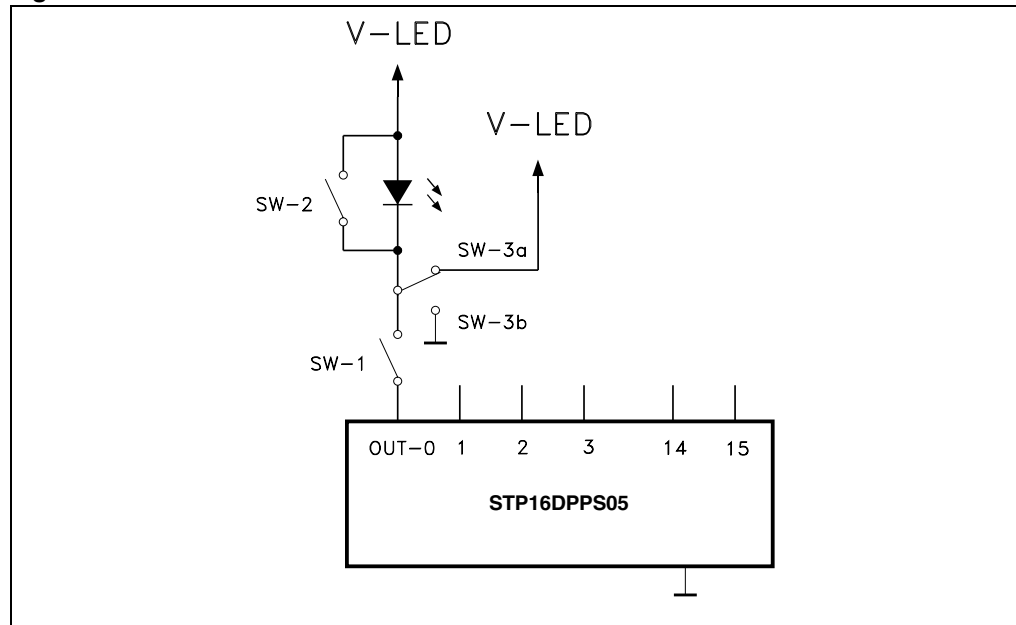
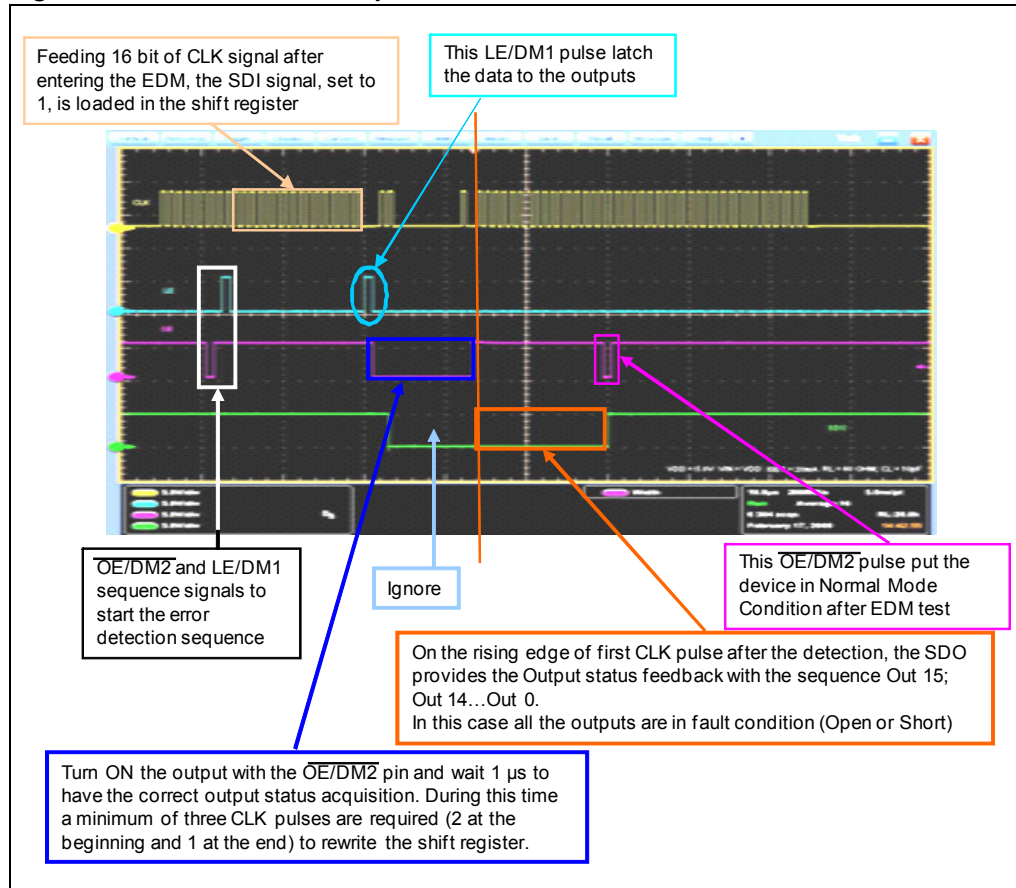


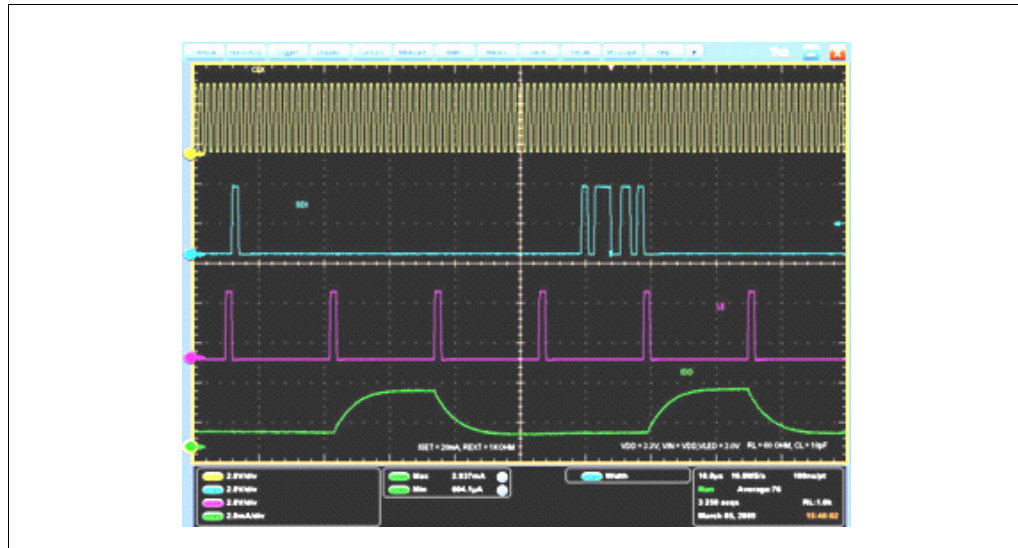
Figure 23. Error detection sequence



## 7.5 Auto power-saving

The auto power-saving feature minimizes the quiescent current if no active data is detected on the latches and auto powers-up the device as the first active data is latched.

Figure 24. Auto power-saving feature



Conditions:

Temp. = 25 °C, Vdd = 3.3 V, Vin = Vdd, VLed = 3.0 V, Iset = 20 mA

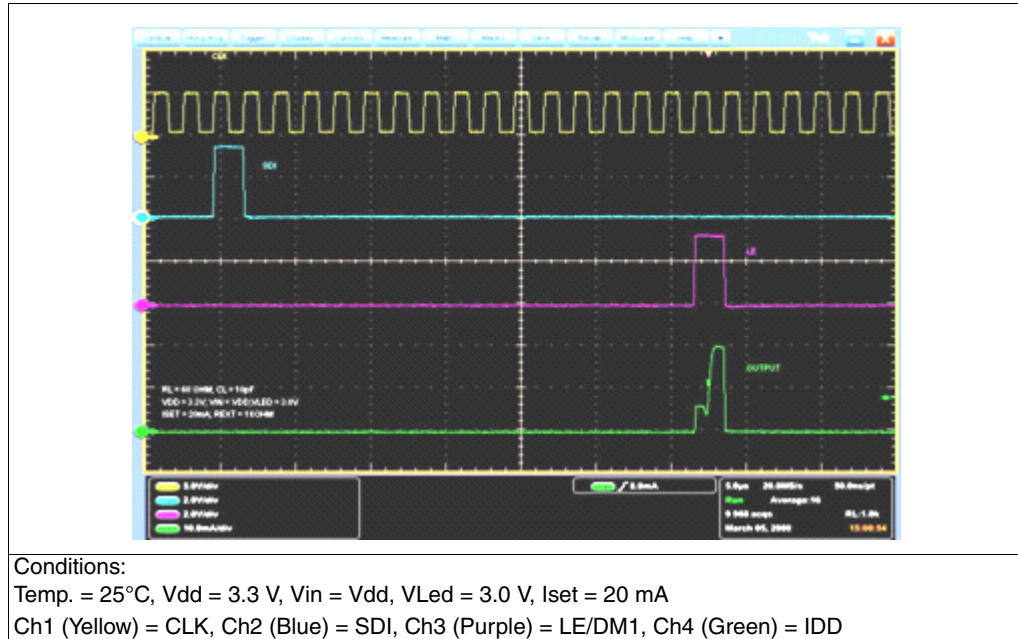
Ch1 (Yellow) = CLK, Ch2 (Blue) = SDI, Ch3 (Purple) = LE/DM1, Ch4 (Green) = IDD

IDD consumption:

IDD (normal operation) = 2.93 mA

IDD (shutdown condition) = 170  $\mu$ A

Figure 25. Auto power-saving feature



*Note:* When the device goes from auto power-saving to normal operating condition, the first output that switches ON shows the  $T_{ON}$  condition as seen in the plot above.



## 8 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

**Table 15. QSOP-24 mechanical data**

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.54	1.62	1.73	0.061	0.064	0.068
A1	0.1	0.15	0.25	0.004	0.006	0.010
A2		1.47			0.058	
b	0.31	0.2		0.012	0.008	
c	0.254	0.17		0.010	0.007	
D	8.56	8.66	8.76	0.337	0.341	0.345
E	5.8	6	6.2	0.228	0.236	0.244
E1	3.8	3.91	4.01	0.150	0.154	0.158
e		0.635			0.025	
L	0.4	0.635	0.89	0.016	0.025	0.035
h	0.25	0.33	0.41	0.010	0.013	0.016
<	8°	0°				

Figure 26. QSOP-24 package dimensions

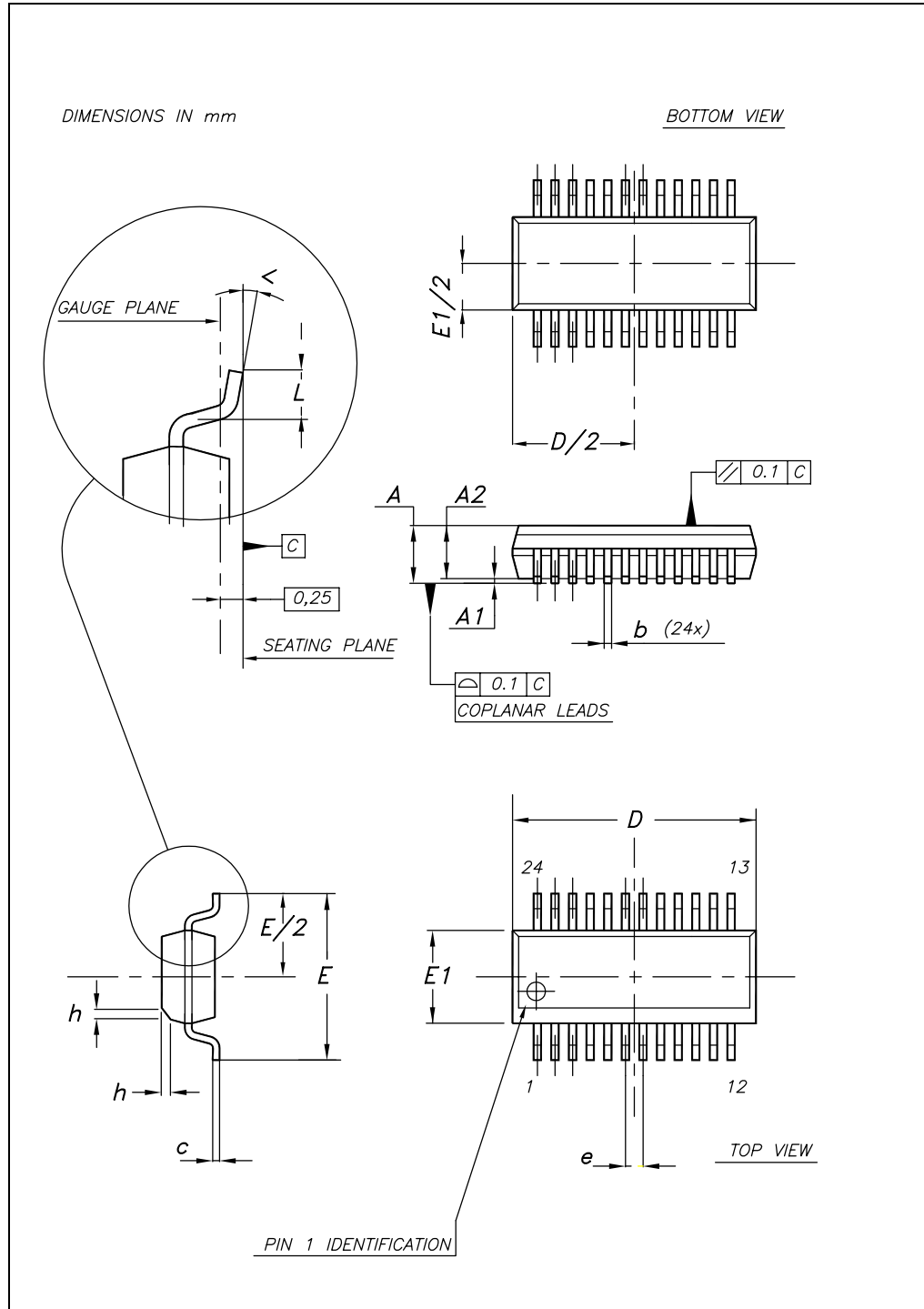


Table 16. QSOP-24 tape and reel

Dim.	mm.			Inches		
	Min	Typ	Max	Min	Typ	Max
R1	12.8	13	13.5	5.039	5.118	5.315
R2		330			129.921	
R3		100			39.37	
eint		16.4			6.457	
e1	1.5	2	2.5	0.591	0.787	0.984

Figure 27. QSOP-24 tape and reel dimensions

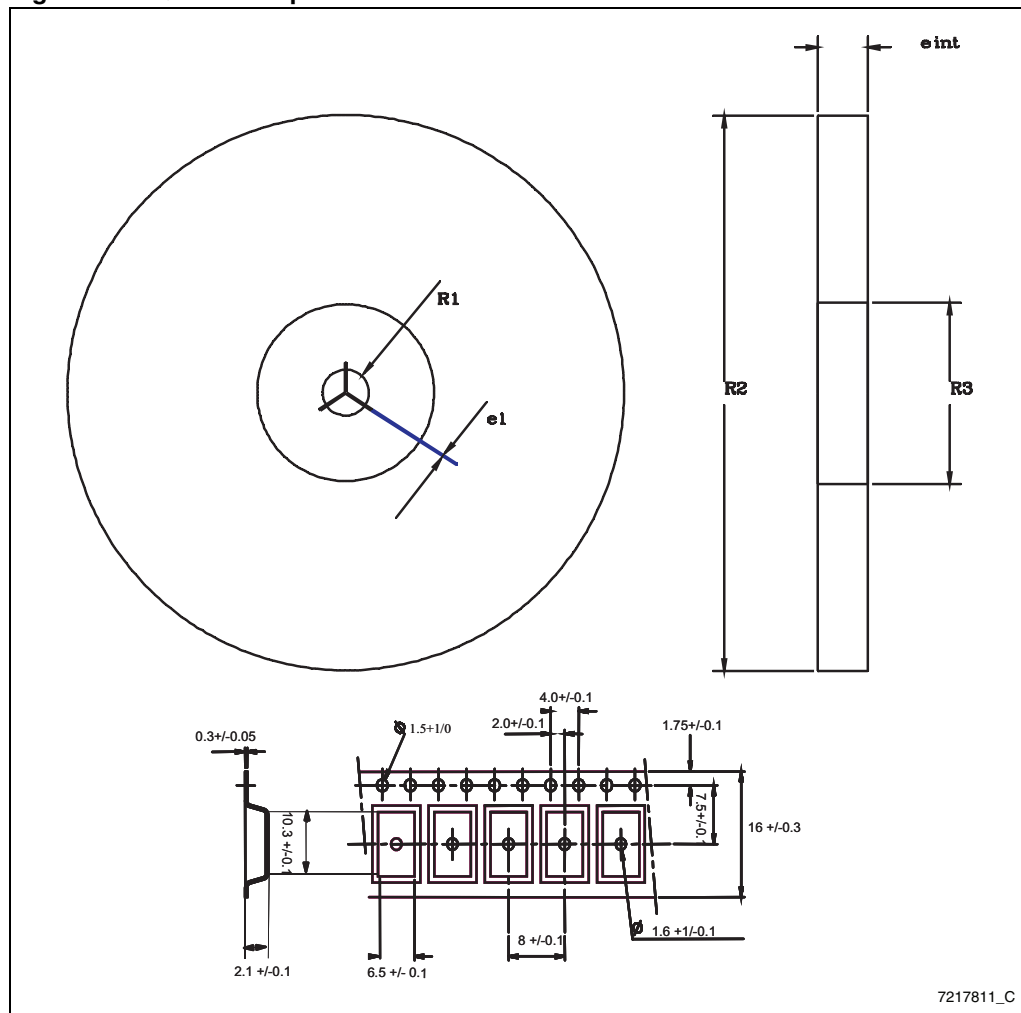


Table 17. TSSOP24 mechanical data

Dim.	mm.			Inches		
	Min	Typ	Max	Min	Typ	Max
A			1.1			0.043
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	7.7		7.9	0.303		0.311
E	4.3		4.5	0.169		0.177
e		0.65 BSC			0.0256 BSC	
H	6.25		6.5	0.246		0.256
K	0°		8°	0°		8°
L	0.50		0.70	0.020		0.028

Figure 28. TSSOP24 package dimensions

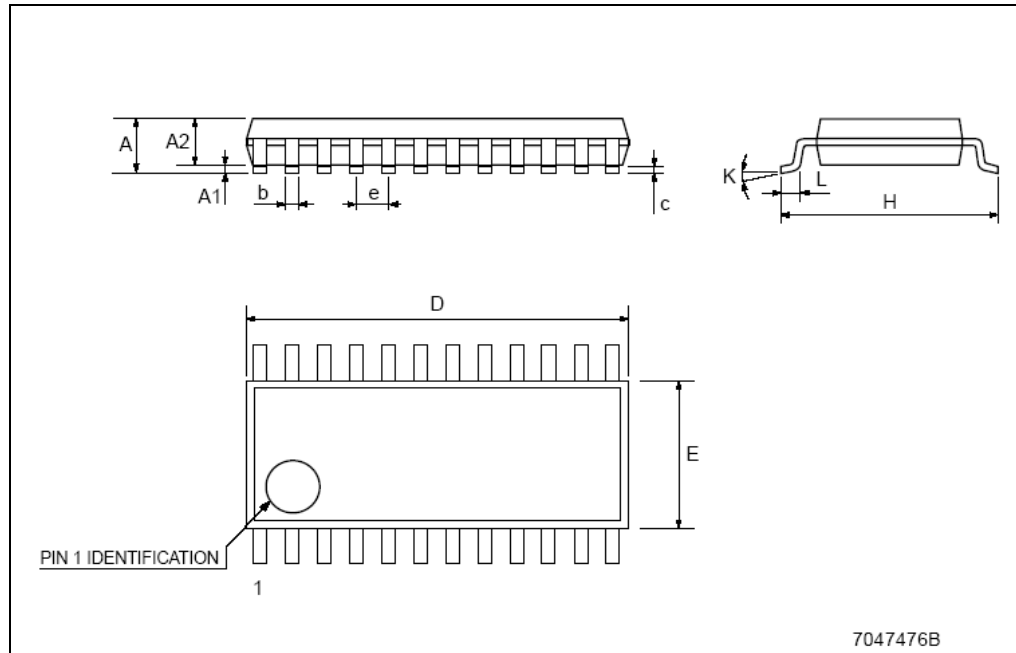
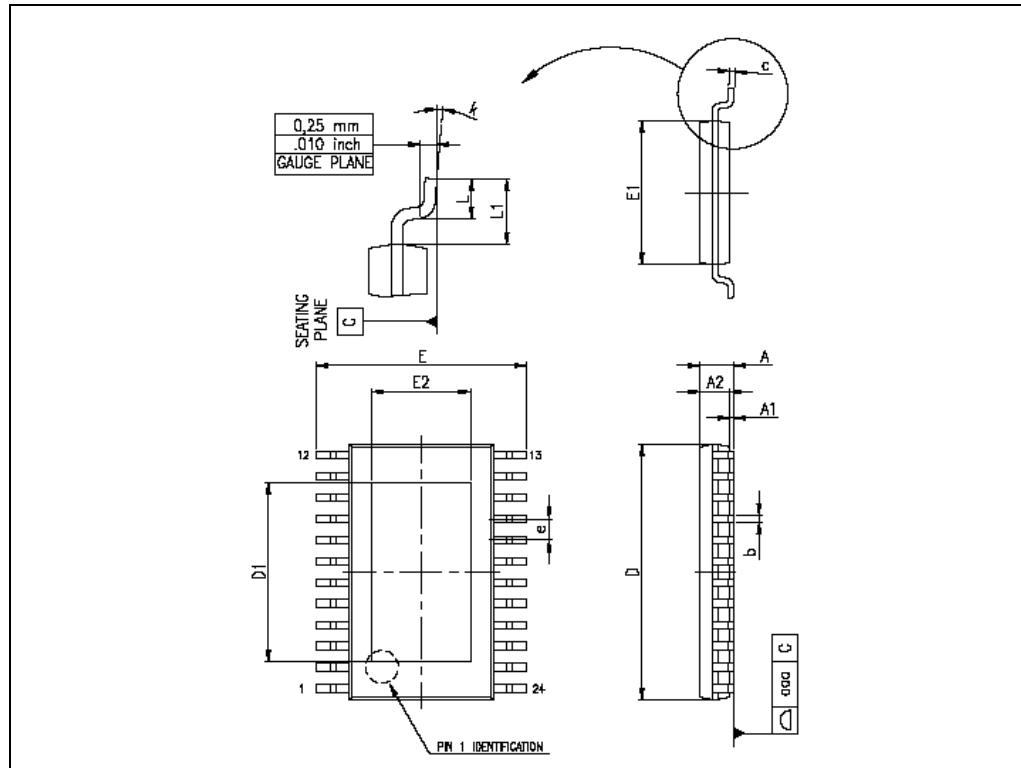


Table 18. TSSOP24 exposed pad mechanical data

Dim.	mm			Inches		
	Min	Typ	Max	Min	Typ	Max
A			1.2			0.047
A1			0.15		0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	7.7	7.8	7.9	0.303	0.307	0.311
D1	4.7	5.0	5.3	0.185	0.197	0.209
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
E2	2.9	3.2	3.5	0.114	0.126	0.138
e		0.65			0.0256	
K	0°		8°	0°		8°
L	0.45	0.60	0.75	0.018	0.024	0.030

Figure 29. TSSOP24 exposed pad dimensions



**Table 19. Tape and reel TSSOP24 and TSSOP24 exposed pad**

Dim.	mm.			Inches		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.8		7	0.268		0.276
Bo	8.2		8.4	0.323		0.331
Ko	1.7		1.9	0.067		0.075
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

**Figure 30. TSSOP24 and TSSOP24 exposed pad tape and reel dimensions**

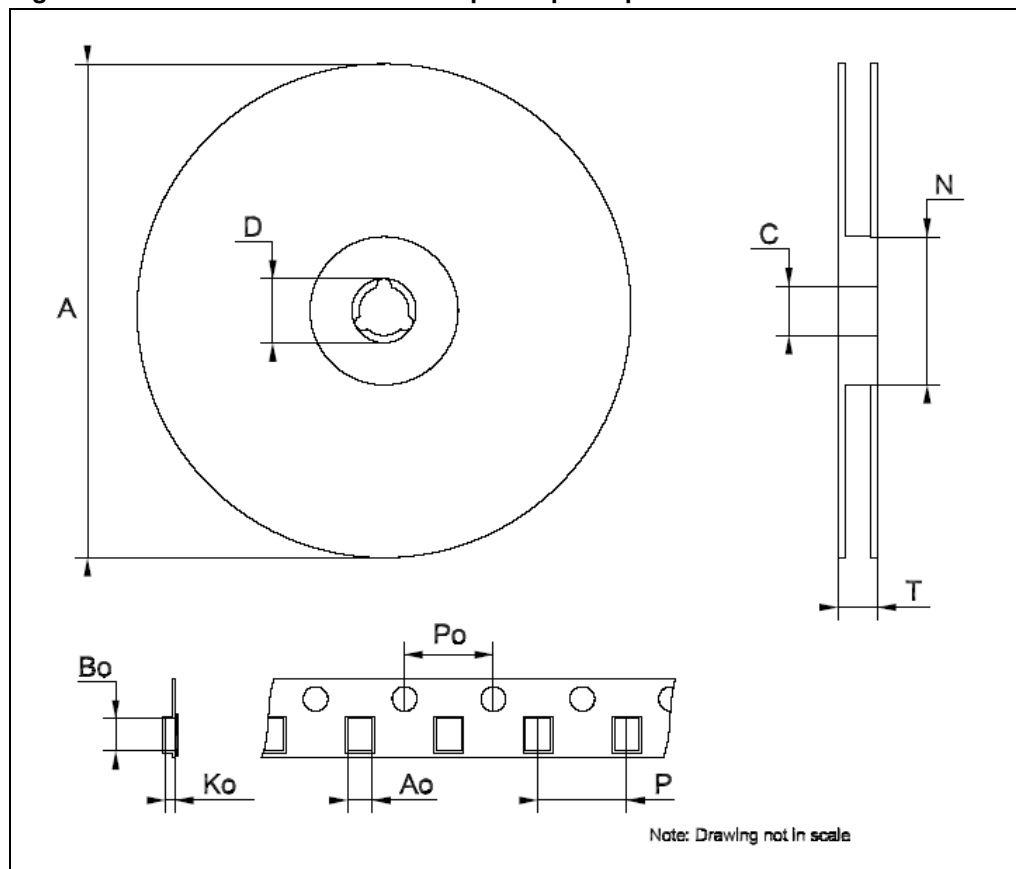


Table 20. SO-24 mechanical data

Dim.	mm.			Inches		
	Min	Typ	Max	Min	Typ	Max
A			2.65			0.104
a1	0.1		0.2	0.004		0.008
a2			2.45			0.096
b	0.35		0.49	0.014		0.019
b1	0.23		0.32	0.009		0.012
C		0.5			0.020	
c1	45°(typ.)					
D	15.20		15.60	0.598		0.614
E	10.00		10.65	0.393		0.419
e		1.27			0.050	
e3		13.97			0.550	
F	7.40		7.60	0.291		0.300
L	0.50		1.27	0.020		0.050
S	°(max.) 8					

Figure 31. SO-24 package dimensions

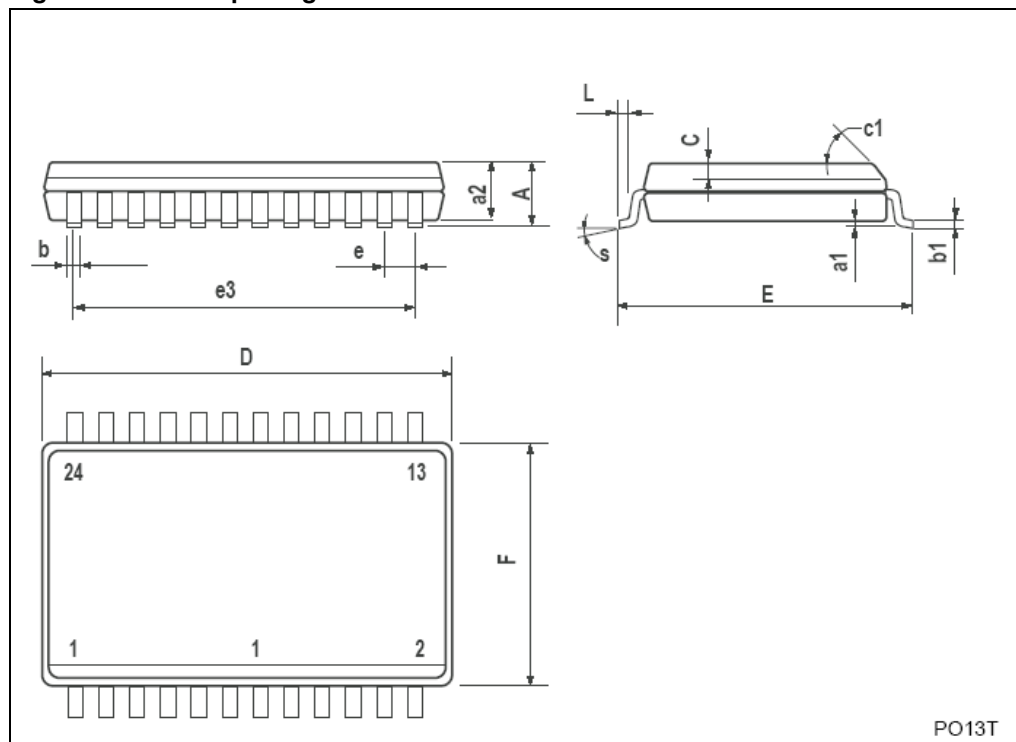
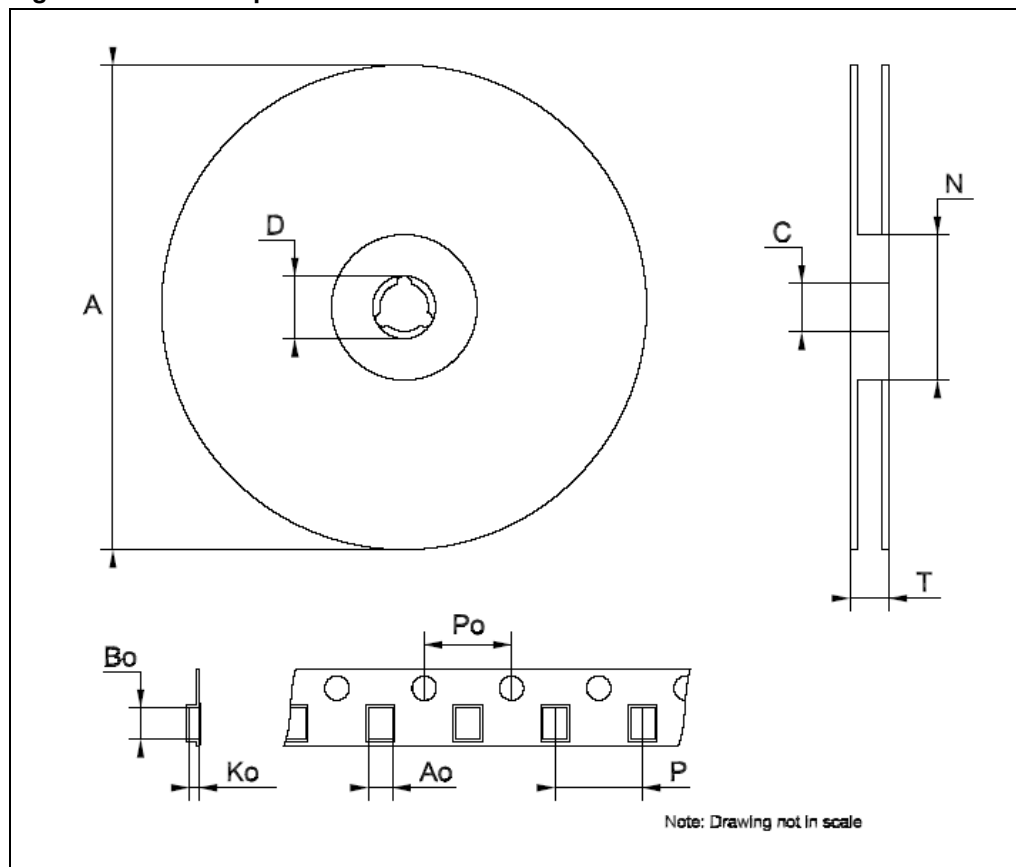


Table 21. Tape and reel SO-24

Dim.	mm.			Inches		
	Min	Typ	Max	Min	Typ	Max
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	10.8		11.0	0.425		0.433
Bo	15.7		15.9	0.618		0.626
Ko	2.9		3.1	0.114		0.122
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476

Figure 32. SO-24 tape and reel dimensions





## 9 Revision history

**Table 22. Document revision history**

Date	Revision	Changes
05-Jun-2009	1	Initial release.
23-Oct-2009	2	Updated document status from preliminary status to final and <i>Note: on page 3</i>

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