

6-Channel Ultra Low Dropout LED Driver

FEATURES

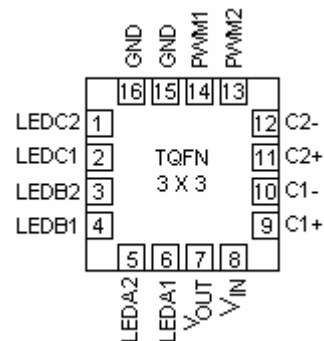
- Charge pump modes: 1-x, 1.33-x, 1.5-x, 2-x
- Ultra low dropout PowerLite™ Current Regulator*
- Drives up to 6 LEDs up to 32 mA each
- Factory preset current value for each LED bank
- PWM brightness control with up to 25,000:1 dimming range at 200 Hz
- Power efficiency up to 94%
- Low input noise & ripple in all charge pump modes
- Low current shutdown mode
- Short circuit current limiting
- Thermal shutdown protection
- Available in 3 x 3 x 0.8 mm 16-pin TQFN package

APPLICATION

- Keypad and Display Backlight
- Cellular Phones
- Digital Still Cameras
- PDAs and Smartphones

DESCRIPTION

The LDS8866 is a high efficiency multi-mode fractional charge pump with ultra low dropout voltage that can drive up to six LEDs. Inclusion of a 1.33-x fractional charge pump mode and ultra low dropout



PowerLite™ Current Regulator (PCR) increases device' efficiency up to 94%. New mode requires no additional external capacitors.

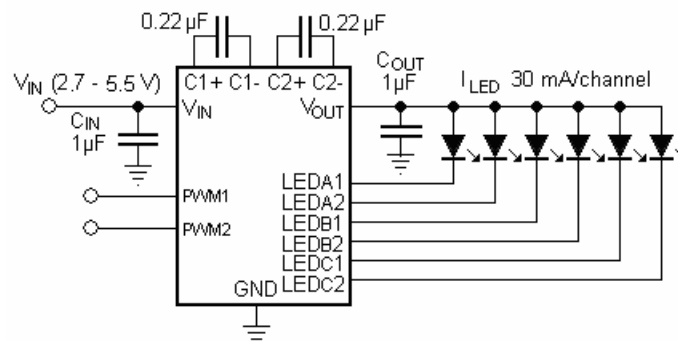
The PWM1/PWM2 logic inputs function as a chip enable and a PWM mode LED brightness control. PWM1 pin controls LEDA and LEDB banks with four LEDs, while PWM2 controls bank LEDC with two LEDs.

The maximum LEDs current is factory preset. Every LED bank with two LEDs each is programmable separately in the range from 0.5 to 32 mA in 0.5 mA steps.

Low noise input ripple is achieved by operating at a constant switching frequency which allows the use of small external ceramic capacitors. The multi-fractional charge pump supports a wide range of input voltages from 2.7 V to 5.5 V.

The device is available in a 16-lead TQFN 3 mm x 3 mm package with a max height of 0.8 mm.

TYPICAL APPLICATION CIRCUIT



ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V _{IN} , LEDx, C1±, C2± voltage	6	V
V _{OUT} voltage	6	V
PWM1, PWM2 voltage	V _{IN} + 0.7V	V
Storage Temperature Range	-65 to +160	°C
Junction Temperature Range	-40 to +125	°C
Soldering Temperature	300	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
V _{IN}	2.7 to 5.5	V
Ambient Temperature Range	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS

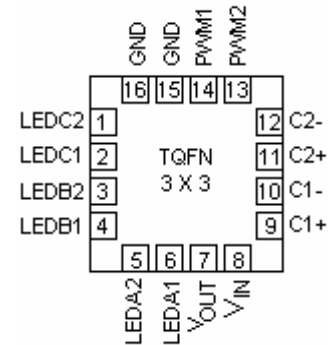
(Over recommended operating conditions unless specified otherwise) V_{IN} = 3.6V, C_{in} = C_{out} = 1 μF, C1 = C2 = 0.22 μF, EN = High, T_{AMB} = 25°C

Name	Conditions	Min	Typ	Max	Units
Quiescent Current	1-x mode		1.7	2.5	mA
Shutdown Current	PWM1 = PWM2 = 0V			1	μA
LED Current Accuracy	To factory preset value	-5	±3	+5	%
LED Channel Matching	(I _{LED} - I _{LEDAVG}) / I _{LEDAVG}	-5	±3	+5	%
Output Resistance (open loop) ¹	1-x mode		0.8		Ω
	1.33-x mode		3.5		
	1.5-x mode		5.5		
	2-x mode		6.5		
Charge Pump Frequency	1.33-x		0.8		MHz
	1.5-x mode and 2-x		1.1		
Output short circuit Current Limit	V _{OUT} < 0.5V		35		mA
1-x to 1.33-x, 1.33-x to 1.5-x, or 1.5-x to 2-x Mode Transition Threshold			75	130	mV
1.33-x to 1-x Mode Transition Hysteresis			600		mV
Charge Pump Transition Filter delay ¹			800		μs
PWM1, PWM2 pins	Input Leakage	-1		1	μA
	Logic Level	High	1.3		V
Low				0.4	
PWM frequency ¹		100		100000	Hz
PWM Pulse HIGH/LOW state			200		ns
PWM Low Time to Shutdown			30		ms
Thermal Shutdown ¹			150		°C
Thermal Hysteresis ¹			20		
V _{IN} Under Voltage Lockout (UVLO)			2.2		V
V _{OUT} Over Voltage Protection ¹				6.2	V

¹ Sample test only

PIN DESCRIPTION

Pin #	Name	Function
1	LEDC2	LEDC2 cathode terminal
2	LEDC1	LEDC1 cathode terminal
3	LEDB2	LEDB2 cathode terminal
4	LEDB1	LEDB1 cathode terminal
5	LEDA2	LEDA2 cathode terminal
6	LEDA1	LEDA1 cathode terminal
7	V _{OUT}	Charge pump output connected to the LED anodes
8	V _{IN}	Charge pump input, connect to battery or supply
9	C1+	Bucket capacitor 1 Positive terminal
10	C1-	Bucket capacitor 1 Negative terminal
11	C2+	Bucket capacitor 2 Positive terminal
12	C2-	Bucket capacitor 2 Negative terminal
13	PWM2	LEDC bank PWM brightness control
14	PWM1	LEDA and LEDB banks PWM brightness control
15, 16	GND	Connect both pins to GND
TAB	TAB	Bottom Thermal Pad; connect to GND on the PCB



Top view: TQFN 16-lead 3 X 3 mm

PIN FUNCTION

V_{IN} is the supply pin for the charge pump. A small 1 μ F ceramic bypass capacitor is required between the V_{IN} pin and ground near the device. The operating input voltage range is from 2.7 V to 5.5 V. Whenever the input supply falls below the under-voltage threshold (2.2 V), all the LED channels are disabled, and the device enters shutdown mode.

PWM1, PWM2 are the enable and PWM LED brightness control logic inputs. Guaranteed levels of logic high and logic low are set at 1.3 V and 0.4 V respectively. When any of PWM pins is taken high, the device becomes enabled with maximum LED current at associated bank. To place the device into zero current mode, both PWM pins must be held low for more than 30 ms.

V_{OUT} is the charge pump output that is connected to the LED anodes. A small 1 μ F ceramic bypass

capacitor is required between the V_{OUT} pin and ground near the device.

GND is the ground reference for the charge pump. The pin must be connected to the ground plane on the PCB.

C1+, C1- are connected to each side of the ceramic bucket capacitor C1

C2+, C2- are connected to each side of the ceramic bucket capacitor C2

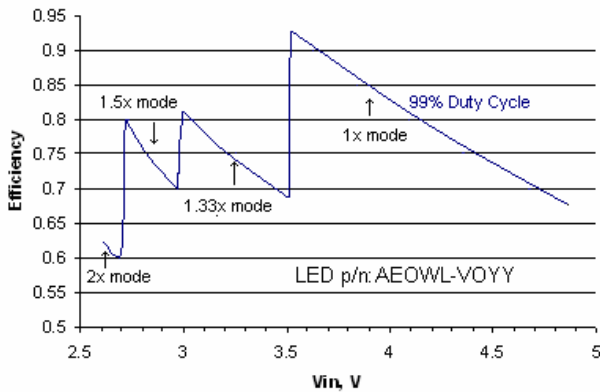
LEDA1 – LEDC2 provide the internal regulated current source for each of the LED cathodes. These pins enter high-impedance zero current state whenever the device is in shutdown mode.

TAB is the exposed pad underneath the package. For best thermal performance, the tab should be soldered to the PCB and connected to the ground plane

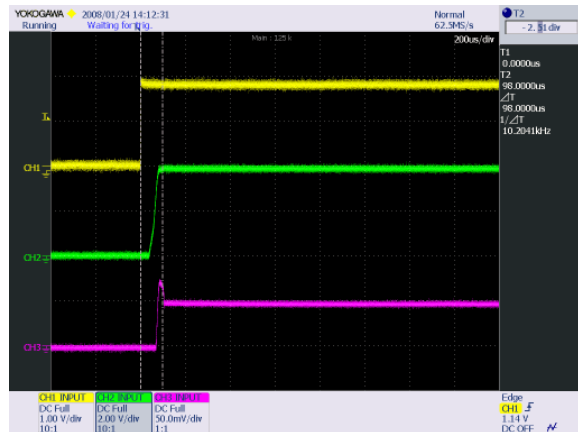
TYPICAL CHARACTERISTICS

$V_{in} = 3.6V$, $I_{OUT} = 180mA$ (6 LEDs at 30mA), $C_1 = C_2 = 0.22 \mu F$, $C_{IN} = C_{OUT} = 1 \mu F$, $T_{AMB} = 25^\circ C$ unless otherwise specified

Power Efficiency vs. Input Voltage at $V_F = 3.2 V$

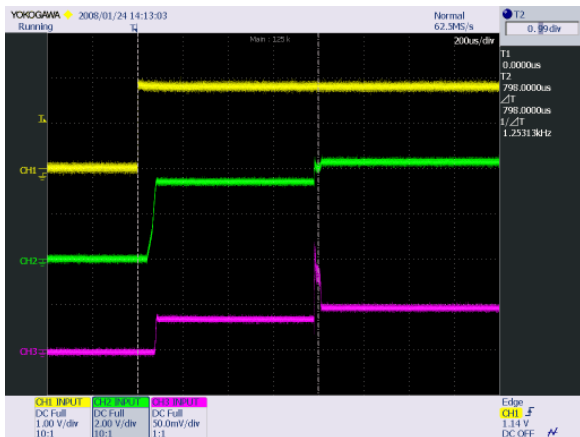


Power-Up in 1-x mode



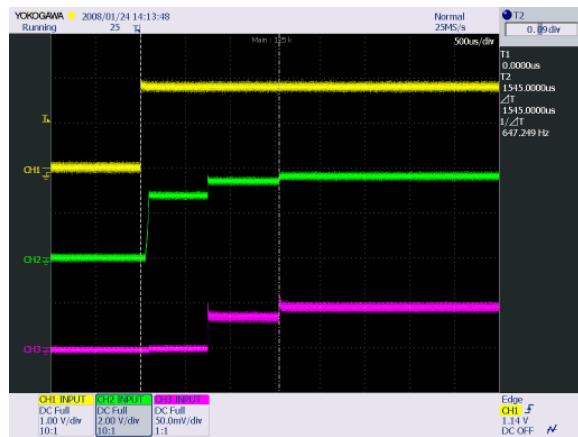
Ch1 – PWM, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Power-Up in 1.33-x Mode



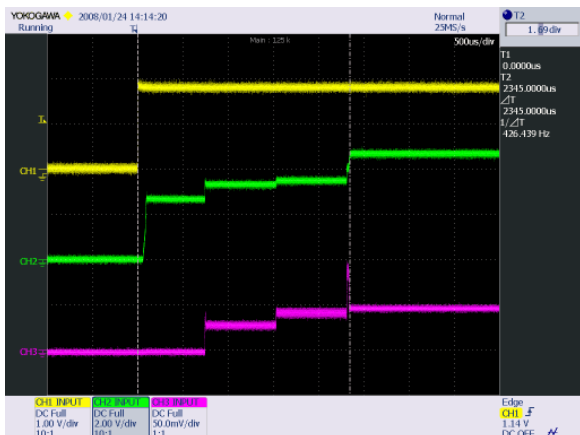
Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Power-Up in 1.5-x Mode



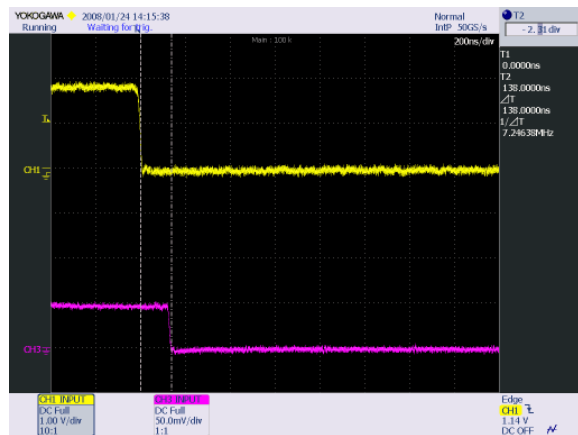
Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Power-Up in 2-x Mode



Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Power-Down Delay (1-x Mode)

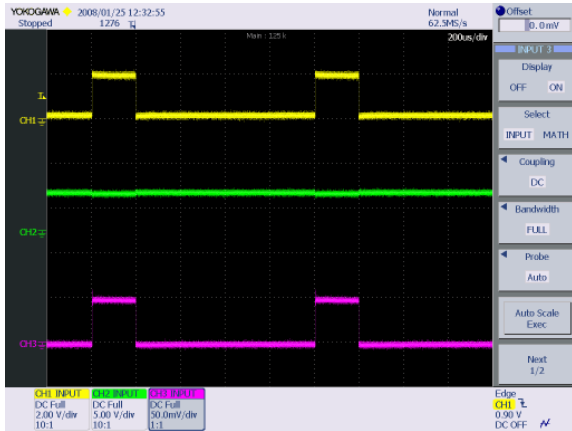


Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

TYPICAL CHARACTERISTICS

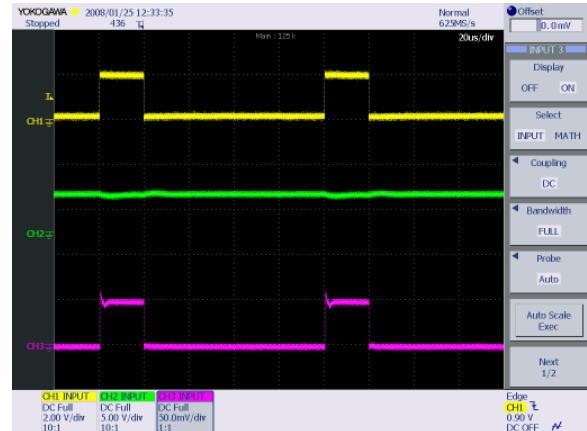
$V_{in} = 3.6V$, $I_{OUT} = 180mA$ (6 LEDs at 30mA), $C_1 = C_2 = 0.22 \mu F$, $C_{IN} = C_{OUT} = 1 \mu F$, $T_{AMB} = 25^\circ C$ unless otherwise specified

Operating Waveforms at 1kHz PWM mode



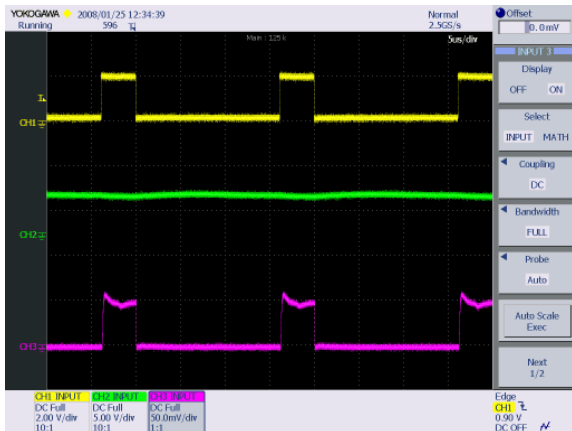
Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Operating Waveforms at 10kHz PWM mode



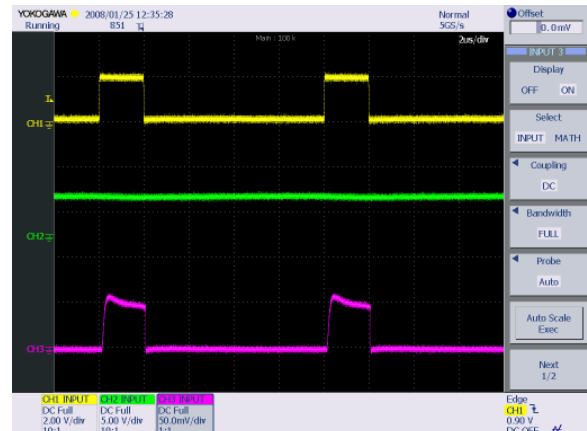
Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Operating Waveforms at 50kHz PWM mode



Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

Operating Waveforms at 100kHz PWM mode



Ch1 – PWM1, PWM2, Ch2 – Vout,
Ch3 – Output current (100mA/div)

BLOCK DIAGRAM

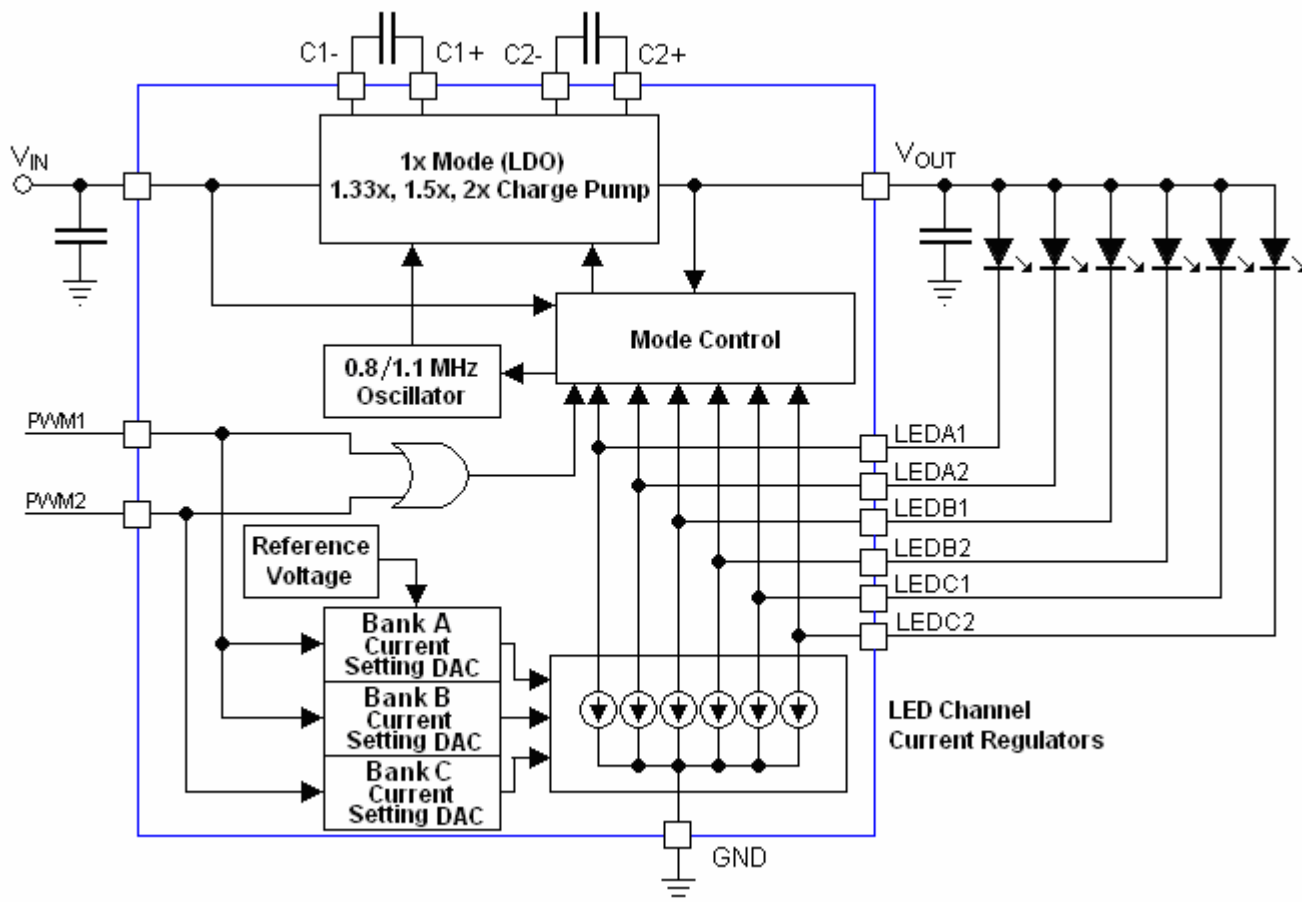


Figure 2. LDS8866 Functional Block Diagram

BASIC OPERATION

At power-up, PWM1 and PWM2 pins should be logic LOW. During power-up device performs internal circuits reset that requires less than 10 μ s. To start device either PWM1 or PWM2 pin should be set logic HIGH 10 μ s after than input voltage applied. Device starts operating at 1-x mode at which the output is approximately equal to the input supply voltage (less any internal voltage losses). If the output voltage is sufficient to regulate all LED currents, the device remains in 1-x operating mode.

The low dropout PowerLite™ Current regulator (PCR) performs well at input voltages V_{in} up to 75 mV above LED forward voltage V_F significantly increasing driver's efficiency. The LDS8866 monitors voltage drop V_d across PCR at every channel in ON state. If this voltage falls below 75 mV (typical) at any one channel, (channel with LED with highest forward voltage), the Mode Control Block changes charge pump mode to the next multiplication ratio.

$V_d = V_{IN} \times M - V_F - R_{cp} \times I_{out}$, where R_{cp} is a Charge Pump Output Resistance at given mode, I_{out} is sum of all LED currents, and M is a charge pump' multiplication ratio.

If the input voltage is insufficient or falls to a level where $V_d \leq 75$ mV, and the regulated currents cannot be maintained, the low dropout PowerLite™ Current Regulator switches the charge pump into 1.33-x mode (after a fixed delay time of about 800 μ s). In 1.33-x mode, the charge pump' output voltage is approximately equal to 1.33 times the input supply voltage (less any internal voltage losses).

This sequence repeats at every mode until driver enters the 2-x mode.

If the device detects a sufficient input voltage is present to drive all LED currents in 1-x mode, it will change automatically back to 1-x mode. This only applies for changing back to the 1-x mode. The difference between the input voltage when exiting 1-x

mode and returning to 1-x mode is called the 1-x mode transition hysteresis (about 600 mV).

Operation of PWM-based LED Current Control

The maximum current value in each of the LDS8866's three LED banks is factory preset; to set each ILED below this value, a PWM (a duty cycle based) control signal can be applied at the PWM1/PWM2 pins.

Using a PWM control technique guarantees stable WLED color temperature over a wide range of LED currents. The LED color temperature set at the factory preset maximum LED current does not vary with respect to the average LED current unlike conventional 1-wire LED current control methods.

The LDS8866's PWM logic control circuits have been designed to operate from 100 Hz to 100 kHz with duty cycles higher than $(0.02 \cdot F)\%$ and lower than $(100 - 0.02 \cdot F)\%$, where F is the PWM control frequency in kHz. The brightness dynamic dimming range at 200 Hz is 25,000 : 1. PWM control frequencies lower than 100 Hz are not recommended (especially with short duty cycles) because LED flicker may become visible.

When PWM current control is enabled, the LED current is modulated from zero to 100% over a single PWM period. For example, when PWM1/PWM2 is logic high, the LED current is set equal to the maximum factory preset value. When PWM1/PWM2 is logic low, the LED current is zero. The average LED current level is then determined by the PWM duty cycle that may be adjusted as described above.

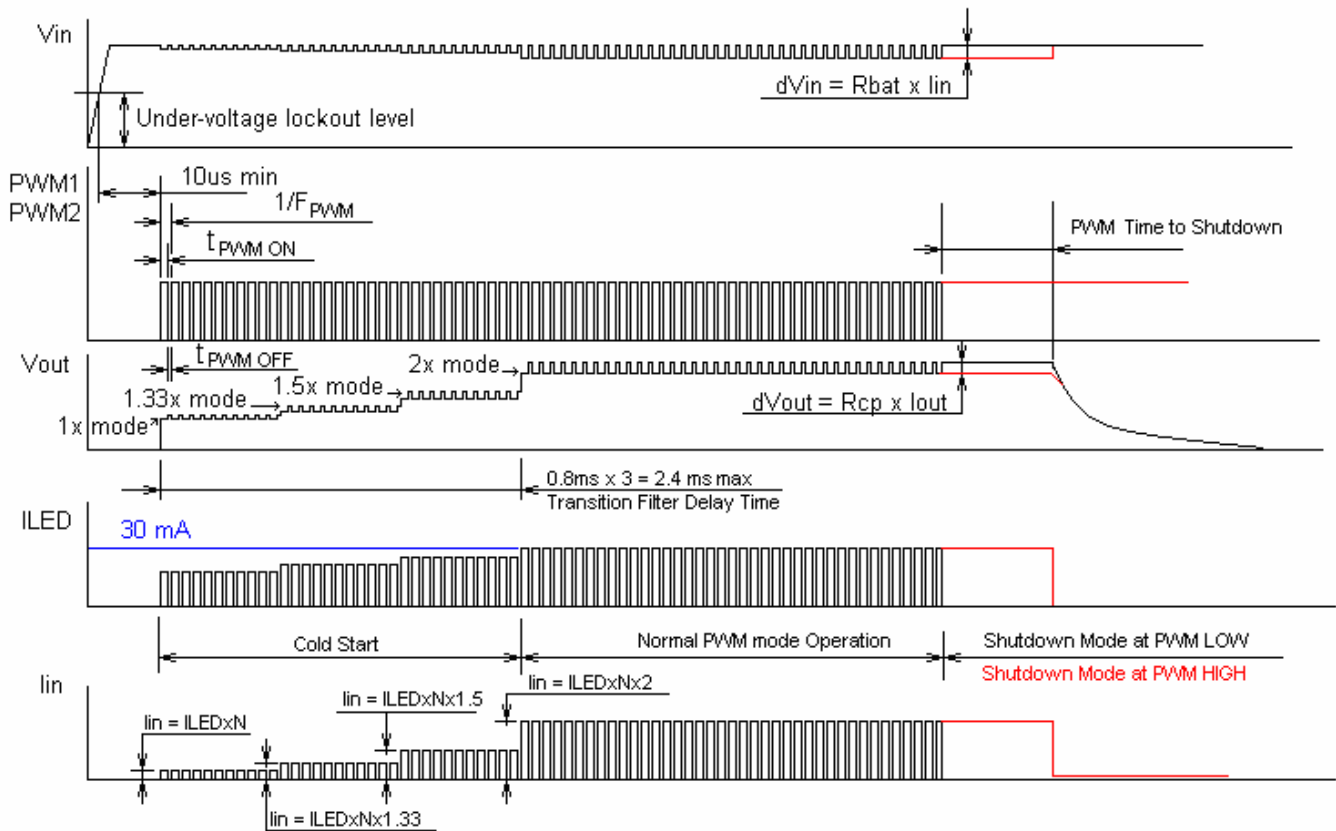


Figure 3. LDS8866 Timing Diagram

Note:

Timing diagram represents condition when LED forward voltage V_f is higher than Charge Pump Mode times(1.5) input voltage minus voltage drop on current regulator V_{PCR} and minus voltage drop on charge pump output resistance R_{cp} at Iled current through N LEDs.

$$V_f > CPM \times V_{in} - V_d - R_{cp} \times I_{led} \times N; \text{ PWM duty Cycle} = T_{PWM\ ON} / (T_{PWM\ ON} + T_{PWM\ OFF})$$

When LED current control is enabled at the PWM1/PWM2 inputs, the LDS8866's maximum input current is determined by the factory preset maximum LED current multiplied by number of LED used, the

charge pump operating mode (1-x, 1.33-x, 1.5-x, or 2-x), and divided by charge-pump driver's efficiency. For example, if six LEDs are used and the charge pump is operating in 2-x mode, the maximum pulse current at V_{IN} would then be 400 mA (= 30 mA/LED x

6LEDs x 2/0.9), assuming that charge pump's efficiency alone at 2-x mode is 90% and maximum factory preset current is 30 mA per LED.

When PWM LED current control is first enabled (at cold start, for example), the LDS8866's V_{IN} , V_{OUT} , and V_{PCR} monitors cause the LDS8866's charge pump to cycle through all four operating modes (if necessary) so that V_{OUT} is high enough to maintain regulated LED current. To prevent nuisance switching of the charge pump during this initial start-up sequence, a 0.8ms transition filter is applied at each charge-pump mode. Depending on V_{IN} and the V_F of the LEDs chosen, the maximum cold-start delay to regulated LED current operation can be up to 2.4ms. (See Timing Diagram Figure 3)

Once the LDS8866 reaches steady-state operation, its charge pump remains in operation even when the LED current is turned off (t_{OFF}). As shown in Figure 3, V_{OUT} increases slightly by an amount proportional to the voltage drop generated by charge pump's R_{OUT} and the total LED current load. The LDS8866's efficiency and LED current regulation are not affected because the LEDs are off during this time.

If the PWM1/PWM2 pins are held high or low longer than 30ms (Time to Shutdown), the LDS8866 turns LEDs off. If PWM1/PWM2 pins are low, shutdown mode is enabled and the supply current drops to 1 μ A or less. If PWM1/PWM2 pins are logic high, the LDS8866 charge pump remains active with an overall quiescent current ~ 1 mA.

Unused LED Channels

For applications with only two or four LEDs, unused LED banks can be disabled via the appropriate PWM pin connected to the ground.

For applications requiring 1, 3, or 5 channels, the unused LED pins should be tied to V_{OUT} (see Figure 4). If LED pin voltage is within 1 V of V_{OUT} , then the channel is switched off and a 250 μ A test current is placed in the channel to sense when the channel moves below $V_{OUT} - 1.5$ V.

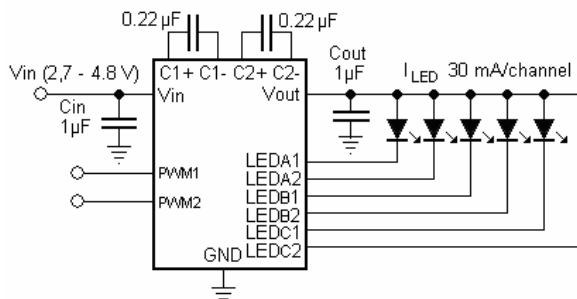


Figure 4. Application circuit with 5 LEDs

Protection Modes

The LDS8866 has follow protection modes

1. LED short to V_{OUT} protection

If LED pin is shorted to V_{OUT} , LED burned out becomes as short circuit, or LED pin voltage is within from V_{OUT} to $(V_{OUT} - 1.5V)$ range, LDS8866 recognizes this condition as "LED Short" and disables this channel. If LED pin voltage is less than $(V_{out} - 1.5V)$, LDS8866 restores LED current at this particular channel to programmed value.

2. V_{OUT} Over-Voltage Protection

The charge pump' output voltage V_{OUT} automatically limits at about 6.2 V maximum. This is to prevent the output pin from exceeding its absolute maximum rating.

3. V_{OUT} Short Circuit Protection

If V_{OUT} is shorted to ground before LDS8866 is enabled, input current may increase up to 200 – 300 mA within 20 μ s after enable and is limited to 35 – 40 mA after that.

4. Over-Temperature Protection

If the die temperature exceeds +150°C, the driver will enter shutdown mode. The LDS8866 requires restart after die temperature falls below 130°C.

5. Input Voltage Under-Voltage Lockout

If V_{IN} falls below 2.2 V (typical value), LDS8866 enters shutdown mode. Device requires restart when input voltage rises above 2.3 V.

6. Low V_{IN} or High LED V_F Voltage Detection

If, in 2-x mode, V_{IN} is too low to maintain regulated LED current for given LED V_F , or LED becomes an open circuit, or if any LED at active channels is disconnected, LDS8866 starts subsequently changing modes (2-x – 1-x – 1.33-x -1.5-x – 2-x ...) in an attempt to compensate insufficient voltage. As a result, average current at all other channels that are ON may fall below regulated level.

LED Selection

LEDs with forward voltages (V_F) ranging from 1.6 V to 3.6 V may be used. Charge pumps operate in highest efficiency when V_F voltage is close to V_{IN} voltage multiplied by switching mode, i.e. $V_{IN} \times 1$, $V_{IN} \times 1.33$, and so on. If the power source is a Li-ion battery, LEDs with $V_F = 2.7$ V - 3.3 V are recommended to achieve highest efficiency performance and extended operation on a single battery charge.

External Components

The driver requires two external 1 μF ceramic capacitors (X5R or X7R type) for decoupling input, output, and two 0.22 μF ceramic capacitors (X5R or X7R type) for the charge pump. In all charge pump modes, the input current ripple is very low, and an input bypass capacitor of 1 μF is sufficient.

In 1-x mode, the device operates in linear mode and does not introduce switching noise back onto the supply.

Recommended Layout

In charge pump mode, the driver switches internally at a high frequency. It is recommended to minimize trace length to all four capacitors. A ground plane should cover the area under the driver IC as well as the bypass capacitors. Short connection to ground on capacitors C_{in} and C_{out} can be implemented with the use of multiple via. A copper area matching the TQFN exposed pad (TAB) must be connected to the ground plane underneath. The use of multiple via improves the package heat dissipation.

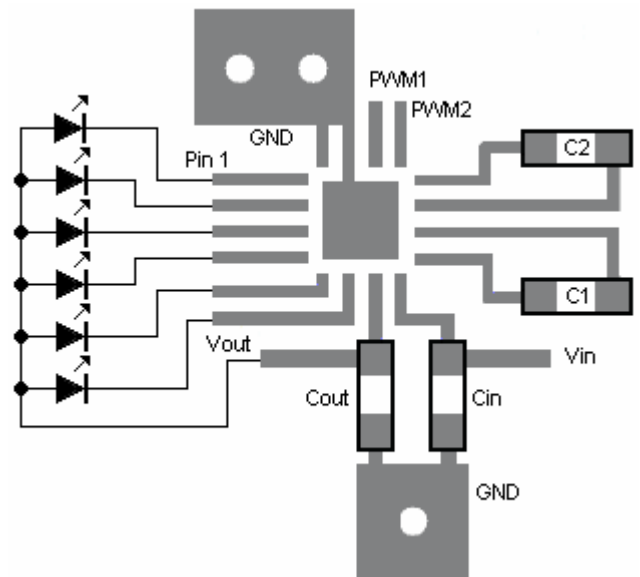
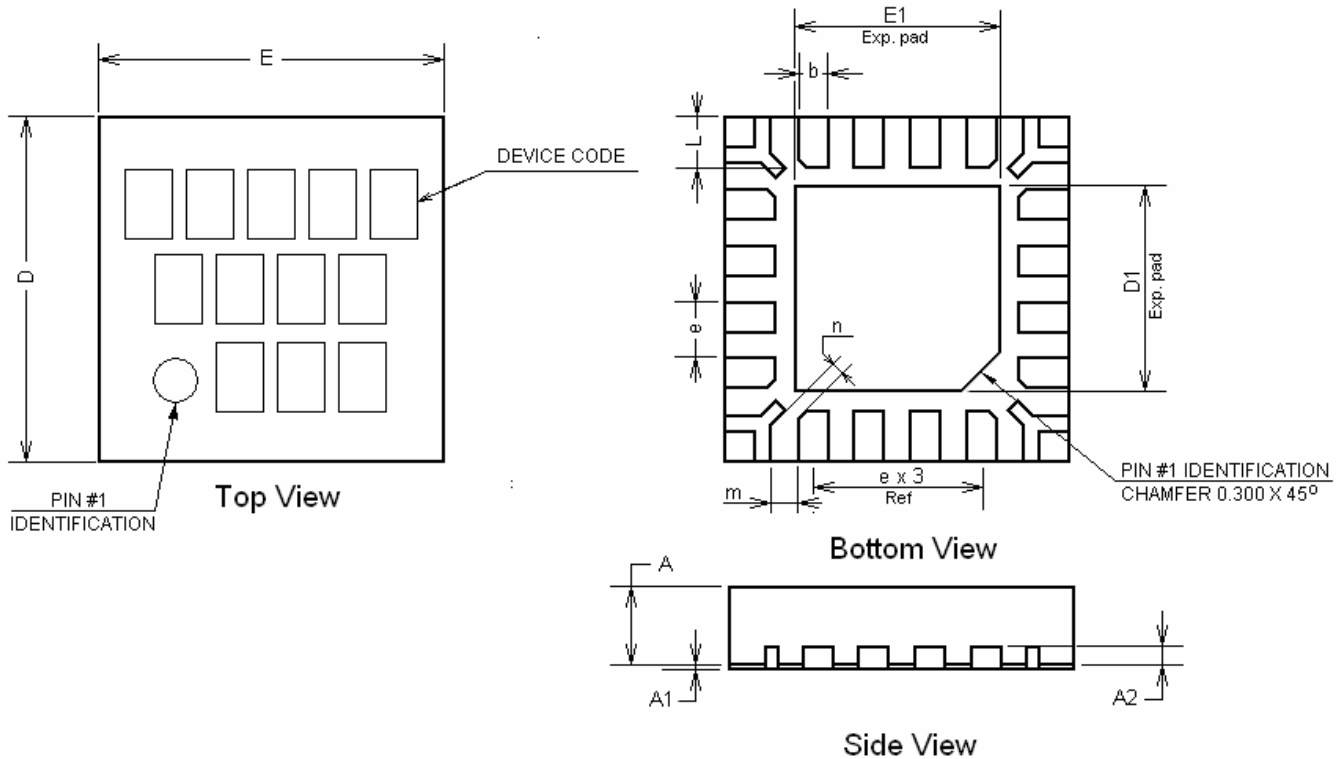


Figure 5. Recommended layout

PACKAGE DRAWING AND DIMENSIONS

16-PIN TQFN (HV3), 3mm x 3mm, 0.5mm PITCH



SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.178	0.203	0.228
b	0.20	0.25	0.30
D	2.95	3.00	3.05
D1	1.65	1.70	1.75
E	2.95	3.00	3.05
E1	1.65	1.70	1.75
e		0.50 typ	
L	0.325	0.375	0.425
m		0.150 typ	
n		0.225 typ	

Note:

1. All dimensions are in millimeters
2. Complies with JEDEC Standard MO-220

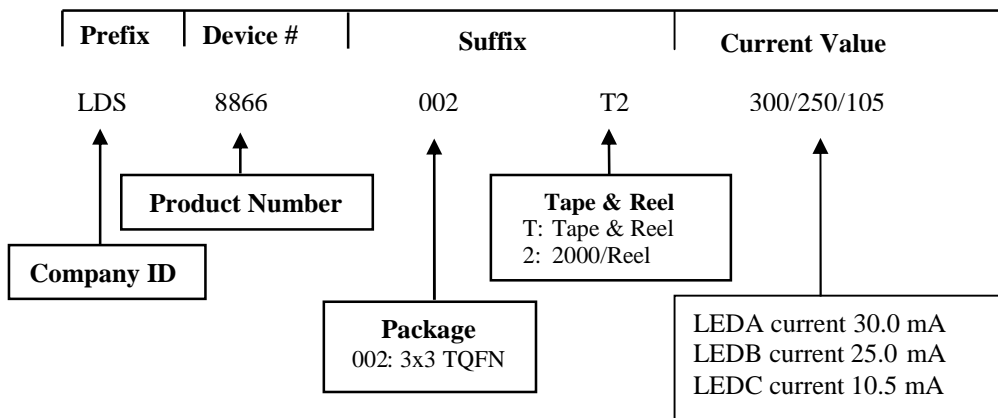
ORDERING INFORMATION

Part Number	Package	Package Marking
LDS8866 002 -T2 300/300/300	TQFN-16 3 x 3mm	8866

Notes:

1. Matte-Tin Plated Finish (RoHS-compliant)
2. Quantity per reel is 2000

EXAMPLE OF ORDERING INFORMATION



Notes:

- 1) All packages are RoHS-compliant (Lead-free, Halogen-free).
- 2) The standard lead finish is Matte-Tin.
- 3) The device used in the above example is a LDS8866 002-T2 (3x3 TQFN, Tape & Reel, 30/25/5 mA maximum current per LED bank).
- 4) For additional package and temperature options, please contact your nearest IXYS Corp. Sales office.

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Document No: 8866DS
Revision: N2.0
Issue date: 10/7/2009