Six Output Programmable LED Current Sink

PRODUCTION DATA SHEET

DESCRIPTION

LED Display Driver: This six channel current sink driver is ideal for controlling brightness and hue of high quality dimmable LED displays. High accuracy, dual mode dimming, and controlled current switching time provides consistent color hue, at brightness ratios of up to 1000:1, and keeps electro magnetic emissions in check.

Its wide compliance voltage range combined with 43 volt breakdown capability make the LX1991 ideal for automotive in-dash displays.

Precision current control: Precision current mirror circuitry sets all channels to the same current with a single programming input. Sinking current value can be programmed up to 30 mA per channel with a single resistor or potentiometer from I_{SET+} to I_{SET-}. Channel to channel matching is typically within ±1 percent of channel mean at the rated output current.

Dual Mode Dimming: Display dimming can be achieved by controlling either current amplitude or duty cycle, and both methods can be employed at the same time.

1000:1 Dimming Range: The DIG_DIM input accepts a TTL or CMOS logic signal that controls duty cycle of the output currents.

Independent Channels: The six channels feature independent regulation with respect to output voltage, so one does not affect the others. Any one or more outputs can be left unloaded without affecting current regulation of the other channels. Multiple channels can also be connected together to sink more current in a single load.

EMI Control: Rise and fall time of sink currents are precisely controlled by placing a capacitor on the SLOPE_C pin. Special control circuitry maintains symmetrical rise and fall times, preserving the LX1991's ability to provide accurate output current response to very narrow input pulses on the DIG_DIM pin.

Power Handling: The LX1991 is supplied in a 4x4 MLPQ package capable of 1.5 watts dissipation. Logic Enable: A separate input puts the LX1991 to sleep at less than 1 uA I_{DD}.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

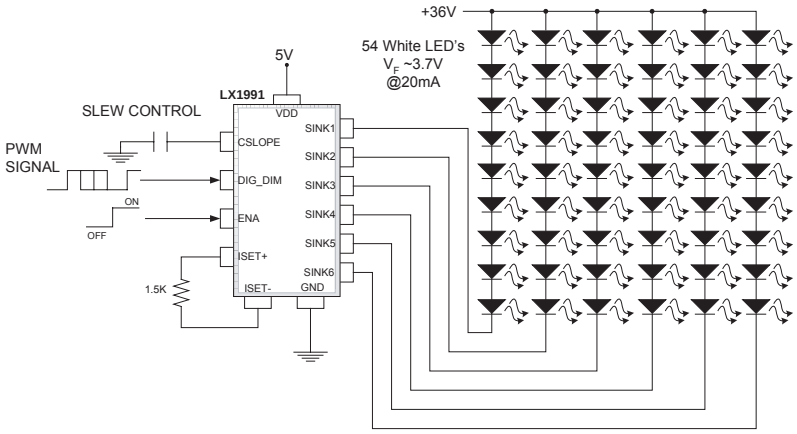
KEY FEATURES

- Six precision independent current sink channels
- Simultaneous Analog and Digital Dimming Modes
- Precision programming of current rise & fall times
- 1% band gap reference
- 40 volt rated output stages
- 3V / 5V logic input compatible
- 1.5 watt power dissipation
- On-chip thermal shutdown
- 16 Pin 4 x 4 MLPQ Package

BENEFITS

- Consistent LED color hue results from high current accuracy
- 1000:1 dimming ratio with digital dimming
- Lowered emissions with current slope programming
- Reduced component count for compact designs
- Drive up to 108 colored LED's per IC (6 x 18 @ 2.1 volts)
- Drive up to 60 white or blue LED's per IC (6 x 10 @ 3.8 volts)

PRODUCT HIGHLIGHT



Bill of Materials	
1	LX1991
1	Cap
1	Resistor
54	White LEDs
57	Total Count

PACKAGE ORDER INFO

T_J (°C)	MIN V_{DD}	MAX V_{DD}	LQ: Plastic 4x4 MLPQ 16-PIN RoHS Compliant / Pb-free Transition DC: 0436
-40 to 85	4.5	5.5V	**LX1991ILQ**

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX1991ILQ-TR)

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VDD) ..... -0.3v to 6V
Analog Output Voltage ($SINK_1$ to $SINK_6$)..... -0.3V to 43V
Analog Inputs (I_{SET}).....-0.3V to VDD +0.5V
Digital Inputs (ENABLE, DIG_DIM) .....-0.3V to VDD +0.5V
Operating Temperature Range.....-40°C – 85°C
Storage Temperature Range.....-65°C – 150°C
Maximum Junction Temperature..... 150°C
Peak Package Solder Reflow Temp. (40 seconds max. exposure)..... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

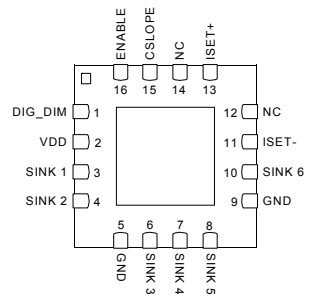
THERMAL DATA

LQ **Plastic 4x4 MLPQ 16-Pin**

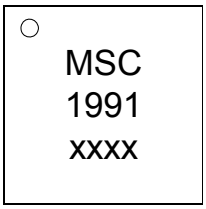
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JC}	2.2°C/W
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	36°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/ 4 layer pc-board system. All of the above assume no ambient airflow.
The θ_{JA} numbers are to MIL-STD-883D Method 1012.1

PACKAGE PIN OUT



LQ PACKAGE
(Top View)



LQ PACKAGE MARKING
xxxx Denotes Date Code / Lot Code

RoHS / Pb-free 100% Matte Tin Lead Finish

FUNCTIONAL PIN DESCRIPTION

PIN NAME	DESCRIPTION
GND	Ground
V_{DD}	Voltage Input, 4.5 to 5.5V input range. V_{DD} is internally switched (see ENABLE) to remove power from chip.
$SINK_1$ – $SINK_6$	Current sink channels one through six. Each output sinks the programmed current from the V_{LED} supply to ground. Compliance voltage is from 1 volt minimum to the V_{LED} supply maximum.
DIG_DIM	A logic input that duty cycle modulates the output currents. All output currents are turned on at the programmed current value when DIG_DIM is high and turned off when it is low. Compatible with both 3V and 5V logic.
ENABLE	Chip Enable Input. If logic high, all functions are enabled. If logic low, internal power is disconnected from the V_{DD} pin, disabling all functions. Logic threshold is 1.6 ± 0.8V maximum over supply and temperature range. Maximum current into VDD when ENABLE < 0.4V is 1 µA .
I_{SET+} I_{SET-}	Current programming resistor pins. Output current in each channel is 24 times the current that flows from I_{SET+} to I_{SET-}. I_{SET} current is 1.26V / R_{SET}. Connect resistor between I_{SET+} and I_{SET-}
C_{SLOPE}	Current rise and fall time programming capacitor. Rise and fall times increase in direct proportion to capacitor value. C = 450µA * T_R or T_F in microseconds, C in picofarads.

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RECOMMENDED OPERATING CONDITIONS

Parameter	LX1991			Units
	Min	Typ	Max	
Supply Voltage (V_{DD})	4.5		5.5	V
ENABLE Input Voltage	0		V_{DD}	V
DIG_DIM Input Voltage	0		V_{DD}	V
C_{SLOPE} Capacitance Range				
I_{SET} Voltage	0		1.26	V
R_{SET} Current Programming Resistor Range	1		40	KΩ
$SINK_1$ To $SINK_6$ Output Voltage Range	0.5	3	40*	V
$SINK_1$ To $SINK_6$ Maximum Output Current			30	mA

*At output voltages greater than 5V total power dissipation when using all six outputs at maximum current will exceed power rating of package and ambient of 85°C.

SIMPLIFIED BLOCK DIAGRAM

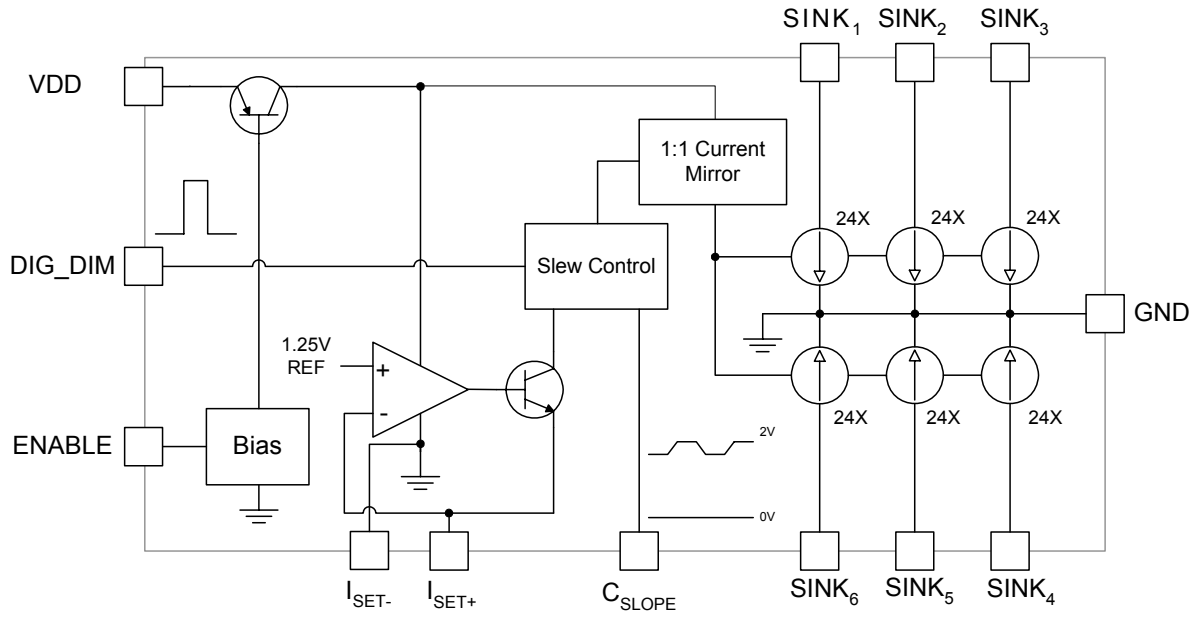

Figure 1 – Simplified Block Diagram

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature –40°C <TA < 85°C except where otherwise noted and with the following test conditions: V_{DD} = 4.5 to 5.5 V_{DC}, R_{SET} = 1.54KΩ, $SINK_X$ = 3V, DIG_DIM = 2.4V. Typical values are at T_A= 25°C

Parameter	Symbol	Test Conditions	LX1991			Units
			Min	Typ	Max	
POWER						
Power Supply Input Voltage	V_{DD}		4.5	5	5.5	V
Quiescent current	$I_{DD\ ON}$	VDD = 5V, ENABLE ≥ 2.4V; DIG_DIM ≥ 2.4V		10	16	mA
Quiescent current	$I_{DD\ OFF}$	VDD = 5V, ENABLE ≥ 2.4V; DIG_DIM ≤ 0.8V		3.6	6	mA
Sleep Current[1]	I_{DD_SLEEP}	VDD = 5V, V_{OUT} = 40V, ENABLE ≤ 0.4V		0.08	1	µA
ENABLE INPUT						
ENABLE Logic Threshold	V_{TH_EN}		0.8	1.6	2.4	V
Input Current	$I_{IH\ ENABLE\_}$	V_{ENABLE} = V_{DD}		4.0	10	µA
Input Current	$I_{IL\ ENABLE}$	V_{ENABLE} = 0V		0.4	1	µA
OUTPUT CURRENT						
$SINK_X$ 30mA	$SINK_{30}$	VDD = 5V, $SINK_X$ = 3V, R_{SET} = 1.02KΩ	28.4	30	31.6	mA
$SINK_X$ 20mA	$SINK_{20}$	VDD = 5V, $SINK_X$ = 3V, R_{SET} = 1.54KΩ	19	20	21	mA
$SINK_X$ 10mA	$SINK_{10}$	VDD = 5V, $SINK_X$ = 3V, R_{SET} = 3.09KΩ	9	10	11	mA
$SINK_X$ 5mA	$SINK_{05}$	VDD = 5V, $SINK_X$ = 3V, R_{SET} = 6.19KΩ	4	5	6	mA
$SINK_X$ Current Matching[2]	$SINK_{X\_MATCH}$	VDD = 5V, $SINK_X$ = 1V to 5V; R_{SET} = 1.54KΩ		±1	±2.5	%
I_{SET} to $SINK_X$ Current Ratio	$SINK_{X\_RATIO}$	VDD = 5V, $SINK_X/I_{SET}$		24.5		
Output Current I_{SET} = 0µA	$SINK_{SET0}$	I_{SET} = 0µA		10	100	$µA_{DC}$
Output Current DIG_DIM ≤ 0.8V	$SINK_{DIG\_DIM0}$	R_{SET} = 1.02KΩ; DIG_DIM ≤ 0.8V		10	100	$µA_{DC}$
Dropout Voltage[3]	$V_{DROPOUT}$	$SINK_X$ = 10mA		200	800	mV
Dropout Voltage[3]	$V_{DROPOUT}$	$SINK_X$ = 30mA		600	1000	mV
Maximum Output Current, I_{SET} Shorted To Gnd. Each Output	$SINK_{ISETSC}$	V_{ISET} = Zero Volts; VDD=5V; $SINK_X$ = 5V		50		mA_{DC}
Output Off State Current	$SINK_{X\ OFF}$	ENA ≤ 0.4V, V_{OUT} = 40V		1	3	$µA_{DC}$
DIG_DIM INPUT						
DIG_DIM Logic Threshold	V_{TH_DD}		0.8	1.6	2.4	V
Input Current, high state	$I_{IH\ DIG\_DIM}$	V_{DIG_DINM} = V_{DD}		50		µA
Input Current, low state	$I_{IL\ DIG\_DIM}$	V_{DIG_DIM} = 0V		0.1		µA
DIG_DIM to $SINK_X$ Pulse Response	$T_{D(ON)}$	C_{SLOPE} ≤ 20pF		340		nS
DIG_DIM to $SINK_X$ Pulse Response	$T_{D(OFF)}$	C_{SLOPE} ≤ 20pF		230		nS
Minimum $SINK_X$ Pulse Width	$SINK_{X\ PWMMIN}$	C_{SLOPE} ≤ 20pF, DIG_DIM ≤ 5uS		5		µS
CURRENT ON / OFF SLOPE						
Current On rise time	T_{RISE}	C_{SLOPE} = 10 nF	15	22	29	µSec
Current On fall time	T_{FALL}	C_{SLOPE} = 10 nF	15	24	29	µSec
Current on / off delay time	T_{delay}	C_{SLOPE} = 10 nF, T_A = 25°C		50		µSec
RSET PIN						
Voltage at Pin R_{SET}	V_{RSET}	R_{SET+} = 1.50K to I_{SET-}	1.24	1.26	1.28	V
Pin R_{SET} Max Source Current	$I_{MAX\ RSET}$			4.5		mA

[1] At enable voltages greater than 0.4V but less than 0.8V the outputs will remain off but the sleep current may be greater than 1µA.
[2] $SINK_X$ current matching is greatest percentage delta between output currents with respect to the mean, with $V_{SINK\ X}$ both at 1V and 5V and R_{SET} = 1.54KΩ.
[3] Dropout is defined as the $SINK_X$ to GND voltage at which the output current sink drops 10% from the nominal value.

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THEORY OF OPERATION / APPLICATION NOTE

FUNCTIONAL DESCRIPTION

The LX1991 is designed to drive LED's used in display illumination and signaling applications such as cellular telephones, PDA's automotive dashboard lighting, panel illumination etc. With a single 5V supply, the six independently regulated constant current outputs can drive 6 white LED's (V_F < 4.0V), or 12 green or amber LED's (V_F < 2.0V each) arranged as 6 parallel x 2 in series. With a separate high voltage LED supply (up to 40V) a large matrix of LED's (>100) can be driven.

The LX1991 features resistor settable output current. Connecting a resistor between I_{SET+} and I_{SET-} pins generates a current that is mirrored into each of the outputs with a gain ratio of about 24. This ratio remains linear for output currents from 3 to 30mA, at output current less than 3mA the ratio increases somewhat. Output current can be varied in an analog fashion by varying R_{SET} resistor, typically this resistor shall be chosen in the range of 1K to 40K.

Duty cycle dimming with a fixed current amplitude is accomplished by driving the DIG_DIM input. The switching frequency can exceed 100 KHz, making it practical to use a PWM output channel from popular micro controllers. The upper limit on frequency correlates to the minimum DIG_DIM sink pulse width which is typically about 5µS.

To use the LX1991 at the maximum usable frequency, or minimum pulse width the CSLOPE pin must be open. The CSLOPE pin allows precise control of the sink current rise and fall time. As the value of the CSLOPE capacitor is increased the slope of the rise and fall time will change correspondingly along with some delay to output. Special control circuitry maintains symmetrical rise and fall times, preserving the LX1991's ability to provide accurate output current response to very narrow input pulses on the DIG_DIM pin.

The ENABLE input is TTL compatible with a turn on threshold of about 1.6V with about 150mV of hysteresis. Below 0.8V the chip is disabled and the sink outputs are off. However ENABLE must be driven below 0.4 volts to insure the minimum sleep current from V_{DD} and output off current.

All inputs and outputs are ESD and short circuit protected making the LX1991 an exceptionally robust component. The device also includes thermal shutdown however it is not recommended to short the I_{SET+} and I_{SET-} inputs together while shorting the outputs to 40V as the power dissipation under these conditions is the greatest.

APPLICATION NOTES

POWER CONSIDERATIONS

Each output has an independent current sink, however each must be held above about 600-800mV (typically) to perform properly and maintain the specified current regulation accuracy. The device is designed however to allow one or more of the outputs to be unused (open) without affecting the other channels Or conversely if more than 30mA is needed the outputs can be combined for higher total currents.

Package power dissipation can be calculated from the following equation:

$$P_D = \left(n \times I_{OUT}\right) \times \left(V_{LOAD} - V_{LED}\right)$$

n	=	Number of outputs used
I_{OUT}	=	Current from each output
V_{LOAD}	=	Output Supply Voltage
V_{LED}	=	Minimum LED forward voltage
P_D	=	Power Dissipated in mW

Care should be exercised not to exceed the power dissipation of the package or the maximum junction temperature of the die. Proper mounting of the package with thermal vias (see PCB Land Guidelines and Thermal Pad Design section) enhances power dissipation capability. As an example to drive 24 white LED's, 4 per channel from a 18V V_{LED} supply @ 25mA per LED string, we will assume the minimum LED forward voltage to be 3.5V with an maximum operating ambient of 50°C.

$$P_D = (6 \times 25mA) \times (18V - (4 \times 3.5V)) = 15 \times 4V = 0.6W$$

This represents a 21.6°C temperature rise (36°C/W *0.6W) for a die temperature of about 72°C, ignoring device drain current power dissipation that only represents about a 3°C rise worst case. This is well under the die junction temperature maximum rating of 150°C, and within the 85°C electrical specifications.

DIMMING

Dimming can be accomplished both with current amplitude control (changing the R_{SET} resistor value) with a PWM signal (toggling the DIG_DIM input) or both. Current between the I_{SET+} and I_{SET-} pins may be varied for current amplitude dimming. If a mechanical input is needed, a rheostat in series with a resistor connected from I_{SET+} to I_{SET-} can be used.:

$$I_{OUT} = \text{Current Ratio} \times I_{SET}$$

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APPLICATION NOTE – CONTINUED

The range of the R_{SET} resistor can vary between 1K and 40K Ohms. The resistor in series with the rheostat will set the maximum current and should be a least 1KΩ in value. If a fixed sink current is desired its easy to find the RSET resistor value. As an example, suppose the desired output current is 25mA per sink channel. The R_{SET} resistor can be calculated as follows:

$$R_{SET(K\Omega)} = \text{Current ratio} \,/\, \text{Output current(mA)} \times VR_{SET}$$

$$R_{SET(K\Omega)} = 24.5 \,/\, 25 \times 1.26 = 1.23K\Omega$$

Once the maximum sink current is set the rheostat will increase the RSET value thus dimming the LED by reducing the sinking current.

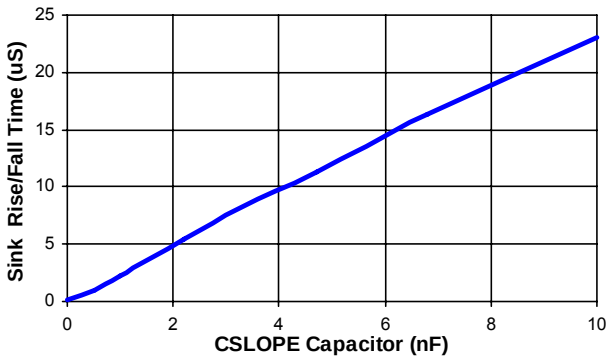
Wide range dimming can be accomplished by using the DIG_DIM input pin to pulse the output sink current. The DIG_DIM pin may be driven with a TTL compatible logic PWM signal to dim the LED's. The recommended PWM frequency for dimming is between 100 Hz and 100 KHz. Below 100 Hz flicker may be observed. Above 100 KHz duty cycle accuracy and minimum pulse width is reduced due to delay times and the current slew rate. To obtain the maximum dim range and still make use of the slope control function (see CSLOPE pin below) it is advisable to use a lower frequency on the DIG_DIM input.

If PWM dimming is used, use of separate power and ground lines directly from the power source point will help to prevent noise generated from the LED current transients from entering video or audio subsystems on the same supply rails. Additional power supply filtering may be needed in PWM dimming applications. Care should be exercised in the PCB layout to prevent coupling from the SINK outputs to the DIG_DIM pin.

CSLOPE PIN

The CSLOPE pin is available to control the rise and fall times of the SINK outputs during pulse dimming. With the CSLOPE pin open a minimum rise and fall time of about 120 to 200nS will be present on the output waveforms along with a delay time (DIG_DIM to SINKx) of about 200nS. As the CSLOPE capacitor is increases in value so will the corresponding rise and fall times and delay to output. The calculation for the CSLOPE value is approximately 450µA * T_R or T_F in microseconds, C in picofarads. So for a 5uS rise and fall time 0.00045 * 5 = 2250pF or about a typical .0022uF capacitor value. For typical slope rise and fall times see the follow chart

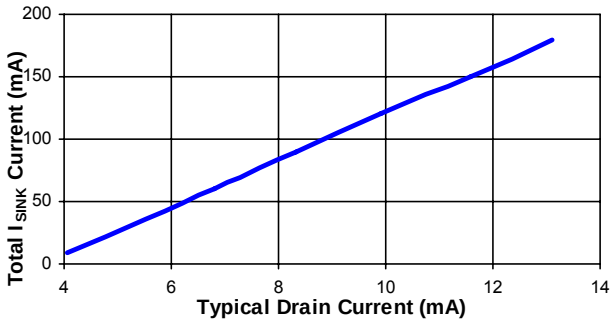
Typical CSLOPE vs Slope Times



DRAIN CURRENT

The chart below illustrates the correlation between the IC's drain current and the total sink output current. The drain current will also increase slightly if one or more the SINKx pins are left floating or when the SINK outputs are near dropout, however in both of these circumstances the increased drain current will be small and controlled and is a feature of the design.

LX1991 Typical Drain Current Vs Sink Current



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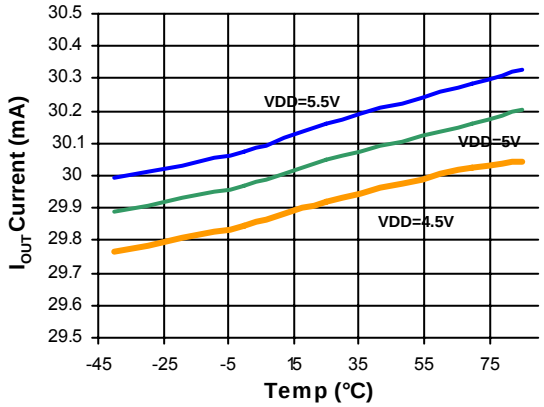
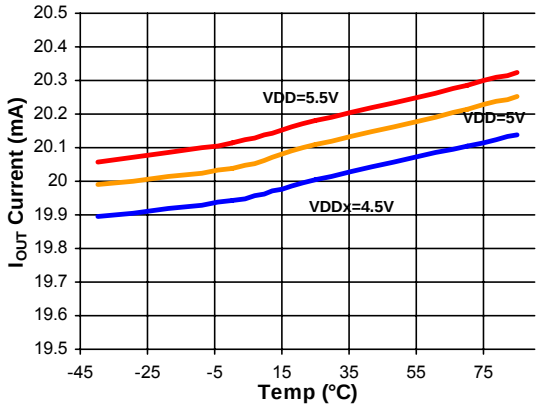
ISINK VS VDD AND TEMPERATURE



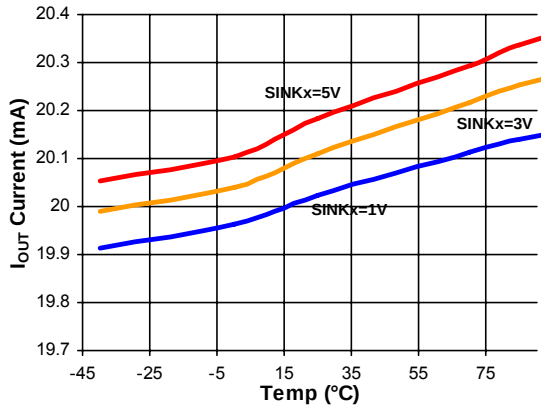
$SINK_X$ = 3V; R_{SET} = 1.02KΩ

ISINK VS VDD AND TEMPERATURE



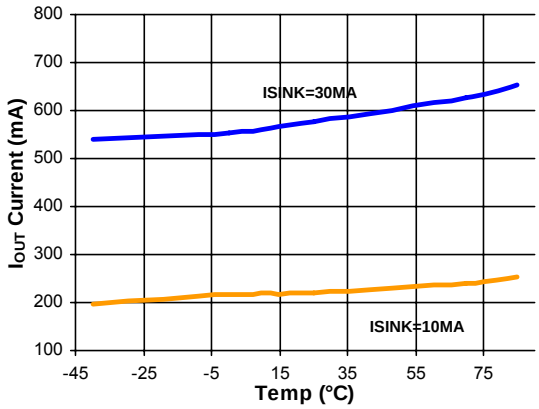
VDD = 5V, R_{SET} = 1.54KΩ

ISINK VS VSINK AND TEMPERATURE



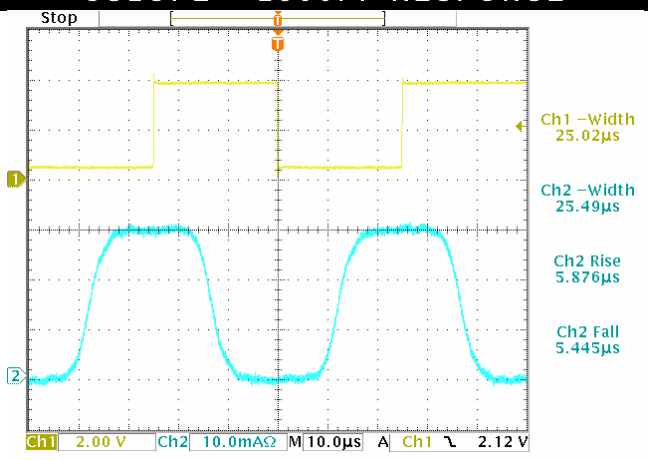
VDD = 5V, R_{SET} = 1.54KΩ

DROPOUT VS TEMPERATURE



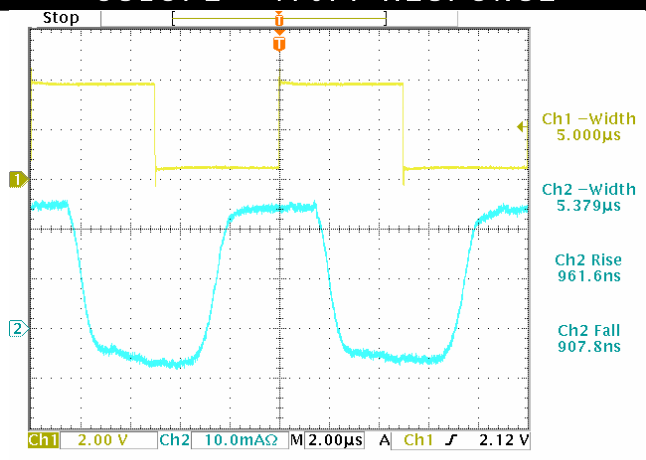
Load = 10kΩ and 1µF
Photo Step = Direct Light Input of 14.6µW/cm^2

CSLOPE = 2500PF RESPONSE



VDD=5V ,CSLOPE = 2500pF, Chan 1 = 20Khz DIG_DIM
Channel 2 = $SINK_X$ = 10mA/DIV, Load = single white LED

CSLOPE = 470PF RESPONSE



VDD=5V, CSLOPE = 470pF, Chan 1 = 100Khz DIG_DIM
Channel 2 = $SINK_X$ = 10mA/DIV, Load = single white LED per channel

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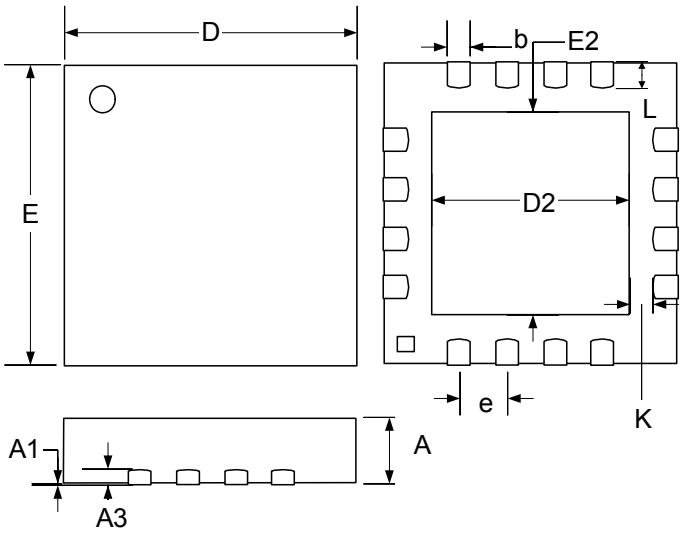
MECHANICAL DRAWING

LQ 16-Pin MLPQ Plastic (4x4mm EP)

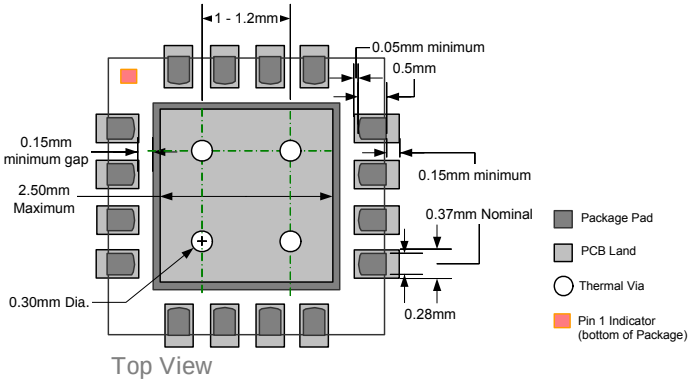


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.80	1.00	0.031	0.039
A1	0	0.05	0	0.002
A3	0.18	0.30	0.007	0.012
b	0.23	0.38	0.009	0.015
D	4.00 BSC		0.157 BSC	
E	4.00 BSC		0.157 BSC	
e	0.65 BSC		0.026 BSC	
D2	2.55	2.80	0.100	0.110
E2	2.55	2.80	0.100	0.110
K	0.20	-	0.008	
L	0.30	0.50	0.012	0.020

Note:

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.

LQ 16-Pin PCB Land Guidelines and Thermal Pad Design



The typical land pattern shown includes thermal vias in the exposed die attach pad for improved thermal performance. Vias should be about 0.3mm in diameter, with the via plated to about 1.0 ounce copper. Vias should be plugged to prevent voids being formed due to capillary action. This can be avoided by tenting the via during the solder mask process. In addition, to reduce solder paste volume on the thermal land, it is recommended that an array of small apertures in the solder mask be used instead of one large aperture, with the goal of 50 – 80% solder paste coverage. Please review IPC / EIA J-Std-001C Section 9.2.6.4 "Bottom Only Termination" for solder joint requirements.

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NOTES