10.709 Gbps Laser Diode Driver Chipset

ADN2843

FEATURES

Data Rates from 9.952 Gbps to 10.709 Gbps
Typical Rise/Fall Time 25 ps/23 ps
Bias Current Range 3 mA to 80 mA
Modulation Current Range 5 mA to 80 mA
Monitor Photodiode Current 50 μA to 1200 μA
Closed-Loop Control of Both Average Optical Power and Extinction Ratio
Laser Fail and Laser Degrade Alarms
Automatic Laser Shutdown, ALS
Dual MPD Functionality for Wavelength Control
CML Data Inputs
50 Ω Internal Data Terminations
3.3 V Single-Supply Operation
Driver Supplied in Dice Format

APPLICATIONS

SONET OC-192, SDH STM-64
Supports 10.667 Gbps and 10.709 Gbps FEC Rates
10 Gb Ethernet IEEE802.3ae

GENERAL DESCRIPTION

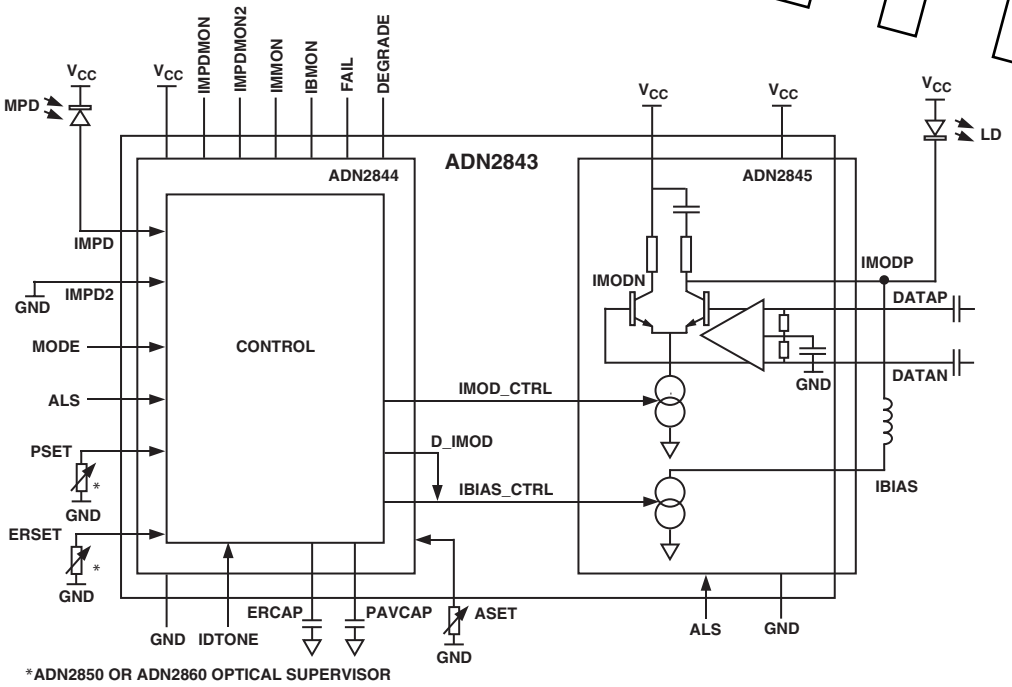
The ADN2943 chipset consists of two components, the ADN2845 and the ADN2844. The ADN2845 is a 10.709 Gbps laser diode driver. The ADN2845 eliminates the need to ac couple since it can deliver 80 mA of modulation while dc coupled to the laser diode. It is intended to be copackaged with the laser to minimize bond lengths, which improves performance of the optical transmitter. For transmission line applications, contact HSN Application Group at fiberoptic.ic@analog.com.

The ADN2844 offers a unique control loop algorithm and provides dual loop control of both average power and extinction ratio.

Programmable alarms are provided for laser fail (end of life) and laser degrade (impending fail).

Both the ADN2844 and the ADN2845 are available as bare die. The ADN2844 is also available in 5 mm × 5 mm 32-lead LFCSP.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADN2843–SPECIFICATIONS

(V_{CC} = 3.0 V to 3.6 V, All specifications T_{MIN} to T_{MAX}, unless otherwise noted. Typical values as specified at 25°C.)

Parameter	Min	Typ	Max	Unit	Conditions
LASER BIAS (BIAS)					
Output Current I_{BIAS}	3		80	mA	
Compliance Voltage	1.2		V_{CC} – 1.0	V	
I_{BIAS} during ALS			10	µA	See Note 1
ALS Shutdown Response Time			10	µs	
MODULATION CURRENT (IMODP, IMODN)					See Note 2
Output Current I_{MOD}	5		80	mA	
Compliance Voltage	1.2		V_{CC}	V	
I_{MOD} during ALS			10	µA	
Rise Time		25		ps	
Fall Time		23		ps	
Random Jitter		170		fs rms	See Note 3
Total Jitter		7.41		ps p-p	See Note 4
POWER SET INPUT (PSET)					
External Capacitance			80	pF	See Note 5
Voltage	1.15		1.35	V	
EXTINCTION RATIO SET INPUT (ERSET)					
Allowable Resistance Range	1.5		25	kΩ	
Voltage	1.15		1.35	V	
ALARM SET (ASET)					
Allowable Resistance Range	1.2		13.2	kΩ	
Voltage	1.15		1.35	V	
Hysteresis		5		%	
CONTROL LOOP					
Time Constant		0.22		s	
DATA INPUTS (DATAP, DATAN)					
V p-p (Single-Ended Peak-to-Peak)	300		800	mV	
Input Impedance (Single-Ended)		50		Ω	
LOGIC INPUTS (ALS, MODE)					
V_{IH}	2.4			V	
V_{IL}			0.8	V	
ALARM OUTPUTS (Internal 30 k to V_{CC})					
V_{OH}	2.4			V	
V_{OL}			0.4	V	
IDTONE					
f_{IN}	10		1000	kHz	
Input Current Range	50		4000	µA	
Voltage on IDTONE	V_{CC} – 2			V	
MONITOR PD (MPD, MPD2)					
Current	50		1200	µA	
Input Voltage			1.65	V	
IBMON, IMMON, IMPDMON, IMPDMON2					
IBMON, IMMON Division Ratio		100		A/A	
IMPDMON, IMPDMON2		1		A/A	
IMPDMON to IMPDMON2 Matching			2	%	Measured at 1200 µA
Compliance Voltage	0		V_{CC} – 1.5	V	
SUPPLY					
V_{CC}	3.0	3.3	3.6	V	
I_{CC} (ADN2844)			36	mA	See Note 6
I_{CC} (ADN2845)		75		mA	See Note 6

NOTES

[1]In ALS mode current is sourced to the laser from the I_{BIAS} pin, which reverse biases the laser.

[2]The ADN2845 high speed specifications are measured into a 5 Ω load.

[3]RMS jitter measured with a 0000 0000 1111 1111 repeating pattern at 10.7 Gbps rate.

[4]Peak-to-peak total jitter measured with a 2^{13} – 1 PRBS with 80 CIDs pattern at 10.7 Gbps rate.

[5]Max capacitance refers to capacitance of photodiode and other parasitic capacitance.

[6]I_{BIAS} = 0, I_{MOD} = 0 (when ALS is asserted). See Power Dissipation section on page 7 for calculation of complete power dissipation.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

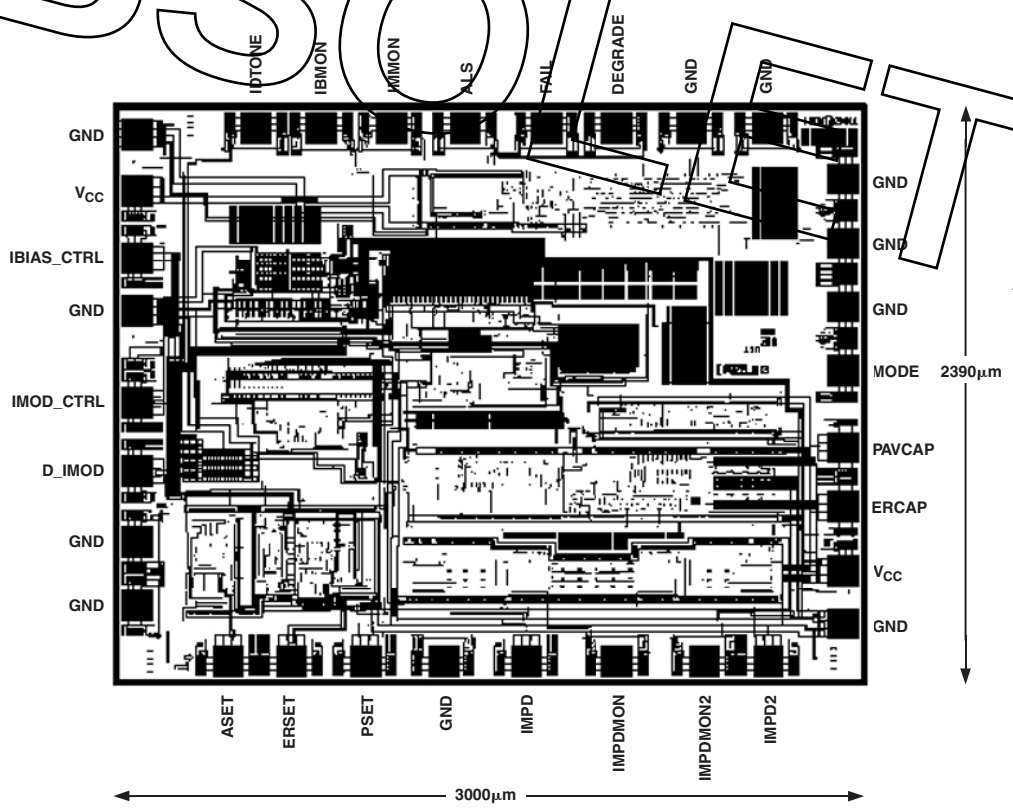
V_{CC} to GND . . . . . 4.2 V
Digital Inputs (ALS, MODE) . . . . . –0.5 V to V_{CC} + 0.3 V
IMODN, IMODP . . . . . V_{CC} + 1.2 V
MOD_CONTROL to GND . . . . . –0.5 V to 4.2 V
IBIAS_CONTROL to GND . . . . . –0.5 V to 4.2 V
D_MOD to GND . . . . . –0.5 V to 4.2 V
DATAP to GND . . . . . –0.5 V to 4.2 V
DATAN to GND . . . . . –0.5 V to 4.2 V
Operating Temperature Range
Industrial . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature (T_J Max) . . . . . 150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Option
ADN2843CHIPSET	–40°C to +85°C	ADN2844 Control Loop: 32-Lead LFCSP ADN2845 Data Switch: Dice
ADN2843CHIPSET-B	–40°C to +85°C	ADN2844 Control Loop: Dice ADN2845 Data Switch: Dice
EVAL-ADN2843		Evaluation Board

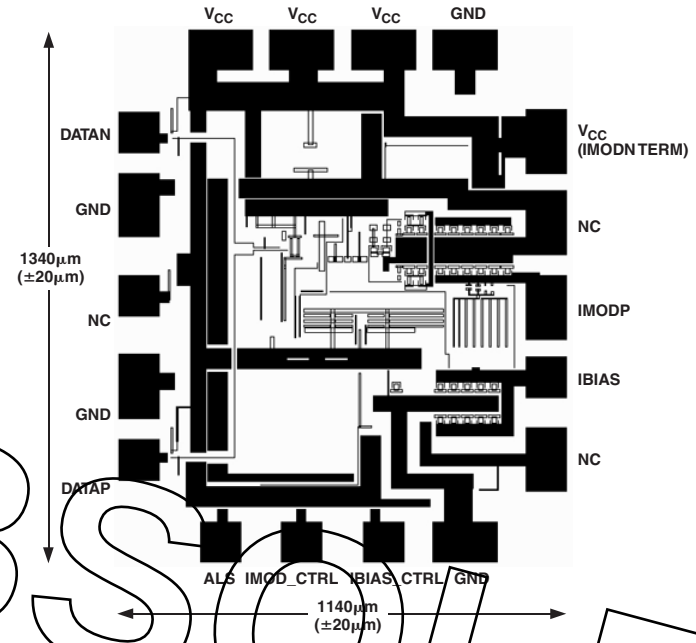
ADN2844 METALLIZATION PHOTOGRAPH



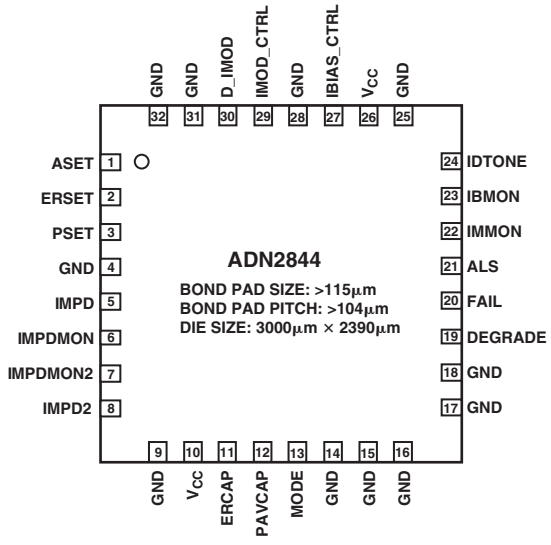
CAUTION

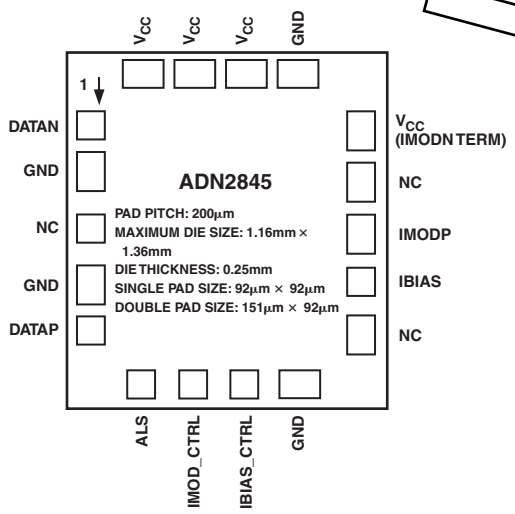
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADN2843 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ADN2845 METALLIZATION PHOTOGRAPH



PIN CONFIGURATIONS





ADN2844 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	ASET	Alarm Current Threshold Set (Should be Terminated with a 1.2 kΩ Resistor when Not Used)
2	ERSET	Extinction Ratio Current Set
3	PSET	Average Optical Power Set
4	GND	Negative Supply
5	IMPD	Monitor Photodiode Current Input (Tie to GND when Not in Use)
6	IMPDMON	Mirrored Current from IMPD (Tie to V_{CC} when Not in Use)
7	IMPDMON2	Mirrored Current from IMPD2 (For Optional Use with Two MPDs, Tie to V_{CC} when Not in Use)
8	IMPD2	Optional Second MPD Current Input (Tie to GND when Not in Use)
9	GND	Negative Supply
10	V_{CC}	Positive Supply
11	ERCAP	Extinction Ratio Loop Capacitor
12	PAVCAP	Average Power Loop Capacitor
13	MODE	Control Loop Operating Mode Logic Input (Should Not Be Left Floating)
14, 15, 17	GND	Negative Supply
18, 31, 32	GND	Negative Supply
16	GND	Negative Supply
19	DEGRADE	DEGRADE Alarm Output, Open Collector, Active High
20	FAIL	FAIL Alarm Output, Open Collector, Active High
21	ALS	Automatic Laser Shutdown Logic Input (Should Not Be Left Floating)
22	IMMON	Modulation Current Mirror Output, Current Source from V_{CC}
23	IBMON	Bias Current Mirror Output, Current Source from V_{CC}
24	IDTONE	ID Tone Input Current (Tie to V_{CC} when Not in Use)
25	GND	Negative Supply
26	V_{CC}	Positive Supply
27	IBIAS_CTRL	Control Output Current Sink
28	GND	Negative Supply
29	IMOD_CTRL	Control Output Current Sink
30	D_IMOD	Control Output Current Sink

ADN2845 PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	DATAN	AC-Coupled CML Data, Negative Differential Terminal
2	GND	Negative Supply
3, 13	NC	No Connect, Leave Floating
4	GND	Negative Supply
5	DATAP	AC-Coupled CML Data, Positive Differential Terminal
6	ALS	Automatic Laser Shutdown Logic Input
7	IMOD_CTRL	Modulation Current Control Input (Control Circuit Sinks IMOD/10 from Pin to GND)
8	IBIAS_CTRL	BIAS Current Control Input (Control Circuit Sinks IBIAS/10 from Pin to GND)
9	GND	Negative Supply
10	NC	No Connect, Leave Floating
11	IBIAS	BIAS Current
12	IMODP	Modulation Current
14	V_{CC}	V_{CC} Connection for IMODN Termination Resistor
15	GND	Negative Supply
16–18	V_{CC}	Positive Supply

GENERAL

Laser diodes have current-in to light-out transfer functions as shown in Figure 1. Two key characteristics of this transfer function are the threshold current, I_{TH}, and slope in the linear region beyond the threshold current, referred to as the slope efficiency, LI.

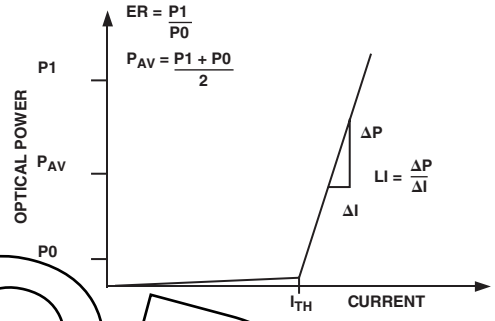


Figure 1. Laser Transfer Function

CONTROL

A monitor photodiode, MPD, is required to control the LD. The MPD current is fed into the ADN2843 to control the power and extinction ratio, continuously adjusting the bias current and modulation current in response to the laser's changing threshold current and light-to-current slope efficiency.

The ADN2843 uses automatic power control, APC, to maintain a constant average power over time and temperature.

The ADN2843 uses closed-loop extinction ratio control to allow optimum setting of the extinction ratio for every device. Thus, SONET/SDH interface standards can be met over device variation, temperature, and laser aging. Closed-loop modulation control eliminates the need to either overmodulate the LD or include external components for temperature compensation, thus reducing research and development time and second sourcing issues.

The ADN2843 dual-loop control has two modes of operation. Each mode is given by the configuration of the MODE and D_IMOD pins as shown below.

Operation Mode	MODE Pin Setting	D_IMOD Pin Connected to
A	HIGH	IBIAS
B	LOW	IBIAS_CTRL

Configuring the ADN2843 in Mode A or Mode B (see Figures 3 and 4) enables users to achieve accurate control of the extinction ratio. Mode B is suitable for applications where an IBIAS pin is not available to the TOSA, or where there is no space on the TOSA for an IBIAS inductor. Experimental data and simulation for typical lasers has shown ER to be 0.3 dB to 0.5 dB better in Mode A, at a 5 dB extinction ratio. Care should be taken to ensure that the extra capacitance on the I_{BIAS} pin due to the D_IMOD connection does not degrade the eye quality. When physical constraints do not allow a low capacitance interconnect between D_IMOD and I_{BIAS}, the ADN2843 should be configured in Mode B (see Figure 4).

Average power and extinction ratio for both modes are set using the PSET and ERSET pins, respectively. Potentiometers are connected between these pins and ground. The potentiometer R_{PSET} is used to set the average power. The potentiometer R_{ERSET} is used to set the extinction ratio. The internal control loops force the PSET and ERSET pins to 1.23 V above GND. For initial setup, R_{PSET} and R_{ERSET} may be calculated using the following formulas:

The PSET resistor is given by the following formulas:

$$R_{PSET} = \frac{1.23\ V}{I_{AV}}(\Omega)$$

where I_{AV} is average MPD current.

The value of the ERSET resistor is a function of the operation mode of the ADN2843 as follows:

For Mode A:

$$R_{ERSET} = R_{PSET} \times \frac{ER+1}{ER-1}$$

For Mode B:

$$R_{ERSET} = \frac{R_{PSET}}{2} \times \frac{ER+1}{ER-1}$$

Note that I_{ERSET} and I_{PSET} will change from laser diode to laser diode, therefore R_{ERSET} and R_{PSET} need to be adjusted for each laser diode. When tuning the laser diode, R_{PSET} should be adjusted first with R_{ERSET} at 25 kΩ. Once the average power is set, R_{ERSET} is adjusted to set the desired extinction ratio, and R_{PSET} is again adjusted to re-establish the desired average power. Once the values R_{PSET} and R_{ERSET} have been adjusted to set the desired average power and extinction ratio, the control loops maintain these values of average power and extinction ratio over environmental conditions and time.

PAVCAP AND ERCAP

The control loop constants are set by the PAVCAP and ERCAP capacitors. The required value for the PAVCAP and ERCAP capacitors is 22 nF.

The PAVCAP and ERCAP capacitors are connected between the respective pins and GND. The capacitors should be low leakage multilayer ceramic capacitors with an insulation resistance >100 GΩ or an RC >1000 s, whichever is lowest.

ALARMS

The ADN2843 is designed to allow interface compliance to ITU-T-G958 (11/94), Section 10.3.1.1.2 (Transmitter Fail), and Section 10.3.1.1.3 (transmitter degrade). The ADN2843 has two alarms, DEGRADE and FAIL. These alarms are raised when I_{BIAS} exceeds the respective DEGRADE and FAIL thresholds. These alarms are active high. A resistor between ground and the ASET pin is used to set the current at which these alarms are raised. The current through the ASET resistor is a ratio of 1:100 to the FAIL alarm threshold. The DEGRADE alarm will be raised at 90% of the FAIL threshold.

Example:

$$I_{FAIL} = 50\ mA\ so\ I_{DEGRADE} = 45\ mA$$

$$I_{ASET} = \frac{I_{FAIL}}{100} = \frac{50\ mA}{100} = 500\ \mu A$$

$$R_{ASET} = \frac{1.23\ V}{I_{ASET}} = \frac{1.23\ V}{500\ \mu A} = 2.46\ k\Omega$$

The laser degrade alarm, DEGRADE, is provided to give a warning of imminent laser failure if the laser diode degrades further or if environmental conditions continue to stress the LD, such as increasing temperature.

The laser fail alarm, FAIL, is activated when the transmitter can no longer be guaranteed to be SONET/SDH compliant. This occurs when one of the following conditions arise:

- The ASET threshold is reached.
- The ALS pin is set high. This shuts off the modulation and bias currents to the LD, resulting in the MPD current dropping to zero. This gives closed-loop feedback to the system that ALS has been enabled.

  DEGRADE is raised only when the bias current exceeds 90% of the alarm threshold.

ALARM INTERFACE

The alarm voltages are open collector outputs. An internal pull-up resistor of 30kΩ that is used to pull the logic high value to V_{CC}. However, this can be overdriven with an external resistor, allowing alarm interfacing to non-V_{CC} levels. The FAIL output may not be connected directly to the ALS pin to shut down the bias and modulation currents. It can however be latched using a flip-flop, and the output of the flip-flop can then be used to activate ALS. Non-V_{CC} alarm output levels must be below the V_{CC} used for the ADN2843.

DATA INPUTS

Figure 2 shows a simplified schematic of the ADN2845 data inputs. The data inputs are terminated via the equivalent of a 100 Ω internal resistor between DATAN and DATAP. This provides 50 Ω termination for single-ended signals. The actual signal on the switching devices is attenuated by a factor of 2 internally. There is a high impedance circuit to set the common-mode voltage, which is designed to change over temperature. It is recommended that ac coupling be used to eliminate the need for matching between the common-mode voltages.

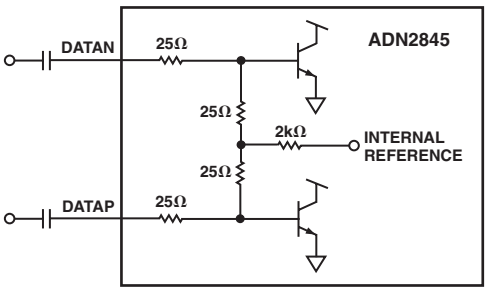


Figure 2. Simplified Schematic of Data Inputs

MONITOR CURRENTS

IBMON, IMMON mirror the bias, modulation current at a ratio of 1:100 for increased monitoring functionality. IMPDMON and IMPDMON2 mirror the current in IMPD and IMPD2, respectively, with a ratio of 1. All monitors source current from V_{CC}.

If the MPD monitoring function is not required, then the IMPD pin should be tied to ground and the monitor photodiode cathode should be connected directly to the PSET pin. When the MPD monitor functions are not used, IMPDMON and IMPDMON2 should be tied to V_{CC}.

MPD CURRENT

The maximum average MPD current is specified in the specifications section. This maximum current specified is limited by the MPD monitoring circuitry. If the monitoring function is not required, then IMPD and IMPD2 should be grounded, the monitor photodiode cathode should be connected directly to the PSET node, and IMPDMON and IMPDMON2 should be tied to V_{CC}. MPD currents as high as 3 mA can be used in this configuration.

Another way to increase the MPD current range without sacrificing the monitoring function is to use IMPD and IMPD2 in parallel. This effectively doubles the current range but raises the lower MPD current specification from 50 μA to 100 μA. If this configuration is used, the IMPDMON and IMPDMON2 pins should be tied together and terminated with a single resistor. The mirror ratio of 1 is maintained in this configuration.

DUAL MPD DWDM FUNCTION

The MPD function mirrors the current in MPD to the PSET pin and to the IMPDMON pin with a ratio of 1. A second monitor photodiode can be connected to the IMPD2 pin. Its current is mirrored to IMPDMON2 and also to the PSET pin, where it is summed with the current mirrored from IMPD. The two MPD monitor currents can be used as inputs to a DWDM wavelength control function when used in combination with various optical filtering techniques. If the IMPD monitor function is not required, the monitor photodiode can be directly connected to the PSET pin, and the IMPD pin must be tied to GND. If the IMPD2 pin is not being used, it should be tied to GND.

IDTONE

The IDTONE pin is supplied for fiber identification/supervisory channels or for control purposes. This pin modulates the optical one level by adding a current to IMOD over a possible range of 2% of minimum I_{MOD} to 10% of maximum I_{MOD}. The IDTONE current is set by an external current sink connected to the IDTONE pin. There is a gain of 2 between the IDTONE pin and the I_{MOD} current. To ratio the IDTONE current to I_{MOD}, the input current can be derived from the IMMON output current.

If the IDTONE function is not being used, this pin must be tied to V_{CC} to properly disable it.

Note that using IDTONE during transmission may cause optical eye degradation.

AUTOMATIC LASER SHUTDOWN (ALS)

The ADN2843 ALS allows compliance to ITU-T-G958 (11/94), Section 9.7. When ALS is asserted, both bias and modulation currents are turned off. In ALS mode, current is sourced to the laser from the I_{BIAS} pin, which reverse biases the laser and ensures that it is turned off. Correct operation of ALS can be confirmed by the FAIL alarm being raised when ALS is asserted. Note this is the only time that DEGRADE will be low while FAIL is high.

Note that for correct ALS operation, the ALS pin on the ADN2845 and ADN2844 should be connected and terminated with a 10 kΩ resistor. The ADN2843 ALS should be driven with correct logic levels (see Specifications section). ALS should never be left floating.

POWER DISSIPATION

The power dissipation of the ADN2845 can be calculated using the following expressions:

$$I_{CC} = 75\,mA + 1.75 \times I_{MOD}(mA) + 0.3 \times I_{BIAS}(mA)$$

$$P = V_{CC} \times I_{CC}\,(A) + V_{IMOD} \times I_{MOD}(A)/2 + V_{IBIAS} \times I_{BIAS}(A)$$

where V_{IMOD} is the average voltage on the IMOD pin, and V_{IBIAS} is the average voltage on the I_{BIAS} pin.

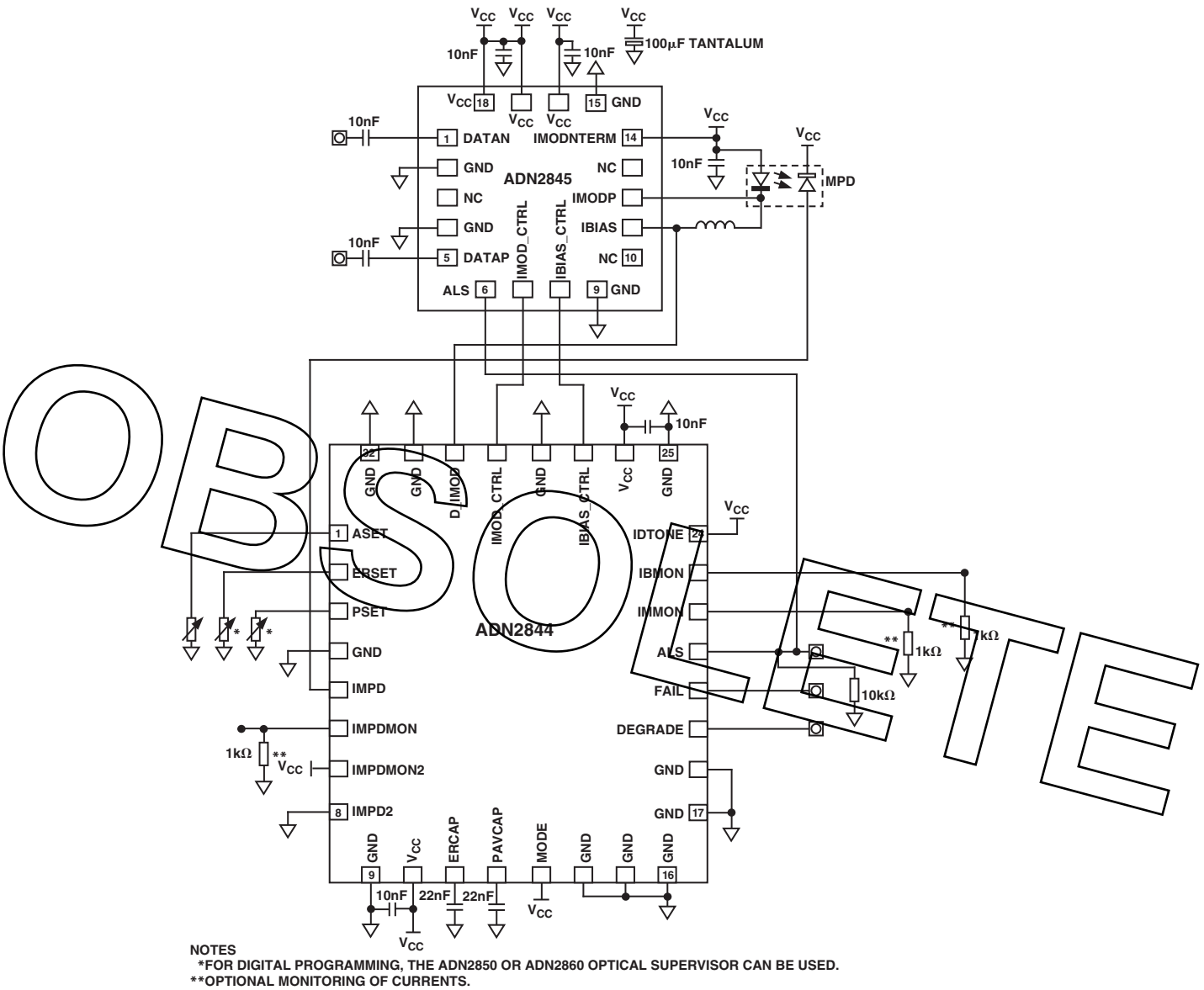
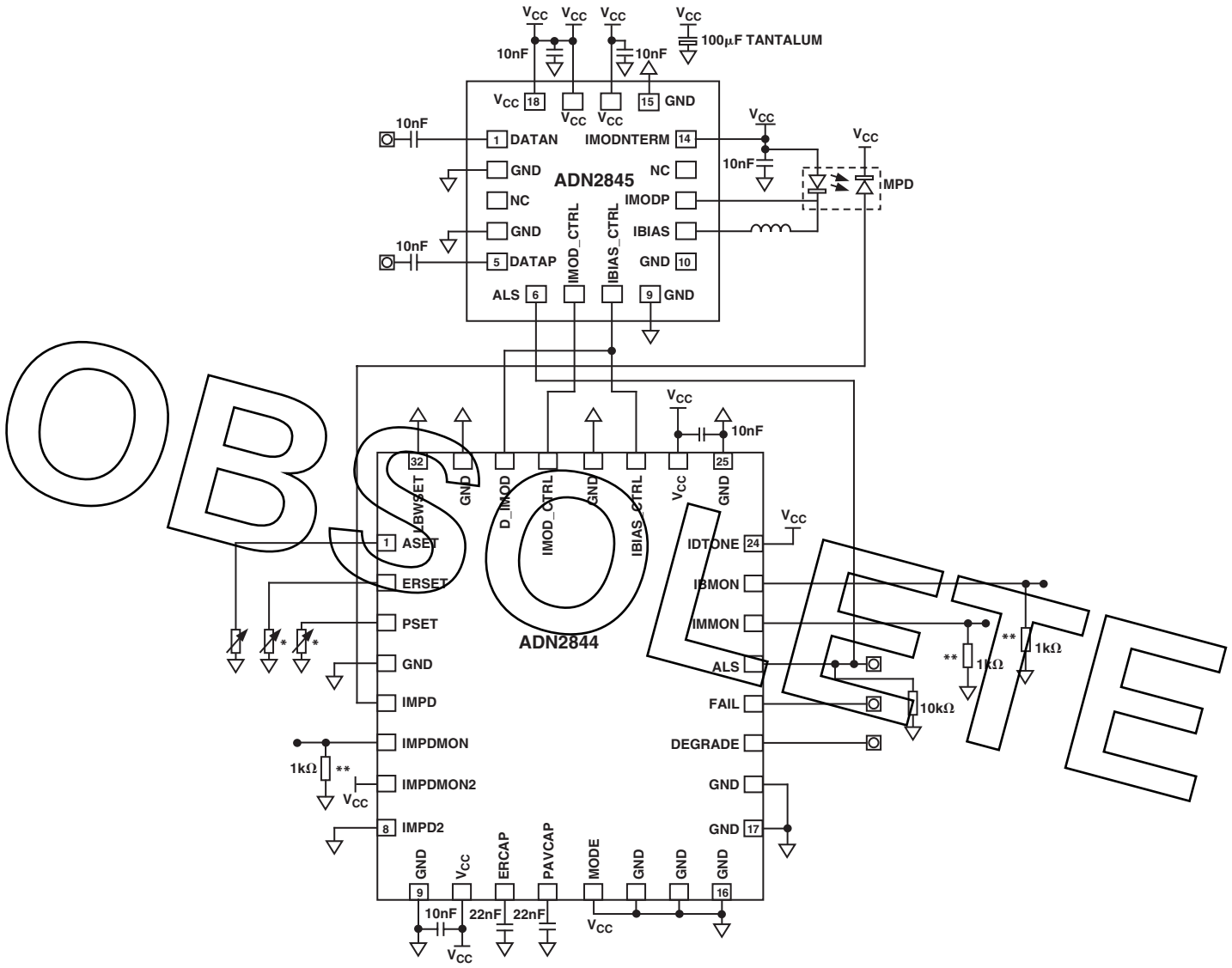


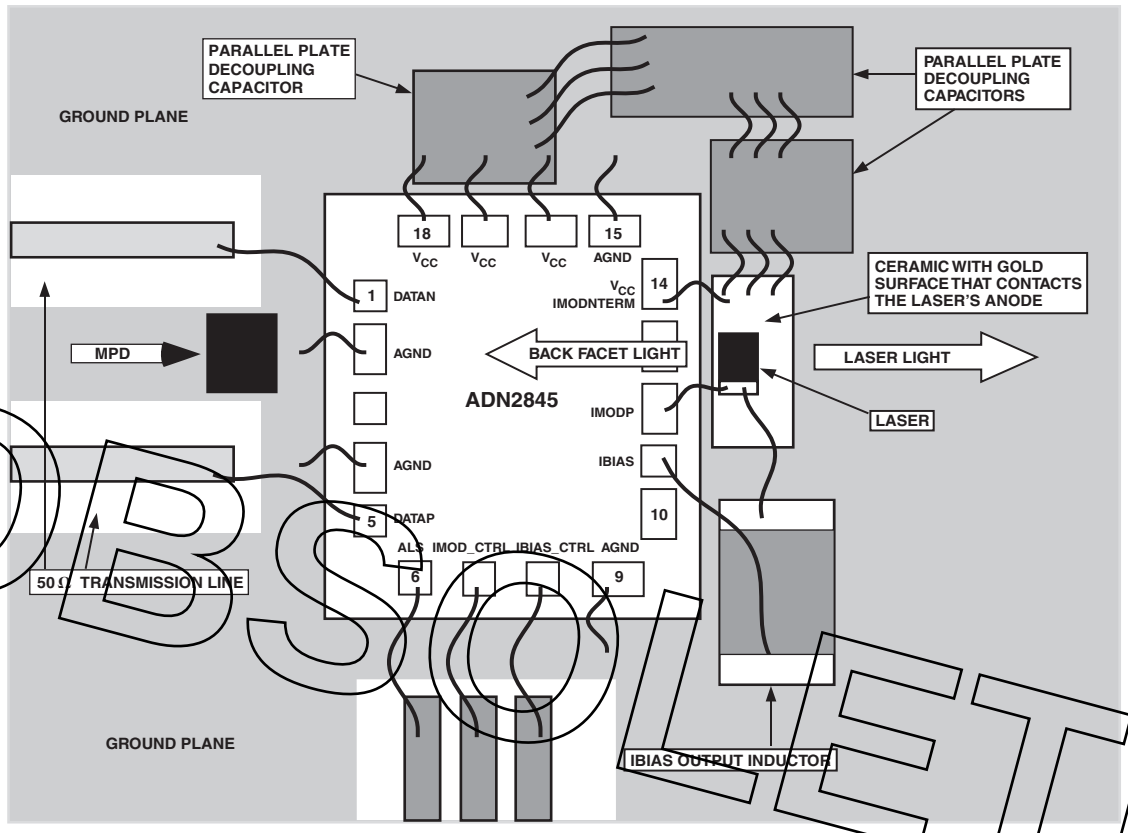
Figure 3. ADN2843 Application Circuit (Mode A)

- Best high frequency board layout techniques including power and ground planes should be used.
- To minimize inductance, keep the connections between the ADN2845 and the laser diode as short as possible. Inductances <0.3 nH are recommended for best performance. Critical bonds are IMODP and V_{CC} (Pin 14). Ribbon bonding can be used to reduce bond inductance. Minimize bond lengths for ADN2845 pads to achieve low inductance.
- Place bypass capacitor on laser anode as close to laser as possible.
- Bypass capacitors should be placed as close as possible to V_{CC} pads.
- 50 Ω controlled impedance interconnects should be used on the DATA inputs.
- Parasitic capacitance on IBIAS_CTRL and IMOD_CTRL interconnects should be less than 100 pF. If decoupling caps are used on IBIAS_CTRL and IMOD_CTRL, they should be tied to V_{CC} rather than GND.
- An inductor should be used in the bias current path. A Microwave Components coil 30-1847-GCCAS-01 (48 mil × 24 mil) should be used.
- The recommended substrate connection is to GND. However, the performance is not affected by connecting the substrate to V_{CC}.



NOTES
*FOR DIGITAL PROGRAMMING, THE ADN2850 OR ADN2860 OPTICAL SUPERVISOR CAN BE USED.
**OPTIONAL MONITORING OF CURRENTS.

Figure 4. ADN2843 Application Circuit (Mode B)



NOTES
- FOR OPTIMUM PERFORMANCE, RIBBON BONDS ARE RECOMMENDED ON PADS 1, 5, 12, AND 14. WIRES ARE 3 MIL OR 5 MIL RIBBONS <400μm LONG. ALL OTHER PINS CAN BE ROUND WIRE <1mm.
- LASER'S ANODE IS CONNECTED TO V_{CC} THROUGH GOLD LAYER ON TOP OF CERAMIC STANDOFF. STANDOFF MINIMIZES LENGTH OF PAD 12 AND PAD 14 RIBBONS.
- PARALLEL PLATE DECOUPLING CAPACITORS SHOULD BE >100pF AND BE OF MICROWAVE AVX TYPE, PART NO. GB0159391KA6N (390pF).
- THE RECOMMENDED SUBSTRATE CONNECTION IS TO GND. HOWEVER, PERFORMANCE IS NOT AFFECTED BY CONNECTING THE SUBSTRATE TO V_{CC}.
- AN INDUCTOR SHOULD BE USED IN THE BIAS CURRENT PATH. A MICROWAVE COMPONENTS COIL 30-1847-GCCAS-01 (48 MIL × 24 MIL) SHOULD BE USED.
- THE EXTERNAL POWER SUPPLY IS CONNECTED AT THE PARALLEL PLATE DECOUPLING CAPACITOR.

Figure 5. Recommended Layout

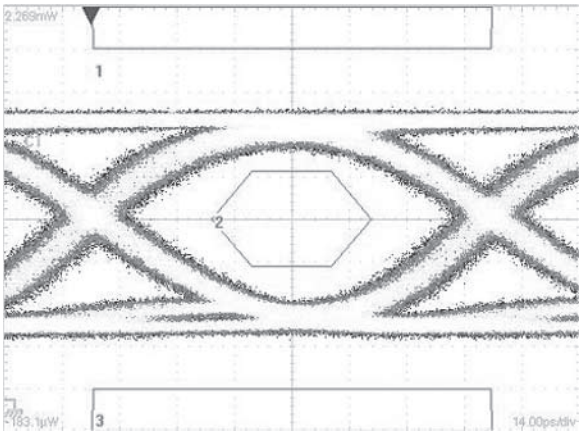


Figure 6. 10 Gbps Optical Diagram Provided Courtesy of NEL.
P_{AV} = 0 dBm, ER = 5 dB, PRBS 31 Pattern.

DIE PAD COORDINATES
(With Origin in the Center of the Die)

ADN2844

Pad Number	Pad Name	X (μm)	Y (μm)
1	ASET	1014.00	–1019.00
2	ERSET	769.00	–1019.00
3	PSET	486.00	–1019.00
4	GND	186.00	–1019.00
5	IMPD	–132.00	–1019.00
6	IMPDMON	–479.00	–1019.00
7	IMPDMON2	–811.00	–1019.00
8	IMPD2	–1056.00	–1019.00
9	GND	–1339.00	–877.00
10	V_{CC}	–1339.00	–672.00
11	ERCAP	–1339.00	–429.00
12	PAVCAP	–1339.00	–204.00
13	MODE	–1339.00	91.00
14	GND	–1339.00	335.00
15	GND	–1339.00	580.00
16	GND	–1339.00	824.00
17	GND	–1051.00	1019.00
18	GND	–761.00	1019.00
19	DEGRADE	–476.00	1019.00
20	FAIL	–207.00	1019.00
21	ALS	102.00	1019.00
22	IMMON	387.00	1019.00
23	IBMON	653.00	1019.00
24	IDTONE	904.00	1019.00
25	GND	1359.00	995.00
26	V_{CC}	1359.00	781.00
27	IBIAS_CNTRL	1359.00	523.00
28	GND	1359.00	317.00
29	IMOD_CTRL	1359.00	–29.00
30	D_IMOD	1359.00	–294.00
31	GND	1359.00	–562.00
32	GND	1359.00	–807.00

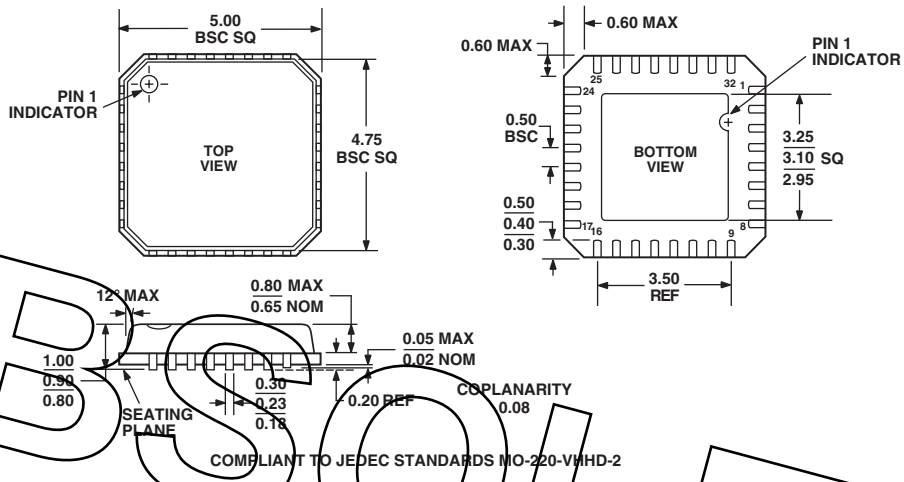
ADN2845

Pad Number	Pad Name	X (μm)	Y (μm)
1	DATAN	–500.00	400.00
2	GND*	–500.00	222.00
3	NC	–500.00	0.00
4	GND*	–500.00	–222.00
5	DATAP	–500.00	–400.00
6	ALS	–300.00	–600.00
7	IMOD_CTRL	–100.00	–600.00
8	IBIAS_CTRL	100.00	–600.00
9	GND*	300.00	–600.00
10	NC*	500.00	–400.00
11	IBIAS	500.00	–200.00
12	IMODP*	500.00	–30.00
13	NC*	500.00	178.00
14	V_{CC} (IMODN)*	500.00	378.00
15	GND*	300.00	600.00
16	V_{CC}*	100.00	600.00
17	V_{CC}*	–100.00	600.00
18	V_{CC}*	–300.00	600.00

*Denotes double bond pad.

OUTLINE DIMENSIONS

32-Lead Lead Frame Chip Scale Package [LFCSP]
5 mm × 5 mm
(CP-32)
Dimensions shown in millimeters



Exposed paddle should be soldered to the most negative supply of the ADN284
(ADN2844 also available as bare die)

C02764–0–4/03(0)