



# +60V Simple Swapper Hot-Swap Switch

MAX5923

## General Description

The MAX5923 is a fully integrated Simple Swapper™ hot-swap switch for positive supply rails. The device allows the safe insertion and removal of circuit cards into live backplanes or ports without causing glitches on the power-supply rail. The device also monitors various circuit parameters and disconnects the load if a fault condition occurs, alerting the host with a logic-level FAULT output. The MAX5923 operates over the +16V to +60V input voltage range.

During startup, an integrated 0.45Ω power MOSFET regulates the current and voltage between the backplane power source and the load. After startup, the MOSFET is fully enhanced to reduce its on-resistance. To ensure robust operation, the MAX5923 contains built-in safety features that monitor fault conditions and prevent damage to the internal MOSFET.

The MAX5923 monitors three parameters for fault conditions: zero current, overcurrent, and thermal overload. The output overcurrent limit counts the time the MAX5923 spends in an overcurrent condition and shuts down the pass transistor if the current limit is exceeded for the overcurrent time limit. The zero-current detection counts the time the output current is below the zero-current threshold and shuts down the pass transistor if the counter reaches the zero-current time limit. The thermal monitoring feature shuts down the pass transistor if the die temperature reaches the overtemperature limit. A fault logic output indicates when an overtemperature or an overcurrent condition has occurred and a zero-current logic output indicates if there is a zero-current condition.

An undervoltage detection circuitry keeps the pass transistor off until the input voltage is above the undervoltage lockout (UVLO) threshold, which is internally set or can be set externally with a resistive divider. A power-OK (POK) output is provided to signal when the output voltage has reached to within 0.75V of the input voltage. An Enable input allows the host system to disconnect the system from the load and/or reset a fault condition by toggling Enable.

The MAX5923 is available in a 20-pin TSSOP package and operates in the extended -40°C to +85°C temperature range.

## Applications

Network Routers/Switches	Servers
Current Limiter	Industrial Equipment

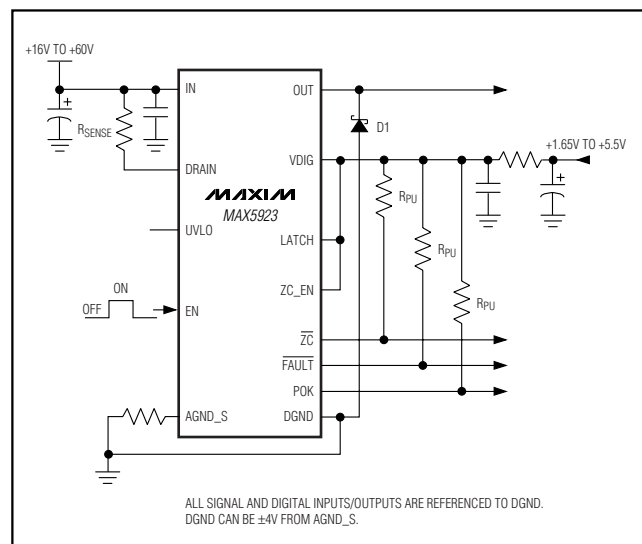
## Features

- ◆ Wide Operating Input Range: +16V to +60V
- ◆ 0.45Ω Integrated Power Switch
- ◆ Programmable Output Current Up to 800mA
- ◆ Over/Undercurrent-Limit Detection
- ◆ Input Logic Signals Compatible with 1.8V to 5V CMOS Logic
- ◆ Separate Analog and Digital Grounds with Up to ±4V Offset
- ◆ Power-OK Status Output
- ◆ Overcurrent Protection with Status Outputs
- ◆ Built-In Thermal Shutdown
- ◆ Internal Switch Protection Circuitry
- ◆ Current-Limit Foldback with Timeout and Duty-Cycle Control
- ◆ Latch or Autorestart Fault Management

## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX5923EUP	-40°C to +85°C	20 TSSOP

## Typical Operating Circuit



Simple Swapper is a trademark of Maxim Integrated Products, Inc.

Pin Configuration appears at end of data sheet.



Maxim Integrated Products 1

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## ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to AGND\_S, Unless Otherwise Noted  
 IN .....-0.3V to +76V  
 UVLO .....-0.3V to +6V  
 VDIG to DGND .....-0.3V to +6V  
 OUT .....-0.3V to (VDRAIN + 0.3V)  
 DRAIN .....-0.3V to (VIN + 0.3V)  
 EN, ZC\_EN, ZC, FAULT, POK  
 and LATCH to DGND .....-0.3V to +6V

DGND .....-5V to +5V  
 Maximum Current into DRAIN .....0.8A  
 Maximum Current into POK, ZC, FAULT (sinking) .....20mA  
 Continuous Power Dissipation (TA = +70°C)  
 20-Pin TSSOP (derate 11.1mW/°C above +70°C) .....879mW  
 Operating Temperature Range .....-40°C to +85°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +160°C  
 Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(VIN = 48V, VDIG = 3.3V, AGND\_S = AGND = DGND = 0V, RSENSE = 0.5Ω ±1%, UVLO = open, EN = VDIG, TA = -40°C to +85°C, unless otherwise noted. Typical values are at TA = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input Voltage Range	VIN		16		60	V
Analog Input Supply Current	IIN	VIN = 72V, measured at AGND after OUT has stopped slewing		1	1.6	mA
Digital Input Voltage Range	VDIG		1.65		5.5	V
Digital Input Supply Current	IDIG	VDIG = 5V		0.05	0.1	mA
DGND-to-AGND Operating Voltage Range			-4		+4	V
Current-Limit Response Time		OUT shorted to AGND (Note 1)		1		μs
OUT Current-Limit Foldback Voltage	VFBSTOP	(Note 2)		18		V
Current-Limit Sense Voltage (VIN - VDRES) (Note 3)	VILIM	Maximum voltage across RSENSE at VOUT > VFBSTOP	198	212	225	mV
		0°C to +85°C	203	212	221	
Current-Limit Sense Foldback Voltage (VIN - VDRES)	VILIM_fb	VOUT = 0V	64	70	76	mV
		0°C to +85°C	50	60	75	
Overcurrent Timeout	tOC	OUT shorted to AGND (Note 4)	50	60	70	ms
DMOS On-Resistance	RDSON	IOUT = 100mA	TA = +25°C	0.45		Ω
			TA = +85°C	0.75		
Power-Off OUT Sink Current		EN = DGND, VOUT = 48V			15	μA
Maximum Output Voltage Slew Rate		dVOUT/dt, VOUT rising, no load		100		V/ms
Maximum Output Current Slew Rate		dIOUT/dt, VOUT rising, CLOAD = 100μF		35		A/ms
Power-OK Threshold (VIN - VOUT)	VTHPOK	VOUT rising, POK from low to high	650	750	850	mV
		Hysteresis		10		%
POK Output Low Voltage	VPOK_LOW	IPOK = 3mA			0.4	V
POK Output Leakage Current		VPOK = 3.3V		0.05	1	μA

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## ELECTRICAL CHARACTERISTICS (continued)

( $V_{IN} = 48V$ ,  $V_{DIG} = 3.3V$ ,  $AGND\_S = AGND = DGND = 0V$ ,  $R_{SENSE} = 0.5\Omega \pm 1\%$ ,  $UVLO = open$ ,  $EN = V_{DIG}$ ,  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ C$ .)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POK Output Delay (Note 5)	tPOK_LOW	POK from high to low, $V_{OUT}$ falling	1	1.4	1.8	ms
	tPOK_HIGH	POK from low to high, $V_{OUT}$ rising	74	88	102	
Zero-Current Detection Threshold Voltage ( $V_{IN} - V_{DRS}$ )	VZCTH		2.7	3.75	4.8	mV
$\overline{ZC}$ Output Low Voltage	VZC_LOW	$I_{ZC} = 3mA$			0.4	V
$\overline{ZC}$ Output Leakage Current		$V_{ZC} = 3.3V$		0.05	1	$\mu A$
Zero-Current Detection Delay	tZCDEL	$\overline{ZC}$ from high to low, $I_{OUT}$ falling (Note 6)	300	350	400	ms
Zero-Current Deglitch Time	tZC_DEG	$I_{OUT}$ rising		10		ms
Thermal Shutdown		Temperature rising		150		$^\circ C$
		Hysteresis		30		
Shutdown Autorestart Time	tRESTART	LATCH = low (Note 7)	1.6	1.92	2.24	s
<b>UNDERVOLTAGE LOCKOUT</b>						
Default $V_{IN}$ UVLO	UVLOTH	UVLO floating, $V_{IN}$ rising	26	28	30	V
		Hysteresis		2.5		
UVLO Comparator Threshold	VREF	Referenced to AGND	1.31	1.33	1.36	V
		Hysteresis		110		mV
UVLO Input Resistance			50			k $\Omega$
<b>LOGIC SIGNALS</b>						
EN, LATCH, and ZC_EN Input High Voltage	$V_{IH}$	$1.65V < V_{DIG} < 5.5V$	$0.7 \times V_{DIG}$			V
EN, LATCH, and ZC_EN Input Low Voltage	$V_{IL}$	$1.65V < V_{DIG} < 2.0V$			$0.3V \times V_{DIG}$	V
		$2.0V < V_{DIG} < 5.5V$			0.8	
EN, LATCH, and ZC_EN Input Current			-1	+1		$\mu A$
EN Low Pulse Width			3			$\mu s$
$\overline{FAULT}$ Output Low Voltage	$V_{OL}$	$I_{SINK} = 3mA$			0.4	V
$\overline{FAULT}$ Output Leakage Current		$V_{\overline{FAULT}} = 3.3V$		0.05	1	$\mu A$

**Note 1:** This is the time from an output overcurrent or short-circuit condition until the output goes into regulated current limit.

**Note 2:** OUT voltage above which the output current limit is at its full value.

**Note 3:** See the *Overcurrent Protection* section.

**Note 4:** This is the time the part stays in current-limit mode during overload condition. After  $t_{OC}$  elapses (or when the junction temperature hits  $+150^\circ C$ ) the part shuts down.

**Note 5:** See *Typical Operating Characteristics*.

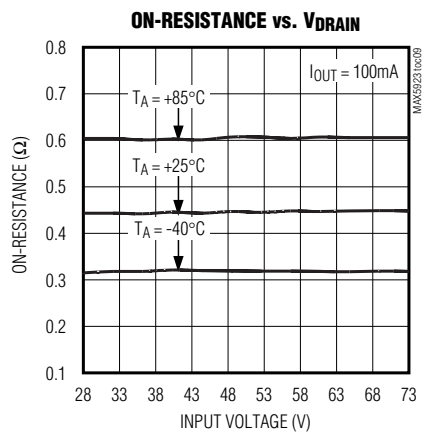
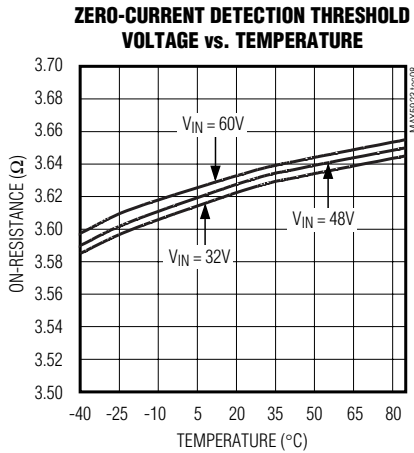
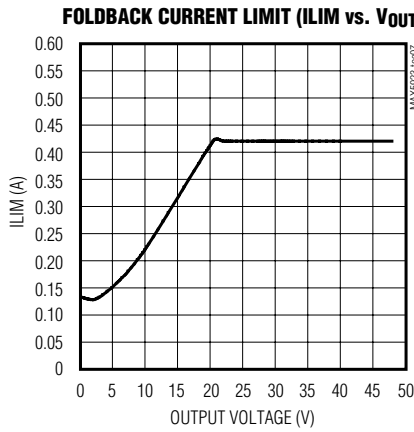
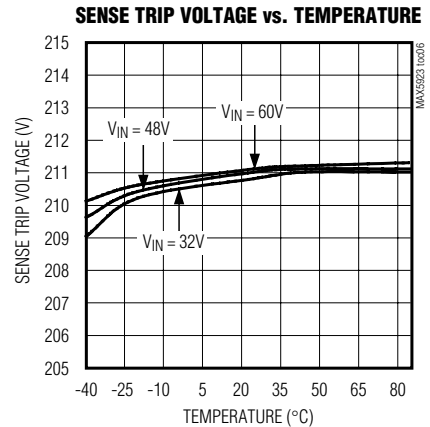
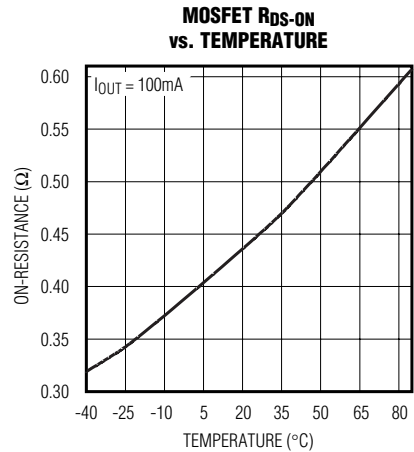
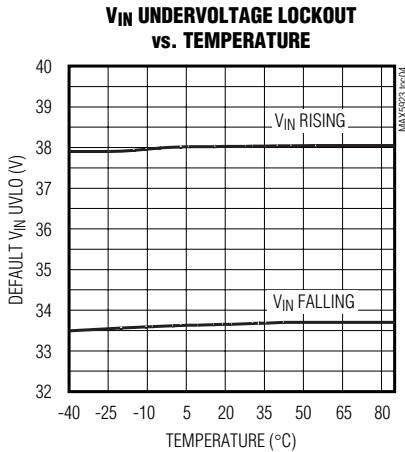
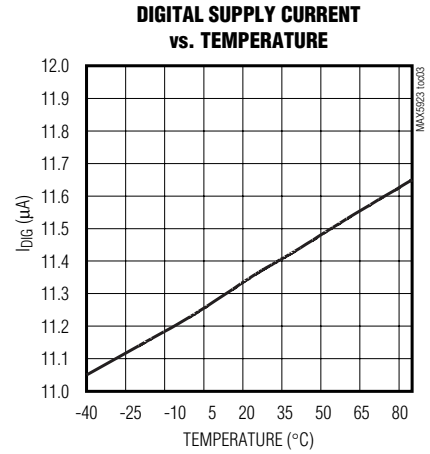
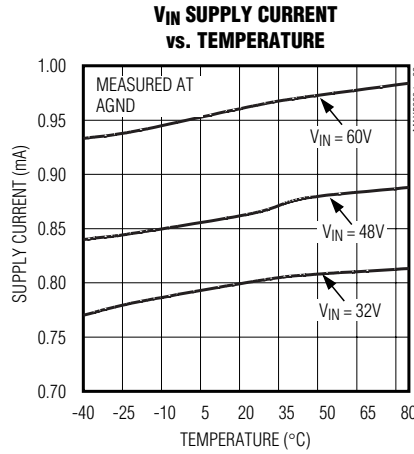
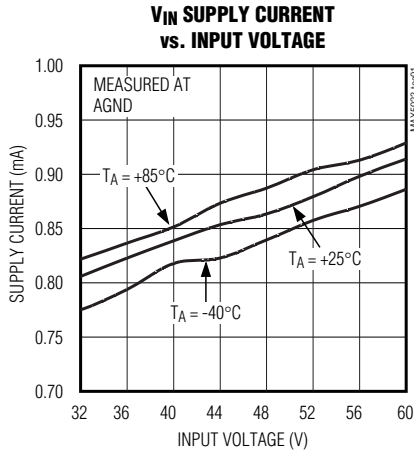
**Note 6:** This is the delay from  $I_{OUT}$  falling below the zero-current threshold until  $\overline{ZC}$  goes low. A  $\overline{ZC}$  condition shuts down and latches off the IC.

**Note 7:** See the *Fault Management* section.

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## Typical Operating Characteristics

( $V_{IN} = 48V$ , VDIG, EN, LATCH, CLASS, ZC\_EN = 3.3V, DCA, AGND\_S = AGND = DGND = 0V,  $R_{SENSE} = 0.5\Omega$ , UVLO floating,  $T_A = +25^\circ C$ , unless otherwise noted.)

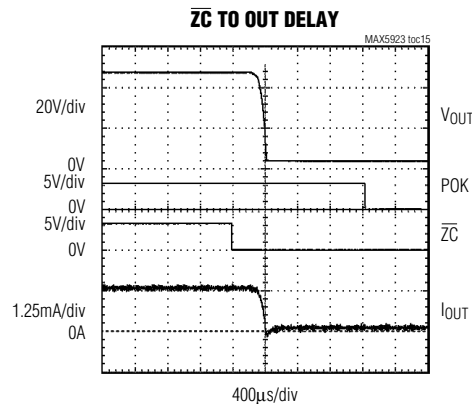
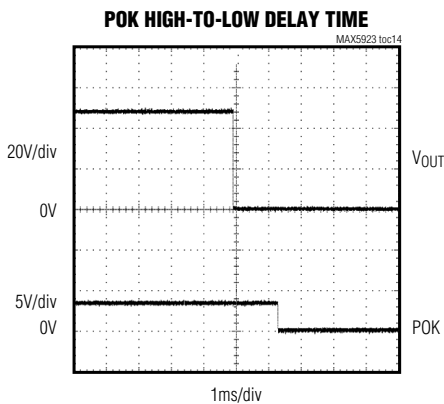
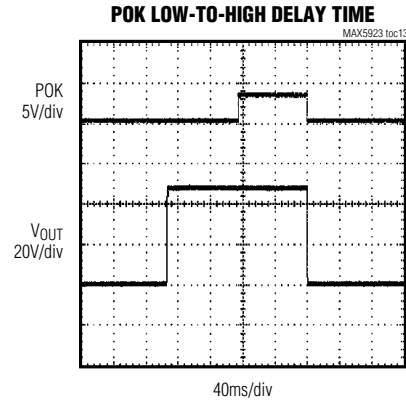
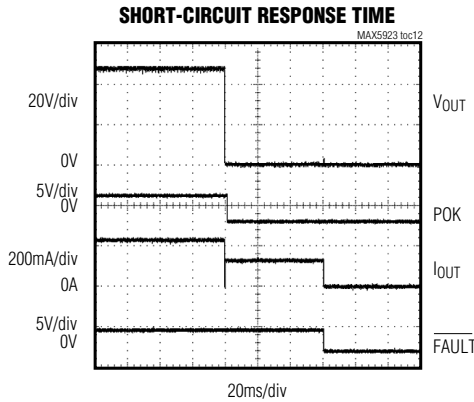
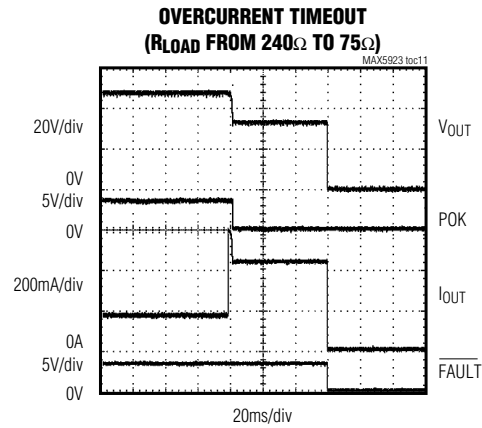
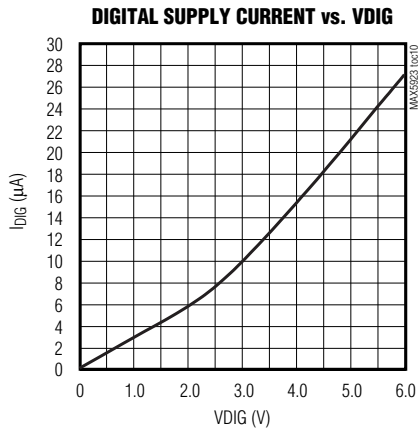


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## Typical Operating Characteristics (continued)

( $V_{IN} = 48V$ ,  $V_{DIG}$ , EN, LATCH, CLASS, ZC\_EN = 3.3V, DCA, AGND\_S = AGND = DGND = 0V,  $R_{SENSE} = 0.5\Omega$ , UVLO floating,  $T_A = +25^\circ C$ , unless otherwise noted.)

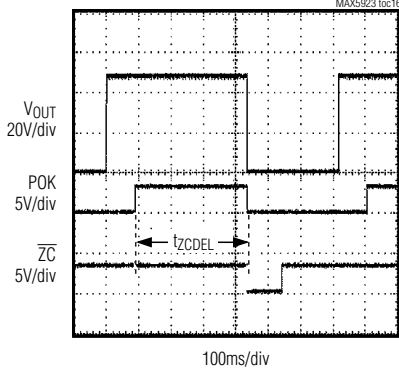


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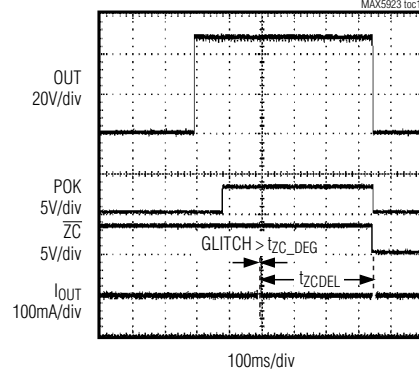
## Typical Operating Characteristics (continued)

( $V_{IN} = 48V$ ,  $V_{DIG}$ ,  $EN$ ,  $LATCH$ ,  $CLASS$ ,  $ZC\_EN = 3.3V$ ,  $DCA$ ,  $AGND\_S = AGND = DGND = 0V$ ,  $R_{SENSE} = 0.5\Omega$ ,  $UVLO$  floating,  $T_A = +25^\circ C$ , unless otherwise noted.)

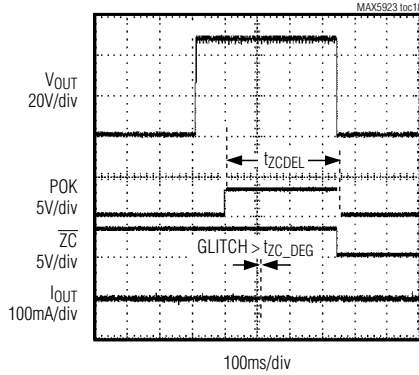
**ZERO CURRENT HIGH-TO-LOW  
DETECTION TIME WAVEFORM**



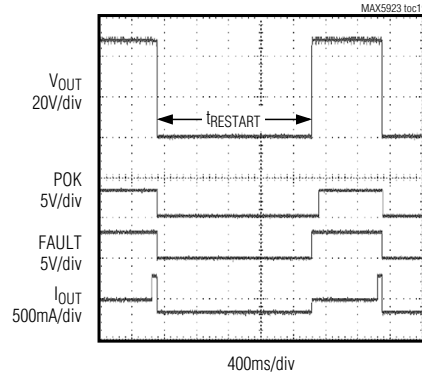
**ZERO CURRENT LOW-TO-HIGH  
DEGLITCH TIME WAVEFORM (11ms GLITCH)**



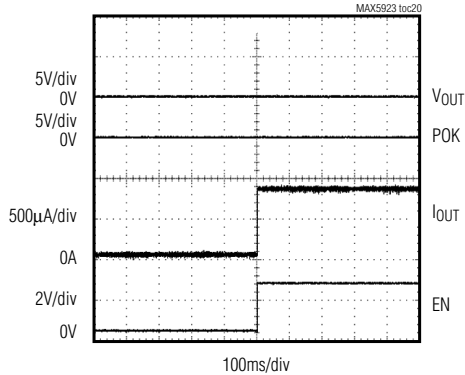
**ZERO CURRENT LOW-TO-HIGH  
DEGLITCH TIME WAVEFORM (10ms)**



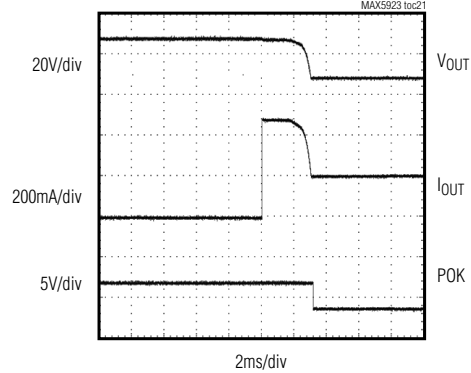
**OVERCURRENT RESTART DELAY**



**STARTUP WITH OUT  
SHORTED TO AGND**



**OVERCURRENT TIMEOUT  
( $R_{LOAD}$  FROM  $240\Omega$  TO  $75\Omega$ )**

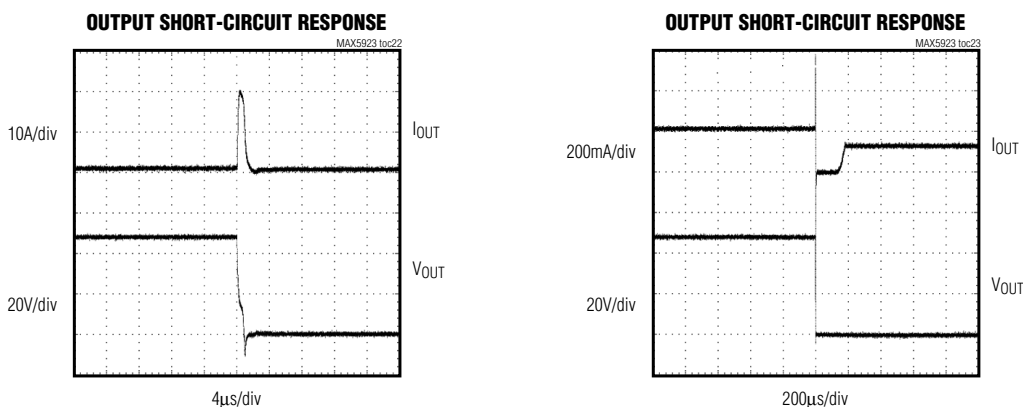


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## Typical Operating Characteristics (continued)

( $V_{IN} = 48V$ ,  $V_{DIG}$ , EN, LATCH, CLASS, ZC\_EN = 3.3V, DCA, AGND\_S = AGND = DGND = 0V,  $R_{SENSE} = 0.5\Omega$ , UVLO floating,  $T_A = +25^\circ C$ , unless otherwise noted.)



## Pin Description

PIN	NAME	FUNCTION
—	AGND	Analog Ground. This is the return of analog power input. AGND can vary $\pm 4V$ from DGND. AGND and DGND must be connected together at a single point in the system.
1, 2	DRAIN	Drain connection for the integrated MOSFET. Connect a sense resistor, $R_{SENSE}$ , from DRAIN to IN. These pins are also the current-sense resistor negative terminal. $R_{SENSE}$ sets the overcurrent-limit and open-circuit detection threshold. These two pins must be connected together.
3	IN	Input Voltage. Connect to a positive voltage source between 16V to 60V from IN to AGND. This is the current-sense resistor positive terminal. Bypass to AGND with a 100 $\mu F$ , 100V electrolytic capacitor and 0.1 $\mu F$ , 100V ceramic capacitor. Place the ceramic capacitor close to this pin.
4, 12, 18, 19	N.C.	No Connection. Not internally connected. Leave pins open. Pins are left unconnected to provide additional spacing between the high-voltage pins and other pins.
5	AGND_S	Analog Ground Sense. Connect a 1 $\Omega$ resistor from AGND_S to AGND. This resistor protects the IC during an output short-circuit condition.
6	UVLO	Undervoltage Lockout Adjustment Input. Referenced to AGND. Connect to the center point of a resistive divider from IN to AGND to adjust the UVLO threshold. Leave open for default value.
7	$\overline{FAULT}$	Fault Signal Open-Drain Logic Output. Reference to DGND. $\overline{FAULT}$ is latched low when: <ul style="list-style-type: none"> <li>An overtemperature condition occurs and/or,</li> <li>An overcurrent condition that has lasted for more than <math>t_{OC}</math>.</li> </ul>
8	POK	Power-OK Open-Drain Logic Output. Reference to DGND. POK goes open drain a time $t_{POK\_HIGH}$ after $V_{OUT}$ raises to within $V_{THPOK}$ from $V_{IN}$ . POK goes low a time $t_{POK\_LOW}$ after $V_{OUT}$ falls out of the $V_{THPOK}$ from $V_{IN}$ .
9	$\overline{ZC}$	Zero-Current Fault Signal. Open-drain logic output. Reference to DGND. $\overline{ZC}$ is latched low when there is a zero-current condition lasting longer than $t_{ZCDEL}$ . $\overline{ZC}$ is open drain otherwise. The zero-current detection circuit is enabled immediately after the POK signal goes high.
10	TP1	Must be left open or connected to AGND
11	TP3	Must be left open or connected to AGND



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## Pin Description (continued)

PIN	NAME	FUNCTION
13	DGND	Digital Ground. DGND can vary $\pm 4V$ from AGND. DGND and AGND must be connected together at a single point in the system.
14	LATCH	Fault Management Selection Digital Input. Referenced to DGND. Connect to logic high to latch off after a fault condition. Connect to logic low for automatic restart after a fault condition (see the <i>Fault Management</i> section).
15	ZC_EN	Zero-Current Detection Enable Logic Input. Referenced to DGND. Connect ZC_EN to a logic high to enable the zero-current detection circuitry. Connect ZC_EN to a logic low to disable this function.
16	EN	ON/OFF Control-Logic Input. Referenced to DGND. Connect to logic high to enable the device. Connect to logic low to disable the device and reset a latched-off condition.
17	VDIG	Digital Supply Voltage. VDIG is the supply voltage for the internal digital logic circuitry. EN, LATCH, and ZC_EN input logic thresholds are automatically scaled to the voltage on VDIG. See the <i>Typical Application Circuit</i> for proper filtering.
20	OUT	Output Voltage

### Detailed Description

The MAX5923 is a fully integrated hot-swap switch that contains a  $0.45\Omega$  integrated power MOSFET and operates from a +16V to +60V supply rail. The device allows the safe insertion and removal of circuit cards into live backplanes without causing problematic glitches on the supply rail. The device also monitors various circuit parameters and disconnects the load if a fault condition occurs, alerting the host with a logic-level FAULT output.

The MAX5923 provides an Enable input to enable/disable the device with a logic signal and logic output POK that indicates when the output voltage has reached within 750mV of the input voltage. Three fault conditions are monitored: a zero-current condition, an overcurrent condition, and a thermal overload condition. A FAULT output indicates to the host if an overcurrent or thermal fault occurs and a  $\overline{ZC}$  output indicates if the output has a zero-current condition. An undervoltage lockout circuitry shuts down the device if the input voltage falls below the UVLO threshold.

#### Power-Up Mode

During power-up, the MAX5923 gradually turns on the integrated N-channel MOSFET. To minimize EMI, the MAX5923 limits the output voltage slew rate at the OUT pin to  $dV_{OUT}/dt = 100V/ms$  (max) and the output current slew rate out of the OUT pin to  $dI_{OUT}/dt = 35A/ms$  (max).

The MAX5923 has an integrated  $0.45\Omega$  N-channel power MOSFET. The MOSFET's drain is connected to the DRAIN pin and its source is connected to the OUT pin. The MAX5923 monitors and provides current-limit protection to the load at all times. The current limit is programmable using an external current-sensing resistor

connected from IN to DRAIN. The MAX5923 features current-limit foldback and duty-cycle limit to ensure robust operation during load-fault and short-circuit conditions (see the *Overcurrent Protection* section).

When  $V_{OUT}$  is within 750mV of  $V_{IN}$  for more than  $t_{POK\_HIGH}$ , POK goes open-drain. After POK is asserted, the MAX5923 activates the zero-current detection function. This function monitors the output for an undercurrent condition and eventually turns off the power to the output if the load is disconnected (see the *Zero-Current Detection* section).

#### Undervoltage Lockout (UVLO)

The MAX5923 operates from a +16V to +60V supply voltage range and has a default UVLO set at +28V. The UVLO threshold is adjustable using a resistive divider connected to the UVLO pin (see Figure 1). When the input voltage is below the UVLO threshold, all operation stops and the MOSFET is held off. When the input voltage is above the UVLO threshold and EN is high, the MAX5923 goes into operation.

To adjust the UVLO threshold, connect an external resistive divider from IN to UVLO and then from UVLO to AGND. Use the following equation to calculate the new UVLO threshold:

$$V_{UVLO\_TH} = V_{REF} \left( 1 + \frac{R1}{R2} \right)$$

$V_{REF}$  is typically 1.33V. The UVLO pin input resistance is  $50k\Omega$  (min), so keep the R1 and R2 parallel combination value at least 20 times smaller than  $50k\Omega$  to minimize the new UVLO threshold error.



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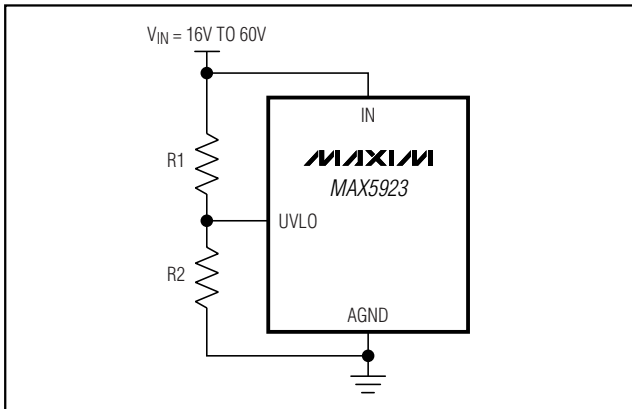


Figure 1. Setting Undervoltage Lockout with an External Resistive Divider

## Digital Logic

VDIG is the input supply for the internal logic circuitry. The logic input thresholds of EN, LATCH, and ZC\_EN are CMOS compatible and are determined by the voltage at VDIG, which can range from 1.65V to 5.5V. The POK and FAULT outputs are open-drain. VDIG and all logic inputs and outputs are referenced to DGND. DGND is not connected to AGND\_S internally and must be connected externally at a single point in the system to AGND\_S. The maximum allowable difference in the voltage between DGND and AGND is  $\pm 4V$ .

## Enable (EN)

EN is a logic input to enable MAX5923. Bringing EN low halts all operations and turns off the internal power MOSFET. When EN is high and the input voltage is above the UVLO threshold, the MAX5923 begins operating. Enable is also used to unlatch the part after a latched fault condition. This is done by toggling EN low and high again after a fault condition.

## Overcurrent Protection

The MAX5923 provides a sophisticated overcurrent protection circuitry to ensure the robust operation under output current transient and current-fault conditions. The current protection circuitry employs a Constant Current Limit, a Current Foldback, and an Overcurrent Timeout. The device monitors the voltage drop,  $V_{SENSE}$  ( $V_{SENSE} = V_{IN} - V_{DRAIN}$ ) in order to determine the load current.

## Constant Current Limit

The MAX5923 monitors  $V_{SENSE}$  at all times and regulates the current through the power MOSFET as necessary to keep  $V_{SENSE}$  (max) to the current-limit sense voltage ( $V_{ILIM} = 212mV$ ). The load-current limit,  $I_{LIM}$ , is programmed by the current-sense resistor,  $R_{SENSE}$ , connected from IN to DRAIN ( $I_{LIM} = V_{ILIM}/R_{SENSE}$ ).

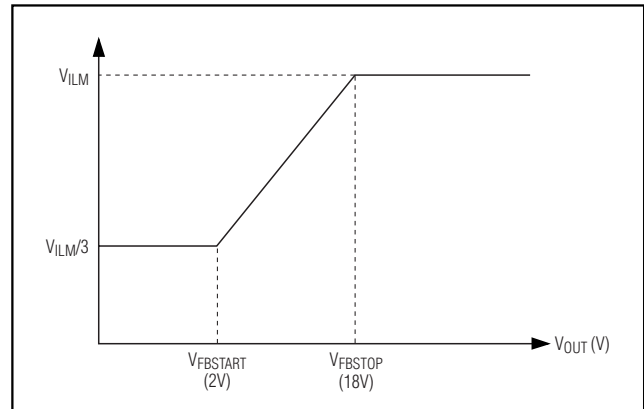


Figure 2. Current Foldback Characteristic

When the load current is less than  $I_{LIM}$ , the MOSFET is fully on. When the load is trying to draw more than  $I_{LIM}$ , the OUT pin works like a constant current source, limiting the output current to  $I_{LIM}$ . If  $I_{OUT}$  is greater than  $I_{LIM}$  for greater than the current-limit timeout, a current-limit fault is generated and the power MOSFET is turned off (see the *Overcurrent Timeout and Fault Management* section).

## Current Foldback

While in current-limit condition, the voltage at the OUT pin drops. As the load resistance reduces (more loading), the output voltage reduces accordingly to maintain a constant load current. The power dissipation in the power MOSFET is  $(V_{DRAIN} - V_{OUT}) \times I_{LIM}$ . As the output voltage drops lower, more power is dissipated across the power MOSFET. To reduce this power dissipation, the MAX5923 offers a current foldback feature where it linearly reduces the  $V_{ILIM}$  value when  $V_{OUT}$  drops below the OUT current-limit foldback voltage ( $V_{FBSTOP} = 18V$ ). Figure 2 illustrates this current foldback limit behavior.

## Overcurrent Timeout

The MAX5923 keeps track of the time it is in current limit. An internal digital counter begins incrementing its count at 1count/ms when  $V_{SENSE}$  exceeds its limit (either  $V_{ILIM}$  or  $V_{ILIM}$  foldback in foldback mode). The counter is reset to zero if the current falls back below the current limit. When the cumulative count reaches 60, an overcurrent fault is generated. After an overcurrent fault condition, the switch is turned off and the FAULT signal goes low. This overcurrent timeout enables the MAX5923 to operate in a periodic overcurrent condition without causing a fault. See Figure 3 for an example of periodic overcurrent condition without causing a fault.

## +60V Simple Swapper Hot-Swap Switch

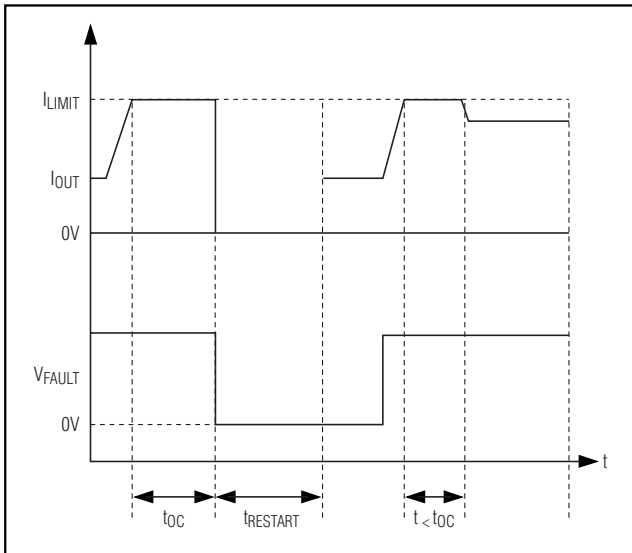


Figure 3. Periodic Overcurrent Without Generating a Fault

### Output Clamping During Short Circuit

During an output short-circuit condition, the energy stored in the output capacitor is dumped onto the short and builds up a large current in the power path and its parasitic inductance. The larger the output capacitor, the larger the current buildup. The parasitic inductive current circulates through the short circuit and brings OUT below ground level. A Schottky diode is needed at the output to provide the path for this circulating current and to prevent OUT from going too far below ground and exceeding the MAX5923's absolute maximum ratings.

For an output capacitor with low ESR (ceramic and film type), and with values of 0.47 $\mu$ F or less, a B1100LB (100V, 1A Schottky) is required as shown in the *Typical Application Circuit*. For higher values of capacitance, more robust clamping is required. For applications using aluminum electrolytic capacitors, which have relatively high ESR, the requirement of the clamp diode is reduced. Good layout with less parasitic trace inductance also helps in reducing the clamping diode requirement and should be examined on a case-by-case basis.

### Power-OK (POK)

POK goes open-drain  $t_{POK\_HIGH}$  (88ms) after  $V_{OUT}$  rises to within 0.75V ( $V_{THPOK}$ ) from  $V_{IN}$ . POK goes low  $t_{POK\_LOW}$  (1.4ms) after  $V_{OUT}$  drops 0.75V below  $V_{IN}$ .

### Zero-Current Detection

Zero-current detection is enabled if ZC\_EN is high and only after the startup period has finished (indicated by POK going high). When  $V_{SENSE}$  falls below the zero-current threshold ( $V_{ZC_{TH}}$ ) for a continuous  $t_{ZC_{DEL}} = 350$ ms, a zero-current fault is generated. The MOSFET is turned off and ZC is latched low. ZC is open drain during initial power-up. After a zero-current fault has occurred, the MAX5923 is latched off and is restarted by applying a low-to-high transition on the EN pin.

At any time during a zero-current condition, if  $V_{SENSE}$  goes above  $V_{ZC_{TH}}$  for the zero-current deglitch time ( $t_{ZC\_DEG} = 10$ ms), the zero-current counter resets to zero and a zero-current fault is not generated. Bring ZC\_EN low to disable the zero-current detection function. ZC stays high impedance in this mode.

### Thermal Shutdown

If the MAX5923 die temperature reaches +150°C, an overtemperature fault is generated. The MOSFET turns off and FAULT goes low. The MAX5923 die temperature must cool down below +120°C before the overtemperature fault condition is removed (see the *Fault Management* section).

### Fault Report (FAULT)

FAULT goes low when there is an overcurrent fault and/or an overtemperature fault. FAULT is open drain otherwise. After a fault, the FAULT signal is latched low. FAULT is unlatched at the beginning of the next power mode.

### Fault Management

The MAX5923 offers either latched-off or autoretry fault management configurable by the LATCH input. Bringing LATCH high puts the device into latch mode while pulling LATCH low selects the autoretry option.

In latch mode, the MAX5923 turns the MOSFET off and keeps it off after an overcurrent fault or an overtemperature fault. After the fault condition goes away, recycle the power supplies or toggle the EN pin low and high again to unlatch the part. However, the part waits a  $t_{RESTART}$  period (1.92s) before recovering from a fault condition and resuming normal operation.

In autoretry mode, MAX5923 turns the MOSFET off after an overcurrent or overtemperature fault. After the fault condition is removed, the device waits a  $t_{RESTART}$  period (1.92s) and then automatically restarts. If the fault was due to an overtemperature condition, the MAX5923 waits for its die temperature to cool down below the hysteresis level before starting the  $t_{RESTART}$  time.



# +60V Simple Swapper Hot-Swap Switch

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

TSSOP4.40mm.EPS

SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
A	—	1.10	—	.043
A <sub>1</sub>	0.05	0.15	.002	.006
A <sub>2</sub>	0.85	0.95	.033	.037
b	0.19	0.30	.007	.012
b <sub>1</sub>	0.19	0.25	.007	.010
c	0.09	0.20	.004	.008
c <sub>1</sub>	0.09	0.14	.004	.006
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	.169	.177
e	0.65 BSC		.026 BSC	
H	6.25	6.55	.246	.258
L	0.50	0.70	.020	.028
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

JEDEC	N	VARIATIONS				
		MILLIMETERS		INCHES		
AB-1	14	D	4.90	5.10	.193	.201
AB	16	D	4.90	5.10	.193	.201
AC	20	D	6.40	6.60	.252	.260
AD	24	D	7.70	7.90	.303	.311
AE	28	D	9.60	9.80	.378	.386

**NOTES:**

1. DIMENSIONS D AND E DO NOT INCLUDE FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE
5. "N" REFERS TO NUMBER OF LEADS

△ THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED

**DALLAS SEMICONDUCTOR** **MAXIM**

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, TSSOP 4.40mm BODY

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