

## FEATURES

- Hot Swap™ Controller for Positive and Negative Supplies
- Supply Tracking Mode
- ±2.7V to ±16.5V Operation
- Analog Current Limit with Foldback
- Allows Safe Board Insertion and Removal from a Live Backplane
- Open-Collector Power Good Comparators
- Automatic Retry or Latchoff After a Current Fault
- Dual Undervoltage Lockout Comparator Inputs
- Current Fault Indication

## APPLICATIONS

- Live Board Insertion
- RAID Systems
- -5.2V ECL Supplies
- Industrial Controls
- Split Supply Systems

## DESCRIPTION

The LT<sup>®</sup>4220 16-pin dual voltage Hot Swap controller allows a board to be safely inserted and removed from a live backplane. The device operates with any combination of 2.7V to 16.5V and -2.7V to -16.5V supplies. Using two external N-channel pass transistors, the board supply voltages can be ramped up at an adjustable rate. A selectable tracking mode allows dual supply tracking control for ramping the positive and negative supplies together.

The LT4220 features foldback current limit and latches off both gates if either supply remains in current limit longer than an adjustable time period. The IC can be configured for automatic restart after a delay set by the same timer.

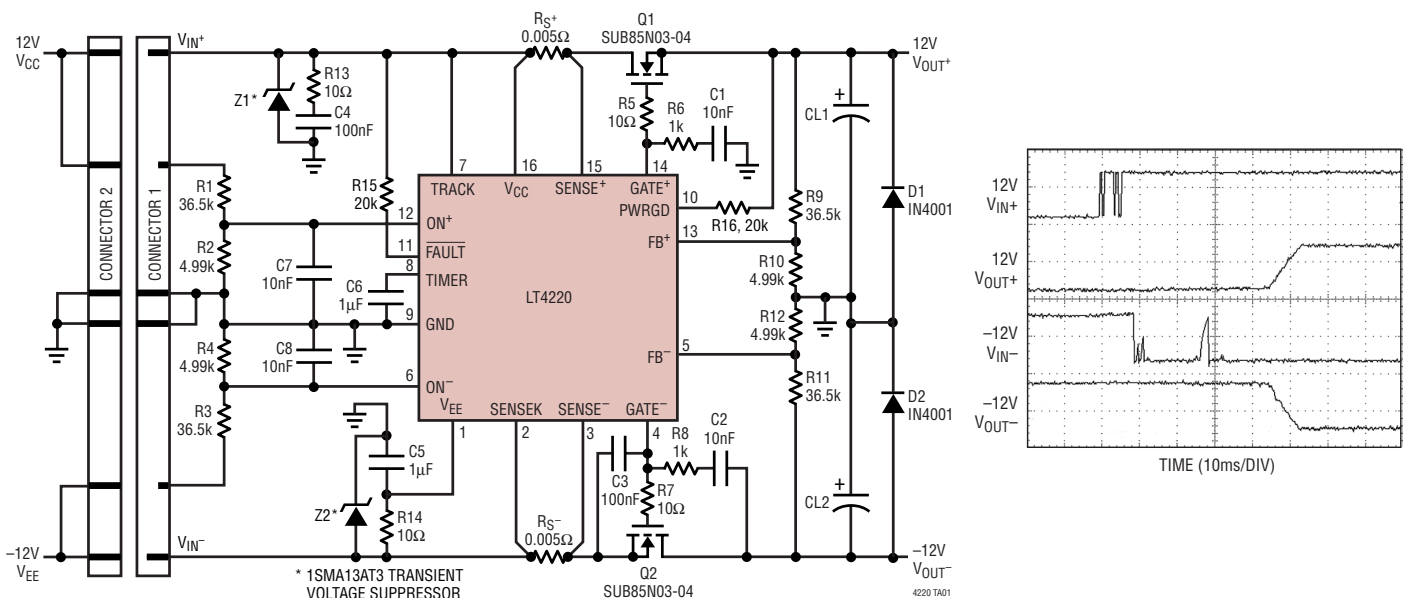
A power good signal indicates when the output voltages monitored by the two FB comparators are within tolerance, and the gate drive signals are at their full on voltage.

The LT4220 is available in a 16-lead narrow SSOP package.

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 Hot Swap is a trademark of Linear Technology Corporation.

## TYPICAL APPLICATION

±12V 10A Hot Swap Controller



# LT4220

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

$V_{CC}$ to GND	22V
$V_{EE}$ to GND	-22V
TRACK, TIMER	-0.3V to $V_{CC} + 0.3V$
ON <sup>+</sup> , FB <sup>+</sup>	$V_{EE} - 0.3V$ to $V_{CC} + 0.3V$
ON <sup>-</sup> , FB <sup>-</sup>	$V_{EE} - 0.3V$ to $V_{CC} + 0.3V$
GATE <sup>+</sup>	-0.3V to $V_{CC} + 8V$
GATE <sup>-</sup>	-16.5V with $V_{EE} = -22V$ to 0V
SENSE <sup>+</sup>	-0.3V to $V_{CC} + 5V$
SENSE <sup>-</sup> , SENSEK	$V_{EE} - 0.3V$ to $V_{EE} + 3V$
PWRGD, FAULT	-0.3V to $V_{CC} + 5V$
Operating Temperature Range	
LT4220C	$0^{\circ}C \leq T_A \leq 70^{\circ}C$
LT4220I	$-40^{\circ}C \leq T_A \leq 85^{\circ}C$
Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Lead Temperature (Soldering, 10 sec)	$300^{\circ}C$

## PACKAGE/ORDER INFORMATION

<p>TOP VIEW</p> <p>GN PACKAGE 16-LEAD PLASTIC SSOP <math>T_{JMAX} = 125^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p>	ORDER PART NUMBER
	LT4220CGN LT4220IGN
	GN PART MARKING
	4220 4220I

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_{CC} = 5V$ ,  $V_{EE} = -5V$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CC}$	$V_{CC}$ Operating Range		● 2.7		16.5	V
$I_{CC}$	$V_{CC}$ Supply Current		●	2.7	4	mA
$V_{EE}$	$V_{EE}$ Operating Range		● -2.7		-16.5	V
$I_{EE}$	$V_{EE}$ Supply Current			-1.6	-2.4	mA
$V_{PLKO}$	$V_{CC}$ Undervoltage Lockout		● 2.35	2.45	2.55	V
$V_{MLKO}$	$V_{EE}$ Undervoltage Lockout		● -2.4	-2.45	-2.5	V
$V_{ON+H}$	ON <sup>+</sup> ON Threshold	ON <sup>+</sup> Rising	● 1.22	1.24	1.26	V
$V_{ON+HYS}$	ON <sup>+</sup> Hysteresis		● 25	50	70	mV
$\Delta V_{ON+H}$	ON <sup>+</sup> ON Threshold Line Regulation	$V_{CC} = 2.7V, V_{EE} = -2.7V$ to $V_{CC} = 16.5V, V_{EE} = -16.5V$	●	0.02	0.15	mV/V
$\Delta V_{ON-H}$	ON <sup>-</sup> ON Threshold Line Regulation	$V_{CC} = 2.7V, V_{EE} = -2.7V$ to $V_{CC} = 16.5V, V_{EE} = -16.5V$	●	0.05	1	mV/V
$V_{ON-HYS}$	ON <sup>-</sup> Hysteresis		● 25	50	70	mV
$V_{ON-H}$	ON <sup>-</sup> ON Voltage Threshold	ON <sup>-</sup> Falling	● -1.22	-1.24	-1.26	V
$I_{ON+}$	ON <sup>+</sup> Input Current	$V_{ON+} = 2V$	●	0.01	±1	μA
$I_{ON-}$	ON <sup>-</sup> Input Current	$V_{ON-} = GND$	●	0.01	±1	μA
$V_{FB+H}$	FB <sup>+</sup> PWRGD Voltage Threshold	FB <sup>+</sup> Rising	● 1.22	1.24	1.26	V
$V_{FB+HYS}$	FB <sup>+</sup> Hysteresis	Gate = 5V	● 25	50	70	mV
$V_{FB-H}$	FB <sup>-</sup> PWRGD Voltage Threshold	FB <sup>-</sup> Falling	● -1.22	-1.24	-1.26	V
$V_{FB-HYS}$	FB <sup>-</sup> Hysteresis	Gate = 3V	● 25	50	70	mV

4220f

## DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $V_{EE} = -5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{\text{INFB}^+}$	FB <sup>+</sup> Input Current	FB <sup>+</sup> = 3V	●		0.09	±1	μA
$I_{\text{INFB}^-}$	FB <sup>-</sup> Input Current	FB <sup>-</sup> = -3V	●		0.08	±1	μA
$\Delta V_{\text{FB}^+ \text{H}}$	FB <sup>+</sup> PWRGD Threshold Line Regulation	$V_{CC} = 2.7\text{V}$ , $V_{EE} = -2.7\text{V}$ to $V_{CC} = 16.5\text{V}$ , $V_{EE} = -16.5\text{V}$	●		0.015	0.15	mV/V
$\Delta V_{\text{FB}^- \text{H}}$	FB <sup>-</sup> PWRGD Threshold Line Regulation	$V_{CC} = 2.7\text{V}$ , $V_{EE} = -2.7\text{V}$ to $V_{CC} = 16.5\text{V}$ , $V_{EE} = -16.5\text{V}$	●		0.05	0.5	mV/V
$V_{\text{SENSE}^+}$	SENSE <sup>+</sup> Trip Voltage ( $V_{CC} - V_{\text{SENSE}^+}$ )	$V_{\text{FB}^+} = 0\text{V}$ , GATE <sup>+</sup> - 0.5V $V_{\text{FB}^+} = 1\text{V}$ , GATE <sup>+</sup> - 0.5V	●	6 36	15 48	22 60	mV mV
$V_{\text{SENSE}^-}$	SENSE <sup>-</sup> Trip Voltage ( $V_{\text{SENSE}^-} - V_{\text{SENSE}^-}$ )	$V_{\text{FB}^-} = 0\text{V}$ , GATE <sup>-</sup> - 0.5V $V_{\text{FB}^-} = -1\text{V}$ , GATE <sup>-</sup> - 0.5V	●	-10 -43	-15 -52	-22 -61	mV mV
$I_{\text{GATEUP}^+}$	GATE <sup>+</sup> Pull-Up Current	Charge Pump On, $V_{\text{GATE}^+} = 7\text{V}$	●	-9	-13	-17	μA
$I_{\text{GATEUP}^-}$	GATE <sup>-</sup> Pull-Up Current	$V_{\text{GATE}^-} = -3\text{V}$	●	-6	-10	-14	μA
$I_{\text{GATEDN}^+}$	GATE <sup>+</sup> Pull-Down Current	Any Fault Condition, $V_{\text{GATE}^+} = 1\text{V}$	●	20	40	60	mA
$I_{\text{GATEDN}^-}$	GATE <sup>-</sup> Pull-Down Current	Any Fault Condition, $V_{\text{GATE}^-} = V_{EE} + 4\text{V}$	●	30	70	130	mA
$\Delta V_{\text{GATE}^+}$	External N-Channel GATE <sup>+</sup> Drive	$V_{\text{GATE}^+} - V_{CC}$ , $V_{CC} = 2.7\text{V}$ , $V_{EE} = -2.7\text{V}$ $V_{CC} = 5\text{V}$ to $16.5\text{V}$ , $V_{EE} = -5\text{V}$ to $-16.5\text{V}$	●	3.5 5	4 6.5	6 8	V V
$\Delta V_{\text{GATE}^-}$	External N-Channel GATE <sup>-</sup> Drive	$V_{\text{GATE}^-} - V_{EE}$ , $V_{CC} = 2.7\text{V}$ , $V_{EE} = -2.7\text{V}$ $V_{CC} = 5\text{V}$ to $16.5\text{V}$ , $V_{EE} = -5\text{V}$ to $-16.5\text{V}$	●	3.5 7.5	5.2 8.5	6 9	V V
$V_{\text{TIMERH}}$	TIMER High Threshold, Sets $\overline{\text{FAULT}}$		●	1.22	1.24	1.26	V
$V_{\text{TIMERL}}$	TIMER Low Threshold, Allows Restart		●	0.4	0.5	0.6	V
$I_{\text{TIMERUP}}$	TIMER Pull-Up Current	TIMER = 0V	●	-40	-65	-85	μA
$I_{\text{TIMERDN}}$	TIMER Pull-Down Current	TIMER = 1V	●	2	3.3	4.5	μA
$I_{\text{TIMER(R)}}$	TIMER Current Ratio	$I_{\text{TIMERDN}}/I_{\text{TIMERUP}}$			5	7	%
$V_{\text{OL}}$	PWRGD Output Low Voltage	$I_O = 2\text{mA}$ $I_O = 5\text{mA}$	●			0.3 0.5	V V
$I_{\text{OH}}$	PWRGD Leakage Current	$V_{\text{PWRGD}} = 16.5\text{V}$	●		0.1	2	μA
$V_{\text{FOL}}$	$\overline{\text{FAULT}}$ Output Low Voltage	$I_O = 2\text{mA}$ $I_O = 5\text{mA}$	●			0.3 0.5	V V
$I_{\text{FPH}}$	$\overline{\text{FAULT}}$ Leakage Current	$V_{\overline{\text{FAULT}}} = 16.5\text{V}$	●		0.06	2	μA
$V_{\text{TRKTHR}}$	TRACK Input Threshold		●	0.3	0.8	1.1	V
$I_{\text{TRK}}$	TRACK Input Current	TRACK = 16.5V	●		0.05	2	μA
$V_{\text{TRKFB}^+}$	TRACK Mode FB <sup>+</sup> Threshold	$I_{\text{GATE}^+} = 0\mu\text{A}$ , TRACK = $V_{CC}$ (Note 3)	●		40	70	mV
$V_{\text{TRKFB}^-}$	TRACK Mode FB <sup>-</sup> Threshold	$I_{\text{GATE}^-} = 0\mu\text{A}$ , TRACK = $V_{CC}$ (Note 3)	●		40	80	mV

## AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{CC} = 5\text{V}$ ,  $V_{EE} = -5\text{V}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{PHLON+}$	ON <sup>+</sup> Low to GATE <sup>+</sup> Low	5k Pull-Up to GATE <sup>+</sup> , 1nF Load Capacitor	● 0.6	0.8	1.2	$\mu\text{s}$
$t_{PLHON+}$	ON <sup>+</sup> High to GATE <sup>+</sup> High	5k Pull-Up to GATE <sup>+</sup> , 1nF Load Capacitor	● 0.6	1.5	3	$\mu\text{s}$
$t_{PHLFB+}$	FB <sup>+</sup> Low to PWRGD Low	5k Pull-Up to PWRGD	● 0.5	0.8	1.2	$\mu\text{s}$
$t_{PLHFB+}$	FB <sup>+</sup> High to PWRGD High	5k Pull-Up to PWRGD	● 0.6	1.25	3	$\mu\text{s}$
$t_{PHLON-}$	ON <sup>-</sup> Low to GATE <sup>-</sup> Low	5k Pull-Up to GATE <sup>-</sup> , 1nF Load Capacitor	● 0.6	1	1.5	$\mu\text{s}$
$t_{PLHON-}$	ON <sup>-</sup> High to GATE <sup>-</sup> High	5k Pull-Up to GATE <sup>-</sup> , 1nF Load Capacitor	● 1	2.1	3.5	$\mu\text{s}$
$t_{PHLFB-}$	FB <sup>-</sup> Low to PWRGD Low	5k Pull-Up to PWRGD	● 0.6	1	1.5	$\mu\text{s}$
$t_{PLHFB-}$	FB <sup>-</sup> High to PWRGD High	5k Pull-Up to PWRGD	● 0.8	1.25	2	$\mu\text{s}$
$t_{SENSE+}$	SENSE <sup>+</sup> to GATE <sup>+</sup> Low	1nF On GATE <sup>+</sup> , 100mV Step, 5k Pull-Up	● 1	4	6	$\mu\text{s}$
$t_{SENSE-}$	SENSE <sup>-</sup> to GATE <sup>-</sup> Low	1nF On GATE <sup>-</sup> , 100mV Step, 5k Pull-Up	● 1	4	6	$\mu\text{s}$

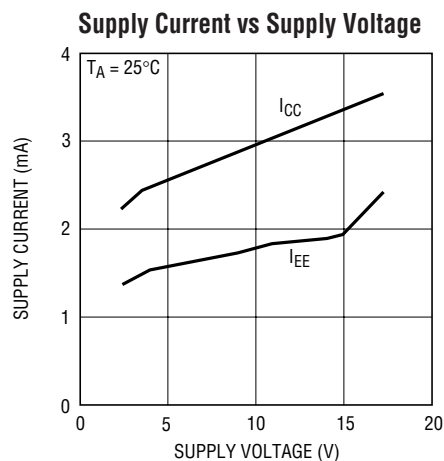
**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All currents into device pins are positive; all currents out of device

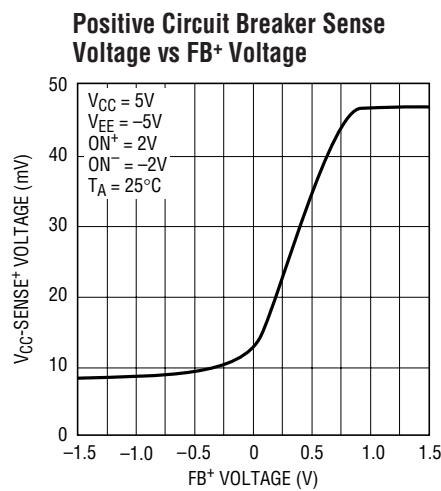
pins are negative. All voltages referenced to ground (GND) unless specified.

**Note 3:** The absolute voltage difference between FB<sup>+</sup> and FB<sup>-</sup> required to force either the GATE<sup>+</sup> or GATE<sup>-</sup> current to 0 $\mu\text{A}$ .

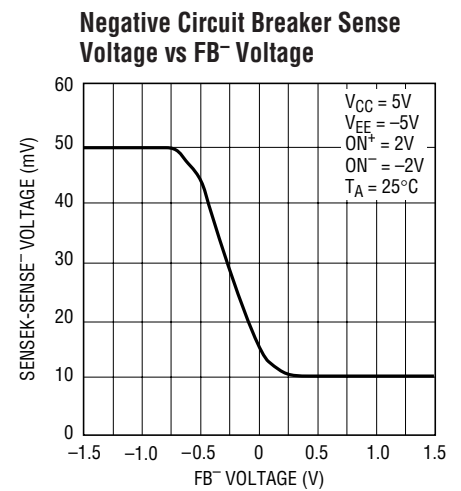
## TYPICAL PERFORMANCE CHARACTERISTICS



4220 G01



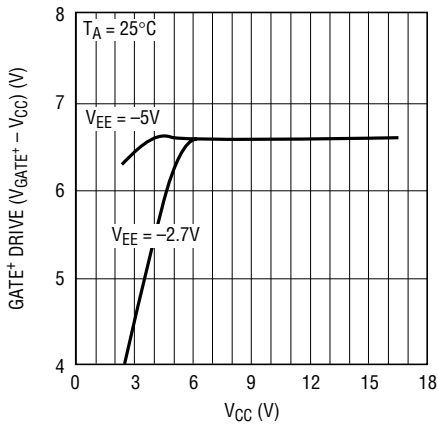
4220 G02



4220 G03

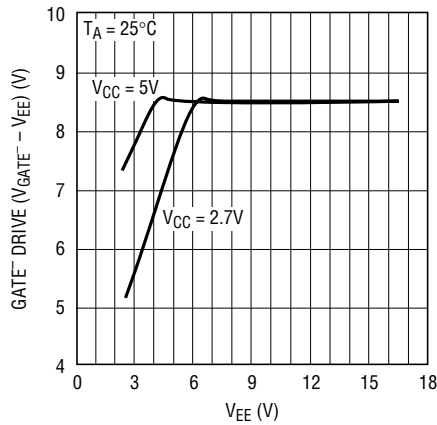
# TYPICAL PERFORMANCE CHARACTERISTICS

**GATE+ Drive vs V<sub>CC</sub>**



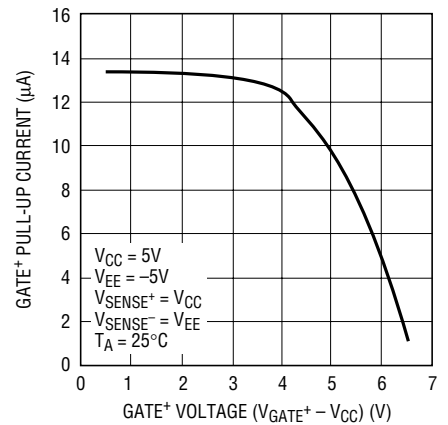
4220 G04

**GATE- Drive vs V<sub>EE</sub>**



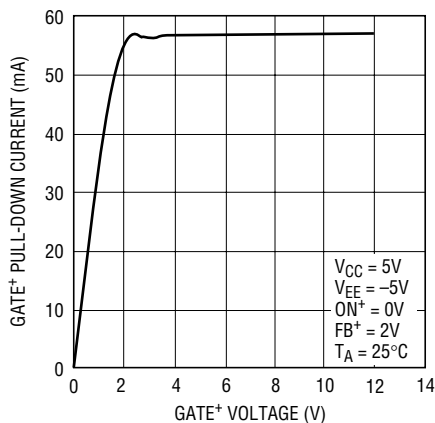
4220 G05

**GATE+ Pull-Up Current vs GATE+ Voltage**



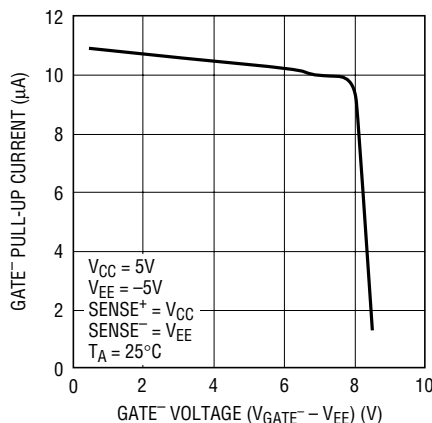
4220 G06

**GATE+ Pull-Down Current vs GATE+ Voltage**



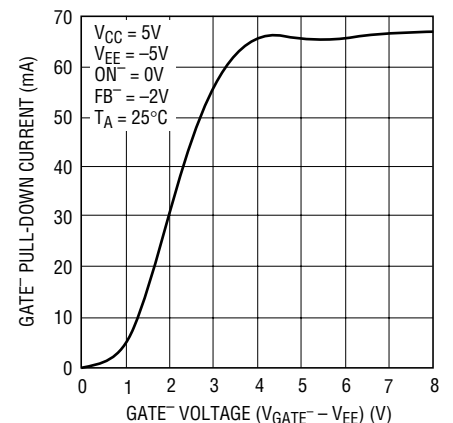
4220 G07

**GATE- Pull-Up Current vs GATE- Voltage**



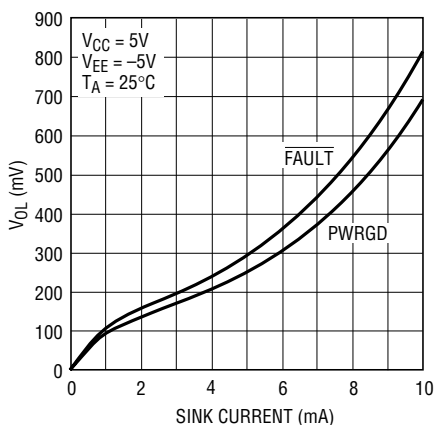
4220 G08

**GATE- Pull-Down Current vs GATE- Voltage**



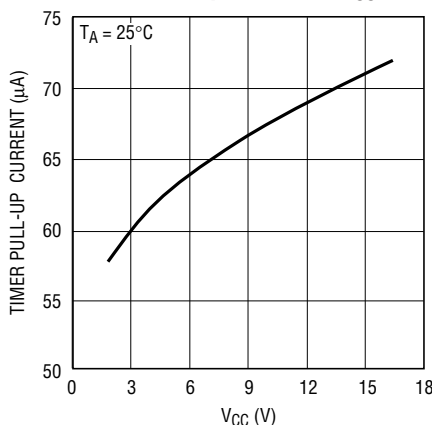
4220 G09

**PWRGD and FAULT V<sub>OL</sub> vs Sink Current**



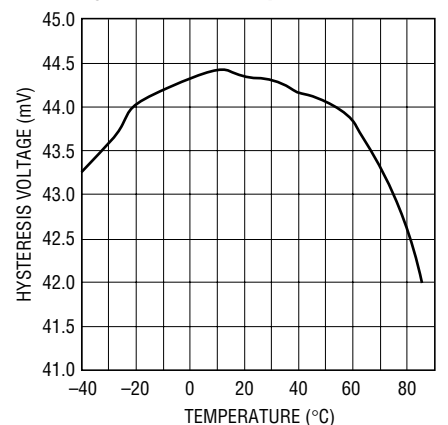
4220 G10

**TIMER Pull-Up Current vs V<sub>CC</sub>**



4220 G11

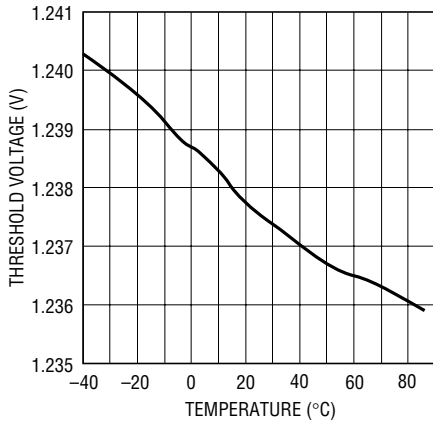
**ON+, ON- and FB+, FB- Hysteresis vs Temperature**



4220 G12

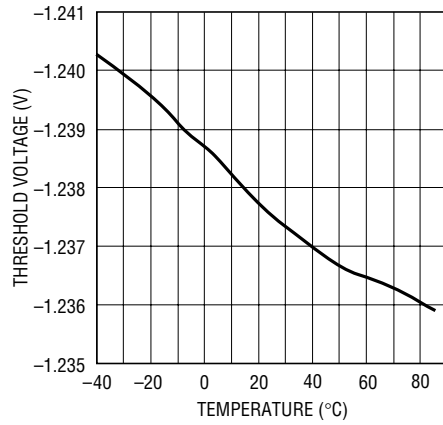
## TYPICAL PERFORMANCE CHARACTERISTICS

**FB<sup>+</sup> and ON<sup>+</sup> Threshold Voltage vs Temperature**



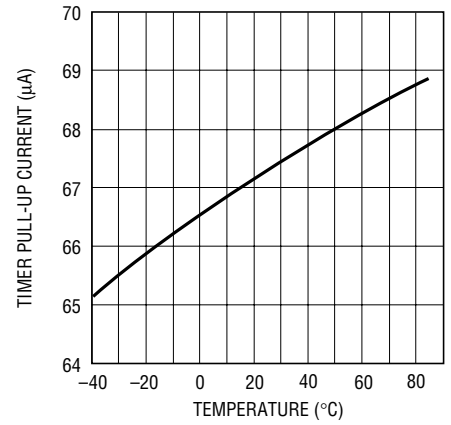
4220 G13

**FB<sup>-</sup> and ON<sup>-</sup> Threshold Voltage vs Temperature**



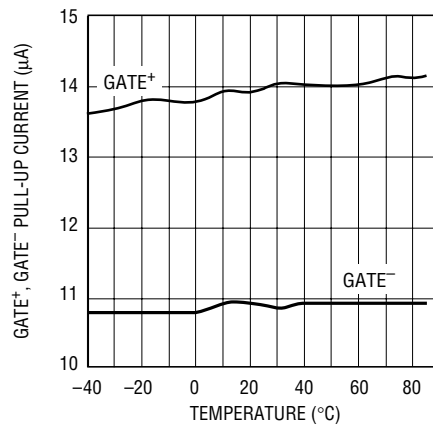
4220 G14

**TIMER Pull-Up Current vs Temperature**



4220 G15

**GATE<sup>+</sup>, GATE<sup>-</sup> Pull-Up Current vs Temperature**



4220 G16

## PIN FUNCTIONS

**$V_{EE}$  (Pin 1):** Negative Supply. The negative supply input ranges from  $-2.7V$  to  $-16.5V$  for normal operation.  $I_{EE}$  is typically  $-1.6mA$ . An internal undervoltage lockout circuit disables the device for inputs greater than  $-2.45V$ . A  $10\Omega$ ,  $1\mu F$  RC bypass network from  $V_{IN-}$  to the  $V_{EE}$  pin decouples transients from the device.

**SENSEK (Pin 2):** Negative Supply Current Limit Kelvin Sense Pin. Connect to  $V_{IN-}$ .

**SENSE<sup>-</sup> (Pin 3):** Negative Supply Current Limit Sense Pin. A sense resistor is placed in the supply path between SENSEK and SENSE<sup>-</sup>. The current limit circuit will regulate the voltage across the sense resistor to  $-50mV$  (SENSEK – SENSE<sup>-</sup>) when the  $FB^-$  voltage is less than  $-0.7V$ . If  $V_{FB^-}$  goes above  $-0.7V$ , the voltage across the sense resistor decreases linearly and stops at  $-15mV$  when  $V_{FB^-}$  is  $0V$ . If current limit is not used, connect to SENSEK.

**GATE<sup>-</sup> (Pin 4):** Gate Drive for the External Negative Supply N-Channel FET. An internal  $10\mu A$  current source drives the pin. An external capacitor connected from the GATE<sup>-</sup> pin to  $V_{OUT-}$  will control the rising slope of the  $V_{OUT-}$  signal. The voltage is clamped to  $9V$  above  $V_{EE}$ .

When the current limit is reached, the GATE<sup>-</sup> pin voltage will be adjusted to maintain a constant voltage across the  $R_{S^-}$  resistor while the timer capacitor starts to charge. If the TIMER pin voltage exceeds  $1.24V$ , the fault latch will be set and both GATE<sup>-</sup> and GATE<sup>+</sup> pins will be pulled low.

The GATE<sup>-</sup> pin is pulled to  $V_{EE}$  whenever the ON<sup>+</sup> pin is below  $1.24V$ , the ON<sup>-</sup> pin is above  $-1.24V$ , or either supply is in the undervoltage lockout voltage range, or the fault latch is set by the TIMER pin rising above  $1.24V$ .

**FB<sup>-</sup> (Pin 5):** Negative Power Good Comparator Input. This pin monitors the negative output voltage ( $V_{OUT-}$ ) with an external resistive divider. When the voltage on  $FB^-$  is below  $-1.24V$  and the initial GATE<sup>-</sup> drive voltage has reached a maximum (indicated by setting the internal GATE<sup>-</sup> good latch) and the  $FB^+$  release conditions are met, the PWRGD pin is released. PWRGD is pulled low when the  $FB^-$  pin is above  $-1.185V$ . Note the PWRGD pin is wire-ORed with the  $FB^+$  pin conditions.

$FB^-$  also controls the negative supply current limit sense amplifier input offset to provide foldback current limit. The  $FB^-$  pin linearly reduces the negative supply sense amplifier offset from  $-52mV$  to  $-15mV$  for  $FB^-$  in the range  $-0.75V < FB^- < 0V$ . To disable  $V_{EE}$  PWRGD and foldback current limit, the  $FB^-$  pin should be set to a voltage in the range:  $-1.3V > FB^- > V_{EE} + 0.5V$  but should never be more negative than  $-5.8V$  for normal operation.

**ON<sup>-</sup> (Pin 6):** The Negative Supply Good Comparator Input. This pin monitors the negative input voltage ( $V_{EE}$ ) with an external resistive divider for undervoltage lockout. When the voltage at the ON<sup>-</sup> pin is below the  $V_{ON-H}$  high-to-low threshold ( $-1.24V$ ), the negative supply is considered good. If the ON<sup>-</sup> pin rises above  $-1.185V$ , both GATE<sup>-</sup> and GATE<sup>+</sup> are pulled low. If ON<sup>-</sup> is not used, the ON<sup>-</sup> pin should be set to  $-1.3V > ON^- > V_{EE} + 0.5V$ .

**TRACK (Pin 7):** Supply Tracking Mode Control. If the TRACK pin is pulled high, the internal supply tracking circuit will be enabled during start-up. The TRACK circuit monitors the  $FB^+$  and the  $FB^-$  pins to keep their magnitude within a small voltage range by controlling the GATE<sup>+</sup> and GATE<sup>-</sup> charge currents. The tracking is disabled when either FB comparator indicates the output is good. Tracking is re-enabled if ON<sup>+</sup> is pulled below  $1.185V$ , ON<sup>-</sup> is pulled above  $-1.185V$  or either supply is below the internal undervoltage lockout. Typically, the TRACK pin is tied to GND or to  $V_{CC}$ . If left floating, tracking is enabled.

**TIMER (Pin 8):** Fault Time Out Control. An external timing capacitor at this pin programs the maximum time the part is allowed to remain in current limit before issuing a fault and turning off the external FETs. Additionally, for autorestart, this pin controls the time before an autorestart is initiated.

When the part goes into current limit, a  $65\mu A$  pull-up current source starts to charge the timing capacitor. When the voltage reaches  $V_{TIMERH}$  ( $1.24V$ ), the internal fault latch is set, FAULT pulls low and both GATE pins are pulled low; the pull-up current will be turned off and the capacitor is discharged by a  $3.3\mu A$  pull-down current. When the TIMER pin falls below  $0.5V$ , the part is allowed to restart if the ON<sup>+</sup> pin is pulsed below  $1.185V$ , thereby resetting internal fault latch—typically done by connecting the

## PIN FUNCTIONS

$\overline{\text{FAULT}}$  pin to the  $\text{ON}^+$  pin, otherwise the part remains latched off.

To disable the timeout circuit breaker, connect the  $\text{TIMER}$  pin to GND.

**GND (Pin 9):** Supply Ground Pin.

**PWRGD (Pin 10):** Open-Collector Output to GND.  $\text{PWRGD}$  goes to high impedance after the initial  $\text{GATE}^-$  and final  $\text{GATE}^+$  pins have reached their maximum voltage and after the  $\text{FB}^+$  pin goes above 1.24V low-to-high threshold and after the  $\text{FB}^-$  pin falls below  $-1.24\text{V}$  high-to-low threshold. An external pull-up resistor can pull the pin to a voltage higher or lower than  $V_{\text{CC}}$ . If not used,  $\text{PWRGD}$  can be left floating or tied to GND.

**$\overline{\text{FAULT}}$  (Pin 11):** Open-Collector Output to GND. The  $\overline{\text{FAULT}}$  pin is pulled low whenever the  $\text{TIMER}$  pin rises above  $V_{\text{TIMERH}}$  (1.24V) threshold, thereby setting the internal fault latch. It goes to high impedance whenever the internal fault latch is reset. The fault latch is reset with either internal undervoltage lockout conditions, or by the  $\text{ON}$  comparators if the  $\text{TIMER}$  pin is also below 0.5V. If not used, the  $\overline{\text{FAULT}}$  pin can be left floating or tied to GND.

**$\text{ON}^+$  (Pin 12):** Positive Supply Good Comparator Input. It monitors the positive input voltage ( $V_{\text{CC}}$ ) with an external resistive divider for undervoltage lockout. When the voltage on  $\text{ON}^+$  is above the  $V_{\text{ON+H}}$  high-to-low threshold (1.24V) the positive supply is considered good. If  $\text{ON}^+$  drops below 1.185V, both  $\text{GATE}^-$  and  $\text{GATE}^+$  are pulled low.

If  $\text{ON}^+$  is pulled low after a current limit fault and when the  $\text{TIMER}$  pin is below 0.5V, the fault latch is reset allowing the part to turn back on. Typically the  $\overline{\text{FAULT}}$  pin is tied back to the  $\text{ON}^+$  pin for autorestart. If not used, the  $\text{ON}^+$  pin should be set to a voltage in the range of  $1.3\text{V} < \text{ON}^+ < V_{\text{CC}} + 0.3\text{V}$ . The  $\text{ON}^+$  pin requires a bypass capacitor connected to ground.

**$\text{FB}^+$  (Pin 13):** Positive Power Good Comparator Input. This pin monitors the positive output voltage ( $V_{\text{OUT+}}$ ) with an external resistor divider. When the voltage on  $\text{FB}^+$  is above the  $V_{\text{FB+H}}$  low-to-high threshold (1.24V) and the  $\text{GATE}^+$  drive voltage has reached a maximum, the  $\text{PWRGD}$  is

released.  $\text{PWRGD}$  is pulled low when the  $\text{FB}^+$  pin is below 1.185V. The  $\text{PWRGD}$  pin is wire-ORed with the  $\text{FB}^-$  pin conditions.

$\text{FB}^+$  also controls the positive current limit sense amplifier input offset to provide foldback current limit. The  $\text{FB}^+$  pin linearly reduces the positive sense amplifier offset from 48mV to 15mV for  $\text{FB}^+$  in the range  $0.85\text{V} > \text{FB}^+ > 0\text{V}$ . If  $\text{PWRGD}$  and foldback current limit are not used, the  $\text{FB}^+$  pin should be set to a voltage in the range of  $1.3\text{V} < \text{FB}^+ < V_{\text{CC}} + 0.3\text{V}$ .

**$\text{GATE}^+$  (Pin 14):** High Side Gate Drive for the External Positive Supply N-Channel FET. An internal charge pump guarantees at least 3.5V above  $V_{\text{CC}}$ , for supply voltages at  $\pm 2.7\text{V}$  increasing to a minimum of 5V above  $V_{\text{CC}}$  for supply voltages greater than  $\pm 5\text{V}$ . A 10 $\mu\text{A}$  pull-up current source drives the pin. An external capacitor connected from the  $\text{GATE}^+$  pin to GND will control the rising slope of the  $\text{GATE}^+$  signal. The voltage is clamped to 7V above  $V_{\text{CC}}$ .

When the current limit is reached, the  $\text{GATE}^+$  pin voltage will be adjusted to maintain a constant voltage across the  $R_{\text{S}}^+$  resistor while the timer capacitor starts to charge. If the  $\text{TIMER}$  pin voltage exceeds 1.24V, the  $\text{GATE}^+$  pin will be pulled low.

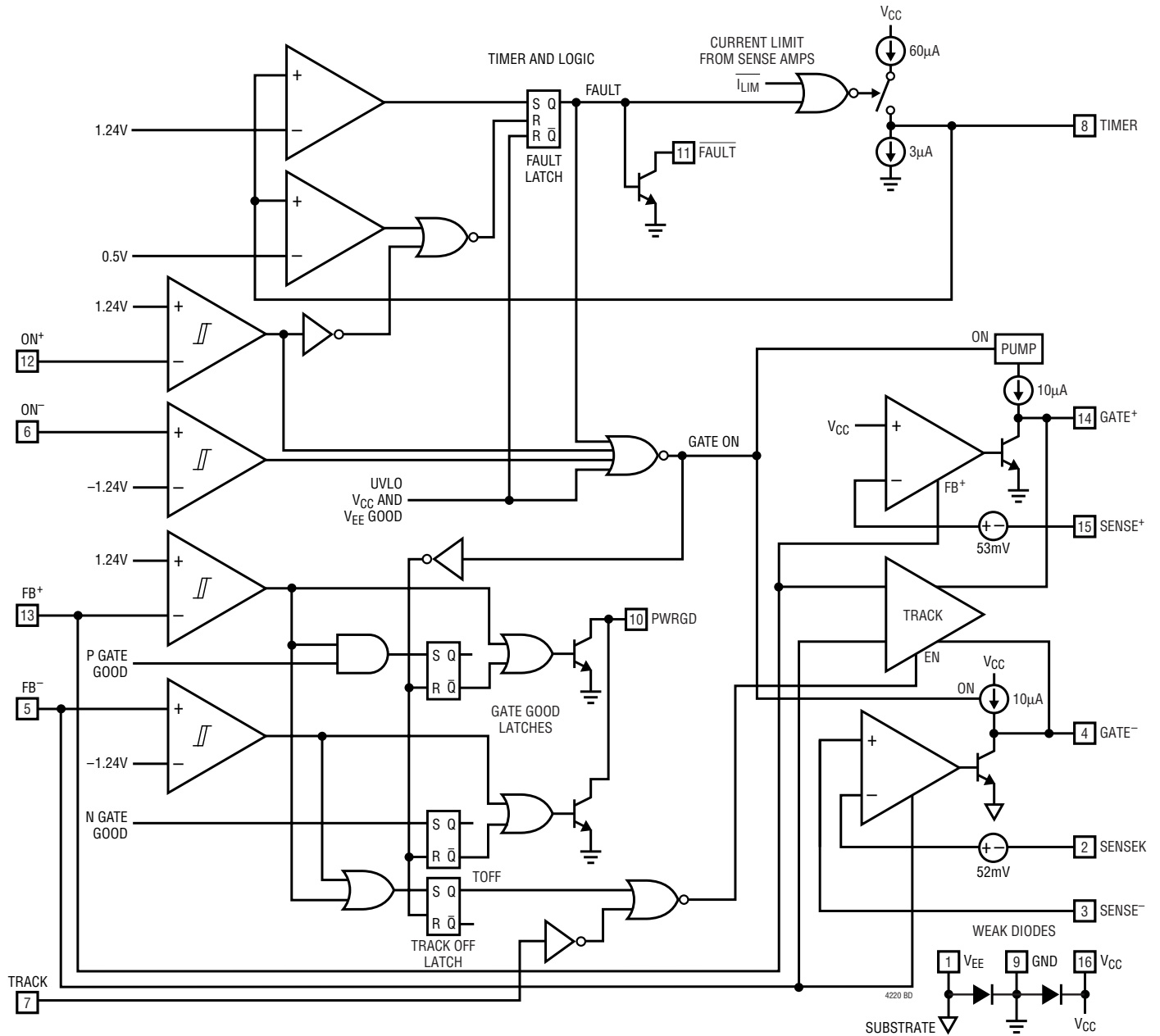
The  $\text{GATE}^+$  pin is pulled to GND whenever the  $\text{ON}^+$  pin is below 1.24V, the  $\text{ON}^-$  pin is above  $-1.24\text{V}$ , either supply is in the undervoltage lockout voltage range, or the  $\text{TIMER}$  pin rises above 1.24V.

**$\text{SENSE}^+$  (Pin 15):** Positive Supply Current Limit Sense Pin. A sense resistor must be placed in the supply path between  $V_{\text{CC}}$  and  $\text{SENSE}^+$ . The current limit circuit will regulate the voltage across the sense resistor to 50mV ( $V_{\text{CC}} - \text{SENSE}^+$ ) when the  $\text{FB}^+$  voltage is greater than 0.85V. If  $V_{\text{FB}^+}$  goes below 0.85V, the voltage across the sense resistor decreases linearly and stops at 15mV when  $V_{\text{FB}^+}$  is 0V.

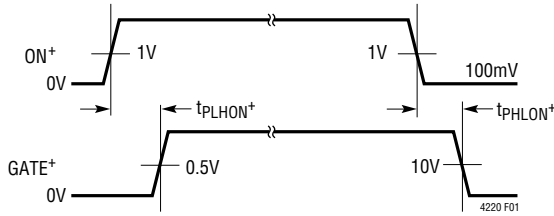
**$V_{\text{CC}}$  (Pin 16):** Positive Supply. The positive supply input ranges from 2.7V to 16.5V for normal operation.  $I_{\text{CC}}$  is typically 2.7mA. An internal undervoltage lockout circuit disables the chip for inputs less than 2.45V. Place a 0.1 $\mu\text{F}$  bypass capacitor next to the  $V_{\text{CC}}$  pin.



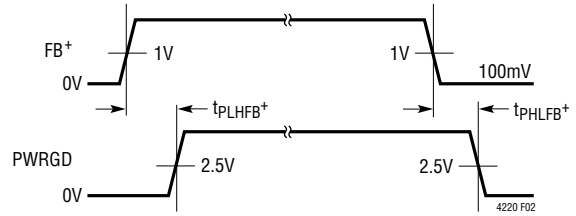
**BLOCK DIAGRAM**



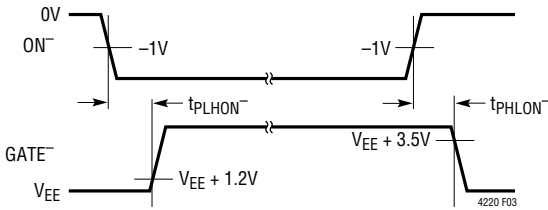
**TIMING DIAGRAMS**



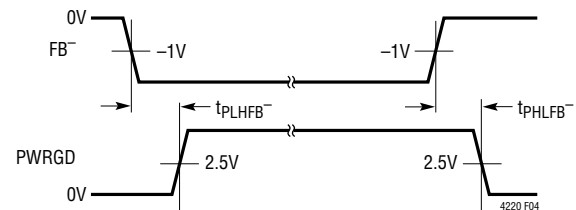
**Figure 1. ON<sup>+</sup>-to-GATE<sup>+</sup> Timing**



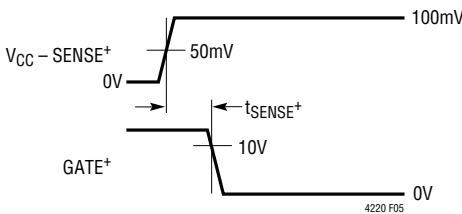
**Figure 2. FB<sup>+</sup>-to-PWRGD Timing**



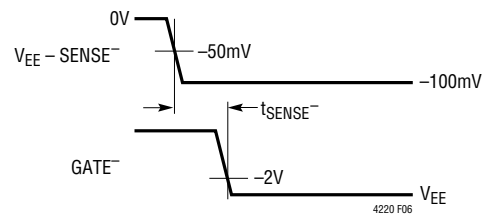
**Figure 3. ON<sup>-</sup>-to-GATE<sup>-</sup> Timing**



**Figure 4. FB<sup>-</sup>-to-PWRGD Timing**



**Figure 5. SENSE<sup>+</sup>-to-GATE<sup>+</sup> Timing**



**Figure 6. SENSE<sup>-</sup>-to-GATE<sup>-</sup> Timing**

**APPLICATIONS INFORMATION**

**Hot Circuit Insertion**

When circuit boards are inserted into a live backplane, the circuit board bypass capacitors can draw large peak currents from the backplane power bus as they charge up. The LT4220 is designed to turn on a board's  $\pm V$  dual supplies in a controlled manner, allowing the circuit board to be safely inserted or removed from a live backplane. The part provides supply tracking as well as undervoltage and overcurrent protection. Power good and fault output signals indicate, respectively, if both power output voltages are ready or if an overcurrent time-out fault has occurred.

The dual power supply on the circuit board is controlled with two external N-channel pass transistors Q1 and Q2 in the  $\pm V$  dual power supply path. The sense resistors  $R_{S+}$  and  $R_{S-}$  provide current detection while capacitor C1 and C2 control the  $V_{OUT+}$  and  $V_{OUT-}$  slew rate. Optionally, the TRACK pin can be tied to  $V_{CC}$  enabling the dual output voltages to ramp up together by tracking the voltages at the FB<sup>+</sup> and FB<sup>-</sup> pins. Resistors R6 and R8 provide current control loop compensation while R5 and R7 prevent high frequency oscillations in Q1 and Q2. C3 and R8 on Q2 prevent fast dV/dt transients from turning Q2 on during

## APPLICATIONS INFORMATION

live insertion. Resistive dividers R1, R2 and R3, R4 provide undervoltage sensing. Resistor dividers R9, R10 and R11, R12 provide a power good signal and control output voltage tracking when TRACK is enabled.

### Internal Supply Diodes

The LT4220 contains two internal diodes which clamp  $V_{EE}$  and  $V_{CC}$  with respect to GND in the event either supply pin is floating.  $V_{EE}$  is clamped one diode above GND and  $V_{CC}$  is clamped one diode below GND. The current through these diodes are designed to handle 10mA internal device current and should not be used for high load current conditions.

### Initial Power-Up Sequence

After the power pins first make contact, transistors Q1 and Q2 remain off. If the voltage at the  $ON^+$  and  $ON^-$  pins exceed the turn-on threshold voltage, the internal voltage on the  $V_{CC}$  and  $V_{EE}$  power pins exceed the undervoltage lockout threshold, and the timer pin voltage is less than 1.24V, the gate drive to transistors Q1 and Q2 will be turned on. The voltage on the  $GATE^+$  and  $GATE^-$  pins will be regulated to control the inrush current if the voltage across  $R_{S^+}$  or  $R_{S^-}$  exceeds the sense amplifier current limit threshold. If supply tracking is enabled, each gate will also be regulated to keep the magnitudes at the  $FB^+$  and  $FB^-$  pins within 50mV of each other.

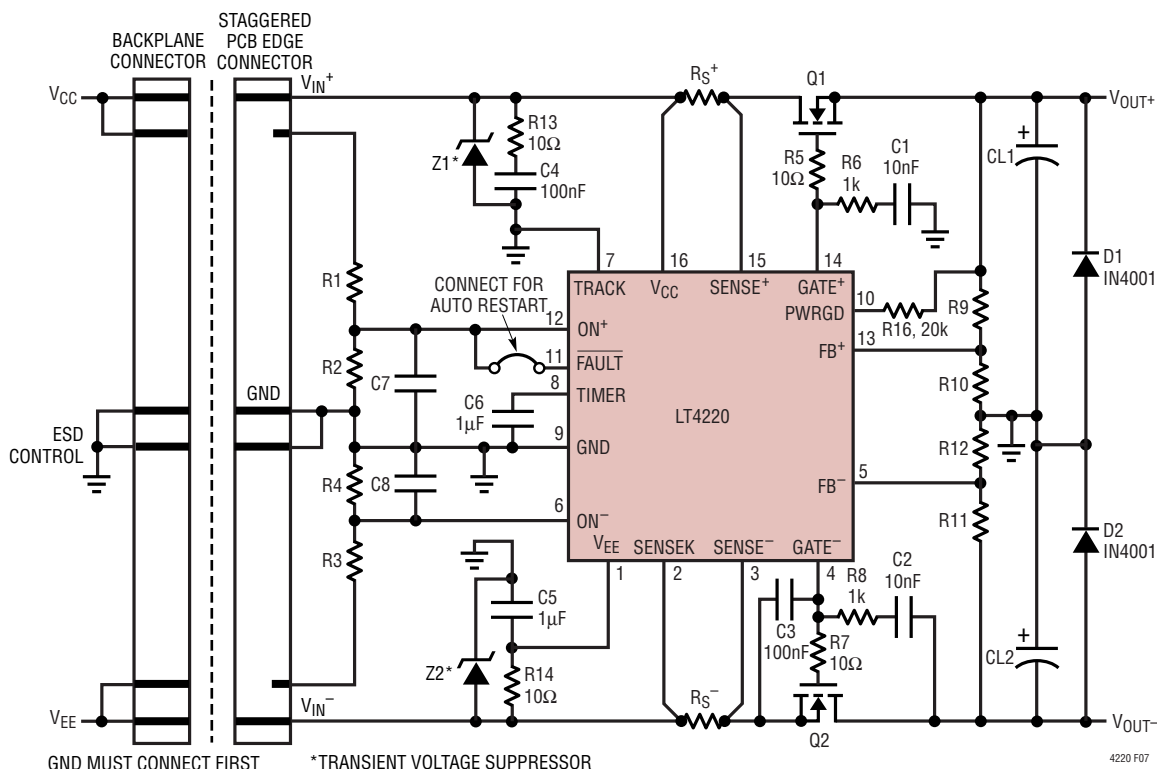


Figure 7. Hot Swap Controller on Daughter Board with Tracking Disabled

## APPLICATIONS INFORMATION

Whenever the output voltages reach their final value as sensed by R9, R10 and R11, R12 and both gate signals are fully on, the PWRGD pin will go high impedance.

A typical timing sequence is shown in Figure 8 with tracking enabled. The sequence is as follows:

- 1) The power pins make contact and the undervoltage lockout thresholds are exceeded.
- 2) The ON comparator thresholds are exceeded and the GATE pins start ramping up.  $V_{OUT+}$  follows  $GATE^+$  by the N-channel FET threshold voltage.
- 3)  $GATE^+$  is limited by the tracking circuit because  $V_{OUT-}$  lags behind  $V_{OUT+}$ . When  $V_{OUT-}$  starts ramping,  $GATE^-$  holds at approximately the threshold voltage of the N-channel FET due to C2 slew rate control.
- 4) When the magnitude of  $V_{OUT-}$  catches up with  $V_{OUT+}$ ,  $GATE^+$  resumes ramping. The slowest  $V_{OUT}$  will limit the faster  $V_{OUT}$  slew rate.
- 5)  $GATE^+$  internal gate good signal threshold is reached.
- 6)  $GATE^-$  internal gate good signal threshold is reached, enabling the FB output comparators. If both FB com-

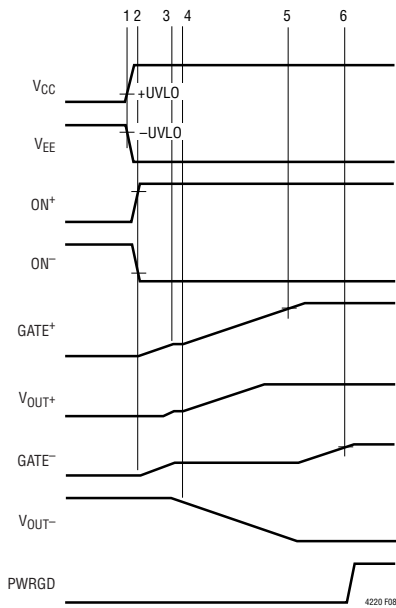


Figure 8. Typical Timing Sequence

parators indicate the output is good, the PWRGD pin output goes high impedance and is pulled up by an external pullup resistor.

### Power Supply Ramping

For large capacitive loads, the inrush current will be limited by the  $V_{OUT+}$  and  $V_{OUT-}$  slew rate or by the fold-back current limit. For a desired inrush current that is less than the fold-back current limit, the feedback networks R6, C1 and R8, C2 can be used to control the  $V_{OUT}$  slew rate. For the desired inrush current and typical gate pull-up current, the feedback network capacitors C1 and C2 can be calculated as:

$$C1 = (10\mu A \cdot CL1) / I_{INRUSH+} \text{ and} \tag{1}$$

$$C2 = (10\mu A \cdot CL2) / I_{INRUSH-} \tag{2}$$

where CL1 and CL2 are the positive and negative output load capacitance. If the supply-tracking mode is enabled (TRACK = High), during startup, the output with the slowest slew rate will also limit the slew rate of the opposite output (Note: Supply-tracking is also controlled by the resistive dividers on the FB pins. See Supply Tracking). Additionally, C1 and C2 should be greater than 5nF to prevent large overshoot in the output voltage for transient loads with small capacitive loads.

Capacitor C3 and resistor R8 prevent Q2 from momentarily turning on when the power pins first make contact. Without C3, capacitor C2 and  $C_{GD(Q2)}$  would hold the gate of Q2 near ground before the LT4220 could power up and pull the gate low. The minimum required value of C3 can be calculated by:

$$C3 = \left[ \frac{|V_{EE}| - V_{TH}}{V_{TH}} (C_{GD(Q2)} + C2) \right] \cdot 1.2 \tag{3}$$

where  $V_{TH}$  is the MOSFET's minimum gate threshold and  $V_{EEMAX}$  is the maximum negative supply input voltage. If C2 is not used, the minimum value for C3 should be 10nF to ensure stability. C2 and C3 must be the same type to ensure tracking over temperature.

## APPLICATIONS INFORMATION

### Current Limit/Electronic Circuit Breaker

The LT4220 features foldback current limit with an electronic circuit breaker that protects against short-circuits or excessive supply currents. The current limit is set by placing sense resistors between  $V_{CC}$  (Pin 16) and  $SENSE^+$  (Pin 15) and between  $SENSEK$  (Pin 2) and  $SENSE^-$  (Pin 3). An adjustable timer will trip an electronic circuit breaker if the part remains in current limit for too long.

To prevent excessive power dissipation in the pass transistors and to prevent voltage spikes on the input supply during overcurrent conditions at the output, the current folds back as a function of the output voltage, which is sensed at the feedback pins  $FB^+$  and  $FB^-$ . When the voltage at the  $FB^+$  (or  $FB^-$ ) pin is 0V, the sense amplifier offset is 15mV (–15mV), and limits the current to  $I_{LIMIT} = 15mV/R_S^+$  (–15mV/ $R_S^-$ ). As the output voltage increases, the sense amplifier offset increases until the  $FB^+$  (or  $FB^-$ ) voltage reaches 0.85V (–0.75V), At which point the current limit reaches a maximum of  $I_{LIMIT} = 48mV/R_S^+$  (–52mV/ $R_S^-$ ).

### Timer Function and Autorestart

The TIMER pin (Pin 8) provides a method for setting the maximum time the LT4220 is allowed to operate in current limit. When the current limit circuitry is not active, the TIMER pin is pulled to GND by a 3.3 $\mu$ A current sink. Whenever the current limit circuit becomes active, by either a positive or negative sense amplifier operating in current limit, a 65 $\mu$ A pull-up current source is connected to the TIMER pin and the voltage rises with a slope equal to  $dV/dt = 65\mu A/C_{TIMER}$ . The desired current limit time (t) can be set with a capacitor value of:

$$C_{TIMER} = t \cdot 65\mu A/1.24V \quad (4)$$

If the current limit circuit turns off, the TIMER pin will be discharged to GND at a rate of:

$$dV/dt = 3.3\mu A/C_{TIMER} \quad (5)$$

Whenever the TIMER pin ramps up and reaches the 1.24V threshold, the internal fault latch is set and the  $\overline{FAULT}$  pin (Pin 11) is pulled low.  $GATE^+$  is pulled down to ground,  $GATE^-$  is pulled down to  $V_{EE}$ , and the TIMER pin starts ramping back to GND by the 3.3 $\mu$ A current sink. After the

fault latch is set, the LT4220 can be restarted by pulling the  $ON^+$  pin low after the TIMER pin falls below 0.5V. The LT4220 can also be restarted by cycling either supply beyond its UVLO. Otherwise the part remains latched off.

For autorestart, the  $\overline{FAULT}$  pin can be tied to the  $ON^+$  pin. The autorestart will occur after the TIMER pin falls below 0.5V.

### Undervoltage Detection

The  $ON^+$  and  $ON^-$  pins can be used to detect an undervoltage condition at the power supply inputs. The  $ON^+$  and  $ON^-$  pins are connected to analog comparators with 50mV of hysteresis. If the  $ON^+$  pin falls below its threshold voltage or the  $ON^-$  pin rises above its threshold voltage, the GATE pins are pulled low and held low until the  $ON^+$  and  $ON^-$  pins exceed their turn-on thresholds (1.24V and –1.24V). External capacitance at the ON pins may be required to filter supply ringing from crossing the ON comparator threshold.

Additionally there is an internal undervoltage lockout on both supplies of approximately  $V_{CC} < 2.45V$  and  $V_{EE} > -2.45V$ . If either supply is in UVLO, both GATE pins will be pulled low and all internal latches will be reset.

### $ON^-$ Protection

If the  $ON^-$  pin is driven directly and not connected to the negative supply through a resistor divider, a 10k resistor must be connected between the driver and the  $ON^-$  pin.

### Power Good Detection

The LT4220 includes two comparators for monitoring the output voltages. The  $FB^+$  and the  $FB^-$  pins are compared against 1.24V and –1.24V internal references respectively. The comparators exhibit 50mV of hysteresis. The comparator outputs are wire-ORed to the open collector PWRGD pin that is enabled once both  $GATE^+$  and  $GATE^-$  pins have reached their maximum gate drive voltage as indicated by the internal gate good latches. The PWRGD pin goes high impedance when both  $FB^+$  and  $FB^-$  inputs exceed  $V_{FB+H}$  and  $V_{FB-H}$  thresholds,  $GATE^+$  is fully on and  $GATE^-$  initially has been fully on.

## APPLICATIONS INFORMATION

### Supply Tracking

If the TRACK pin (Pin 7) is high the supply power-up tracking mode is enabled. This feature forces both supplies to reach their final value at the same time, during power-up and for faults that drive the output supplies to zero. During this mode the GATE pins are controlled to keep the differential magnitude of the FB pins to within 50mV. The FB pins are scaled versions of the output voltages. Therefore, control of the FB pins, via the GATE pins, will control the output voltages at the same scale.

$$|\Delta V_{FB(TRK)}| = |V_{FB^+} - V_{FB^-}| \quad (6)$$

Supply tracking will continue until: either FB pin reaches the associated PWRGD threshold. If any fault condition occurs that turns the GATE pins off, supply tracking will be reenabled. The GATE off conditions include: (1) either ON pin detects undervoltage, (2) internal undervoltage lock-out, (3) the fault latch is set by a current limit time-out.

### V<sub>EE</sub> Bypassing

The V<sub>EE</sub> supply pin should be filtered with an RC network to reduce high dV/dt slew rates from disturbing internal circuits. Typical RC bypassing sufficient to prevent circuit misbehavior is R14 = 10Ω and C5 = 1μF. The GATE<sup>-</sup>, SENSEK and SENSE<sup>-</sup> pins have been designed such that they can be pulled below or above V<sub>EE</sub> for short periods of time while the V<sub>EE</sub> pin is reaching its steady state voltage. If desired, a higher R14 • C5 time constant may be used to prevent short circuit transients from tripping the V<sub>EE</sub> undervoltage lockout circuit at -2.45V. R14 should be sufficient to decouple C5 from causing transients on V<sub>IN-</sub> during live insertion.

Under the condition of a short circuit on V<sub>OUT-</sub>, parasitic inductance and resistance in the V<sub>IN-</sub> path will cause V<sub>IN-</sub> to collapse toward 0V causing the V<sub>EE</sub> pin voltage to also discharge toward 0V before the external FET can be turned off (typically 7μs to 10μs). To prevent a UVLO condition from occurring, the R14 • C5 time constant should be sufficient to hold the V<sub>EE</sub> pin voltage out of the V<sub>EE</sub> UVLO voltage range. If the V<sub>EE</sub> pin reaches its UVLO voltage, GATE<sup>+</sup> will also be pulled low. For the case where C3 is large, causing an even slower N-channel FET turnoff, higher RC bypassing may be necessary to prevent tripping the V<sub>EE</sub> UVLO.

### ON<sup>+</sup>, ON<sup>-</sup> Bypass Capacitors

Bypass capacitors are required from ON<sup>+</sup> to ground and ON<sup>-</sup> to ground. A typical time constant is:

$$TC (ON^+) = (R1||R2)C7 = 44\mu s$$

$$TC (ON^-) = (R3||R4)C8 = 44\mu s$$

### Supply Ringing

Normal circuit design practice calls for capacitive bypassing of the input supply to active devices. The opposite is true for Hot Swap circuits that are connected into a backplane, where capacitive loading would cause transients during an abrupt connection to the backplane. With little or no capacitive decoupling on the powered side of the N-channel FETs, connection transients or load transients will typically cause ringing on the supply leads due to parasitic inductance. It is recommended to use a snubber circuit comprising of a series 10Ω and 0.1μF capacitor to dampen transient ringing. The supply decoupling circuit on the V<sub>EE</sub> pin also provides a snubber for V<sub>IN-</sub>.

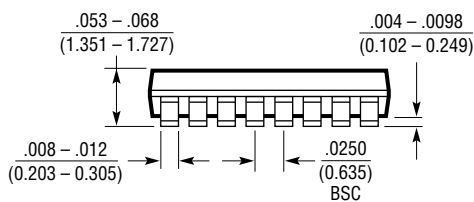
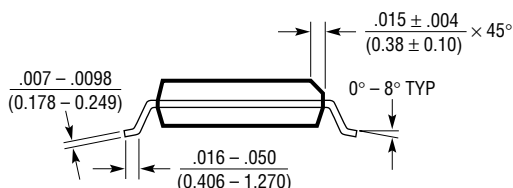
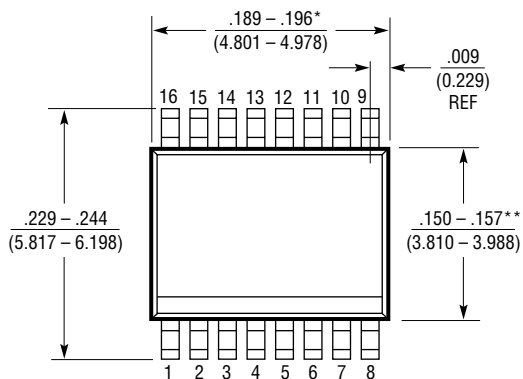
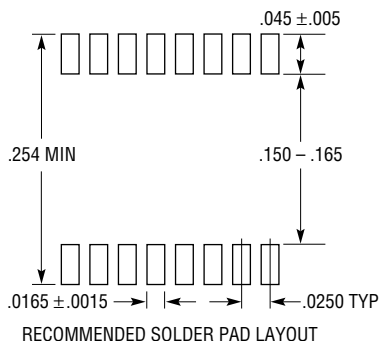
Additionally, if the supply voltage overshoot can exceed the ±22V maximum rating on the part, a transient voltage suppressor is recommended. Voltage transients can occur during load short-circuit conditions, where parasitic inductance in the supply leads can build up energy before the external N-channel FET can be turned off. This is especially true for the negative side FET where a large C3 value slows the turn off of the N-channel FET. Subsequent overshoot when the FET is finally turned off can be as much as 2× the supply voltage even with the snubber circuit. Additional protection using a transient suppressor may be needed to prevent exceeding the maximum supply voltage rating.

### Supply Reversal Protection

A variety of conditions on V<sub>OUT+</sub> and V<sub>OUT-</sub> may result in supply reversal. To protect devices connected to V<sub>OUT+</sub> and V<sub>OUT-</sub> protection diodes should be used. 1N4001 diodes can be used for most applications. Connection of these diodes (D1, D2) are shown in the front page Typical Application.

# PACKAGE DESCRIPTION

## GN Package 16-Lead Plastic SSOP (Narrow .150 Inch) (Reference LTC DWG # 05-08-1641)



NOTE:

1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN  $\frac{\text{INCHES}}{\text{MILLIMETERS}}$
3. DRAWING NOT TO SCALE

\*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

\*\*DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

GN16 (SSOP) 0502

TYPICAL APPLICATION

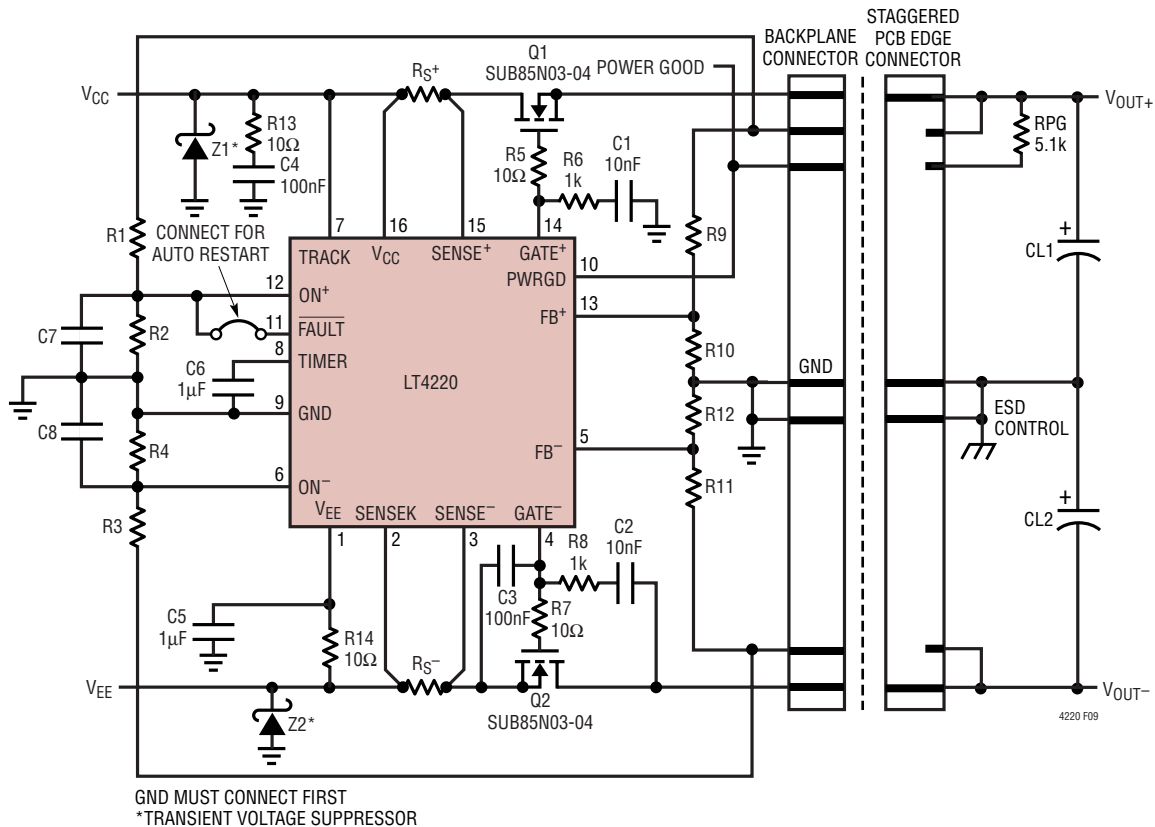


Figure 9. Hot Swap Controller on Mainboard with Tracking

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC®1421	Dual Hot Swap Controller	Two Circuit Breakers for Supplies from 3V to 12V and Supports -12V
LTC1422	Single Hot Swap Controller in SO-8	Operates from 3V to 12V
LTC1645	Dual Hot Swap Controller	Operates from 1.2V to 12V, Allows Supply Sequencing
LTC1647	Dual Hot Swap Controller	Operates from 2.7V to 16.5V, Separate ON Pins
LTC4211	Single Hot Swap Controller with Multifunction Current Control	2.5V to 16.5V, Active Inrush Limiting, Fast Comparator
LTC4230	Triple Hot Swap Controller with Multifunction Current Control	1.7V to 16.5V, Active Inrush Limiting, Fast Comparator