

Absolute Maximum Ratings (Notes 1, 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage, V_{CC}	+90V
Bias Voltage, V_{BB}	+16V
Input Voltage, V_{IN}	0V to 4.5V
Storage Temperature Range, T_{STG}	-65°C to +150°C
Lead Temperature (Soldering, <10sec.)	300°C
ESD Tolerance, Human Body Model	2kV

Limits of Operating Ranges (Note 2)

V_{CC}	+60V to +85V
V_{BB}	+8V to 15V
V_{IN}	0V to +3.75V
V_{OUT}	+15V to +75V
Case Temperature	-20°C to +115°C

Do not operate the part without a heat sink.

Electrical Characteristics

(See Figure 3 for Test Circuit)

Unless otherwise noted: $V_{CC} = +80V$, $V_{BB} = +12V$, $C_L = 8pF$, $T_C = 50^\circ C$.

DC Tests: $V_{IN} = +2.25VDC$

AC Tests: Output = 40V_{PP} (25V - 65V) at 1MHz

Symbol	Spec Parameter	Conditions	Min	Typ	Max	Units
I_{CC}	Supply Current	Three Channels, No Input Signal, No Output Load		18	25	mA
I_{BB}	Bias Current	All three Channels		14	20	mA
V_{OUT}	DC Output Voltage	No AC Input Signal, $V_{IN} = 1.25V$	62	65	68	V_{DC}
A_V	DC Voltage Gain	No AC Input Signal	-18	-20	-22	
ΔA_V	Gain Matching	Note 4, No AC Input Signal		1.0		dB
LE	Linearity Error	Note 4, 5, No AC Input Signal		5		%
t_R	Rise Time	Note 6, 10% to 90%		14		nS
t_F	Fall Time	Note 6, 90% to 10%		14		nS
OS	Overshoot	Note 6		1		%

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur.

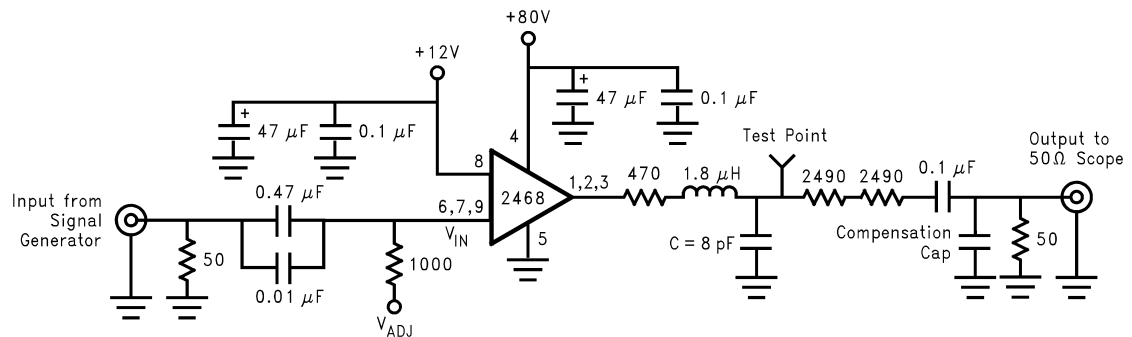
Note 2: Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and the test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may change when the device is not operated under the listed test conditions.

Note 3: All voltages are measured with respect to GND, unless otherwise specified.

Note 4: Calculated value from Voltage Gain test on each channel.

Note 5: Linearity Error is the variation in DC Gain from $V_{in} = 1.0$ volts to $V_{in} = 3.5$ volts.

Note 6: Input from signal generator: $t_R, t_F < 1nS$.

AC Test Circuit

DS200135-3

Note 7: 8 pF load includes parasitics and FET probe (if used).

Note 8: The heatsink must be grounded.

Note 9: Compensation Cap is chosen for good correlation to FET probe.

Note 10: Input and output cables should be low loss 50Ω coax, less than 1M long.

FIGURE 3. Test Circuit (One Channel)

Typical Performance Characteristics ($V_{CC} = +80V_{DC}$, $V_{BB} = +12V_{DC}$, $C_L = +8pF$, $V_{OUT} = 40V_{PP}$ (25-65V), Test Circuit - *Figure 3* unless otherwise specified.

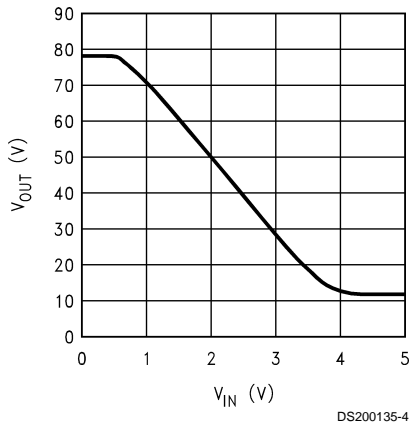


FIGURE 4. V_{out} vs V_{in}

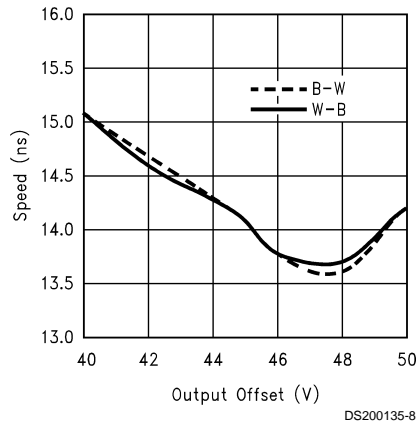


FIGURE 7. Speed vs Offset

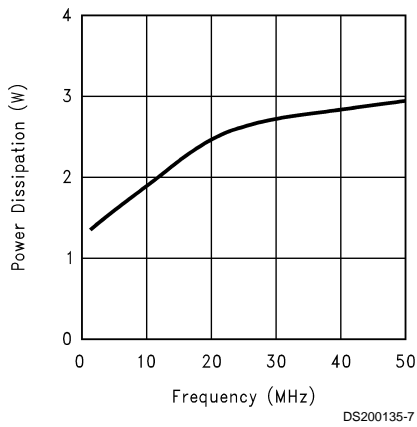


FIGURE 5. Power Dissipation vs Frequency

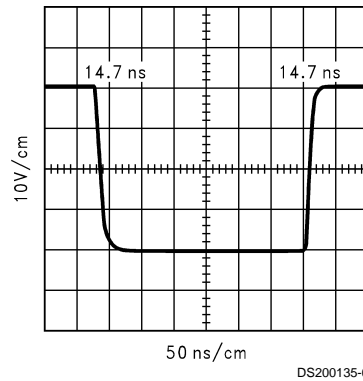


FIGURE 8. LM2468 Pulse Response

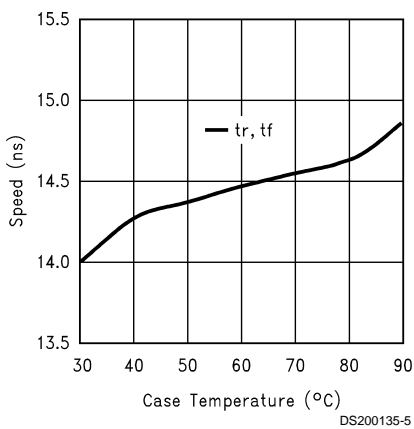


FIGURE 6. Speed vs Temperature

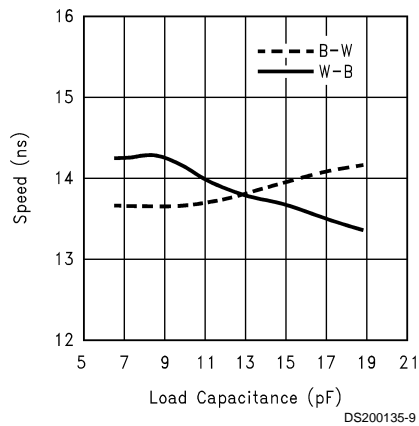


FIGURE 9. Speed vs Load Capacitance

THEORY OF OPERATION

The LM2468 is a high voltage monolithic three channel CRT driver suitable for color monitor applications. The LM2468 operates with 80V and 12V power supplies. The part is housed in the industry standard 9-lead TO-220 molded plastic power package.

The circuit diagram of the LM2468 is shown in *Figure 1*. The PNP emitter follower, Q5, provides input buffering. Q1 and Q2 form a fixed gain cascode amplifier with resistors R1 and R2 setting the gain at -20. Emitter followers Q3 and Q4 isolate the high output impedance of the amplifier from the capacitive load on the output of the amplifier, decreasing the sensitivity of the device to changes in load capacitance. Q6 provides biasing to the output emitter follower stage to reduce crossover distortion at low signal levels.

Figure 2 gives the pinout of the LM2468.

Figure 3 shows a typical test circuit for evaluation of the LM2468. This circuit is designed to allow testing of the LM2468 in a 50Ω environment without the use of an expensive FET probe. In this test circuit, two low inductance resistors in series totalling 4.95KΩ form a 200:1 wideband, low capacitance probe when connected to a 50Ω load (such as 50Ω oscilloscope input). The input signal from the generator is AC coupled to the base of Q5.

APPLICATION HINTS

INTRODUCTION

National Semiconductor (NSC) is committed to provide application information that assists our customers in obtaining the best performance possible from our products. The following information is provided in order to support this commitment. The reader should be aware that the optimization of performance was done using a specific printed circuit board designed at NSC. Variations in performance can be realized due to physical changes in the printed circuit board and the application. Therefore, the designer should know that component value changes might be required in order to optimize performance in a given application. The values shown in this document can be used as a starting point for evaluation purposes. When working with high bandwidth circuits, good layout practices are always critical to achieving maximum performance.

IMPORTANT INFORMATION

The LM2468 performance is targeted for the VGA (640 x 480) to XGA (1024 x 768, 60Hz refresh) resolution market. It is designed to be a replacement for discrete CRT drivers. The application circuits shown in this document to optimize performance and to protect against damage from CRT arc-over are designed specifically for the LM2468. If another member of the LM246X family is used, please refer to its datasheet.

POWER SUPPLY BYPASS

Since the LM2468 is a wide bandwidth amplifier, proper power supply bypassing is critical for optimum performance. Improper power supply bypassing can result in large overshoot, ringing or oscillation. A 0.1μF capacitor should be connected from the supply pin, V_{CC} , to ground, as close to the supply and ground pins as is practical. Additionally, a 10μF to 100μF electrolytic capacitor should be connected from the supply pin to ground. The electrolytic capacitor should also be placed reasonably close to the LM2468's

supply and ground pins. A 0.1μF capacitor should be connected from the bias pin (V_{bb}) to the ground, as close as is practical to the part.

ARC PROTECTION

During normal CRT operation, internal arcing may occasionally occur. Spark gaps, in the range of 200V, connected from the CRT cathodes to CRT ground will limit the maximum voltage, but to a value that is much higher than allowable on the LM2468. This fast, high voltage, high energy pulse can damage the LM2468 output stage. The application circuit shown in *Figure 10* is designed to help clamp the voltage at the output of the LM2468 to a safe level. The clamp diodes, D1 and D2, should have a fast transient response, high peak current rating, low series impedance and low shunt capacitance. FDH400 or equivalent diodes are recommended. Do not use 1N4148 diodes for the clamp diodes. D1 and D2 should have short, low impedance connections to V_{CC} and ground respectively. The cathode of D1 should be located very close to a separately decoupled bypass capacitor (C3 in *Figure 10*). The ground connection of D2 and the decoupling capacitor should be very close to the LM2468 ground. This will significantly reduce the high frequency voltage transients that the LM2468 would be subjected to during an arc-over condition. Resistor R2 limits the arc-over current that is seen by the diodes while R1 limits the current into the LM2468 as well as the voltage stress at the outputs of the device. R2 should be a 1/2W solid carbon type resistor. R1 can be a 1/4W metal or carbon film type resistor. Having large value resistors for R1 and R2 would be desirable, but has the effect of increasing rise and fall times. Inductor L1 is critical to reduce the initial high frequency voltage levels that the LM2468 would be subjected to. The inductor will not only help protect the device, but will also help optimize rise and fall times as well as minimize EMI. For proper arc protection, it is important to not omit any of the arc protection components shown in *Figure 10*.

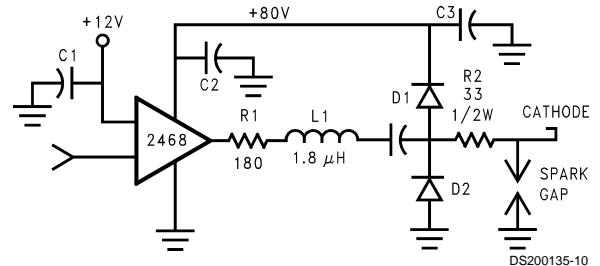


FIGURE 10. One Video Channel of the LM2468 with the Recommended Arc Protection Circuit

OPTIMIZING TRANSIENT RESPONSE

Referring to *Figure 10*, there are three components (R1, R2 and L1) that can be adjusted to optimize the transient response of the application circuit. Increasing the values of R1 and R2 will slow the circuit down while decreasing overshoot. Up to a point, increasing the value of L1 will speed up the circuit as well as increase overshoot. It is very important to use inductors with very high self-resonant frequencies, preferably above 300 MHz. Ferrite core inductors from J.W. Miller Magnetics (part # 78FR39K) were used for optimizing the performance of the device in the NSC application board. The values shown in *Figure 10* can be used as a good starting point for the evaluation of the LM2468. If needed, additional damping can be provided by adding a resistor in parallel with L1 to help control overshoot. Using variable

APPLICATION HINTS (Continued)

resistors for R1 will simplify finding the values needed for optimum performance in a given application. Once the optimum value is determined, the variable resistors can be replaced with fixed values.

Effect of Load Capacitance

Figure 9 shows the effect of increased load capacitance on the speed of the device. This demonstrates the importance of knowing the load capacitance in the application.

Effect of Offset

Figure 7 shows the variation in rise and fall times when the output offset of the device is varied from 40VDC to 50VDC. The rise and fall times shows a maximum variation relative to the center data point (45VDC) of about 7%.

THERMAL CONSIDERATIONS

Figure 6 shows the performance of the LM2468 video amplifiers in the test circuit shown in Figure 3 as a function of case temperature. The figure shows that the rise time of the LM2468 increases by approximately 9% as the case temperature increases from 30°C to 100°C. This corresponds to a speed degradation of 1.3% for every 10°C rise in case temperature. The fall time degrades around 0.6% for every 10°C in case temperature.

Figure 5 shows the maximum power dissipation of the LM2468 vs. Frequency when all three channels of the device are driving an 8pF load with a 40 V_{p-p} signal alternating one pixel on, one pixel off. The graph assumes a 72% active time (device operating at the specified frequency) which is typical in a monitor application. The other 28% of the time the device is assumed to be sitting at the black level (65V in this case). This graph gives the designer the information needed to determine the heat sink requirement for his application. The designer should note that if the load capacitance is increased, the AC component of the total power dissipation will also increase.

The LM2468 case temperature must be maintained below 115°C. If the maximum expected ambient temperature is 70°C and the maximum power dissipation is 2.95W (from Figure 5, 50 MHz bandwidth), then a maximum heat sink thermal resistance can be calculated:

$$R_{TH} = \frac{115^{\circ}\text{C} - 70^{\circ}\text{C}}{2.95\text{W}} = 15.3^{\circ}\text{C}/\text{W}$$

This example assumes a capacitive load of 8pF and no resistive load.

TYPICAL APPLICATION

A typical application of the LM2468 is shown in Figures 11, 12. Used in conjunction with an LM1269 coupled with an LM2479/2480 bias clamp, a complete video channel from monitor input to CRT cathode can be achieved. Performance is ideal for 1024x768 resolution displays with pixel clock frequencies up to 50 MHz. Figures 11, 12 are the schematic for the NSC demonstration board that can be used to evaluate the LM1269/2468 combination in a monitor.

PC Board Layout Considerations

For optimum performance, an adequate ground plane, isolation between channels, good supply bypassing and the minimization of unwanted feedback are necessary. Also, the length of the signal traces from the preamplifier to the

LM2468 and from the LM2468 to the CRT cathode should be as short as possible. The following references are recommended:

Ott, Henry W., "Noise Reduction Techniques in Electronic Systems", John Wiley & Sons, New York, 1976.

"Video Amplifier Design for Computer Monitors", National Semiconductor Application Note 1013.

Pease, Robert A., "Troubleshooting Analog Circuits", Butterworth-Heinemann, 1991.

Because of its high small signal bandwidth, the part may oscillate in a monitor if feedback occurs around the video channel through the chassis wiring. To prevent this, leads to the video amplifier input circuit should be shielded, and input wiring should be spaced as far as possible from output circuit wiring.

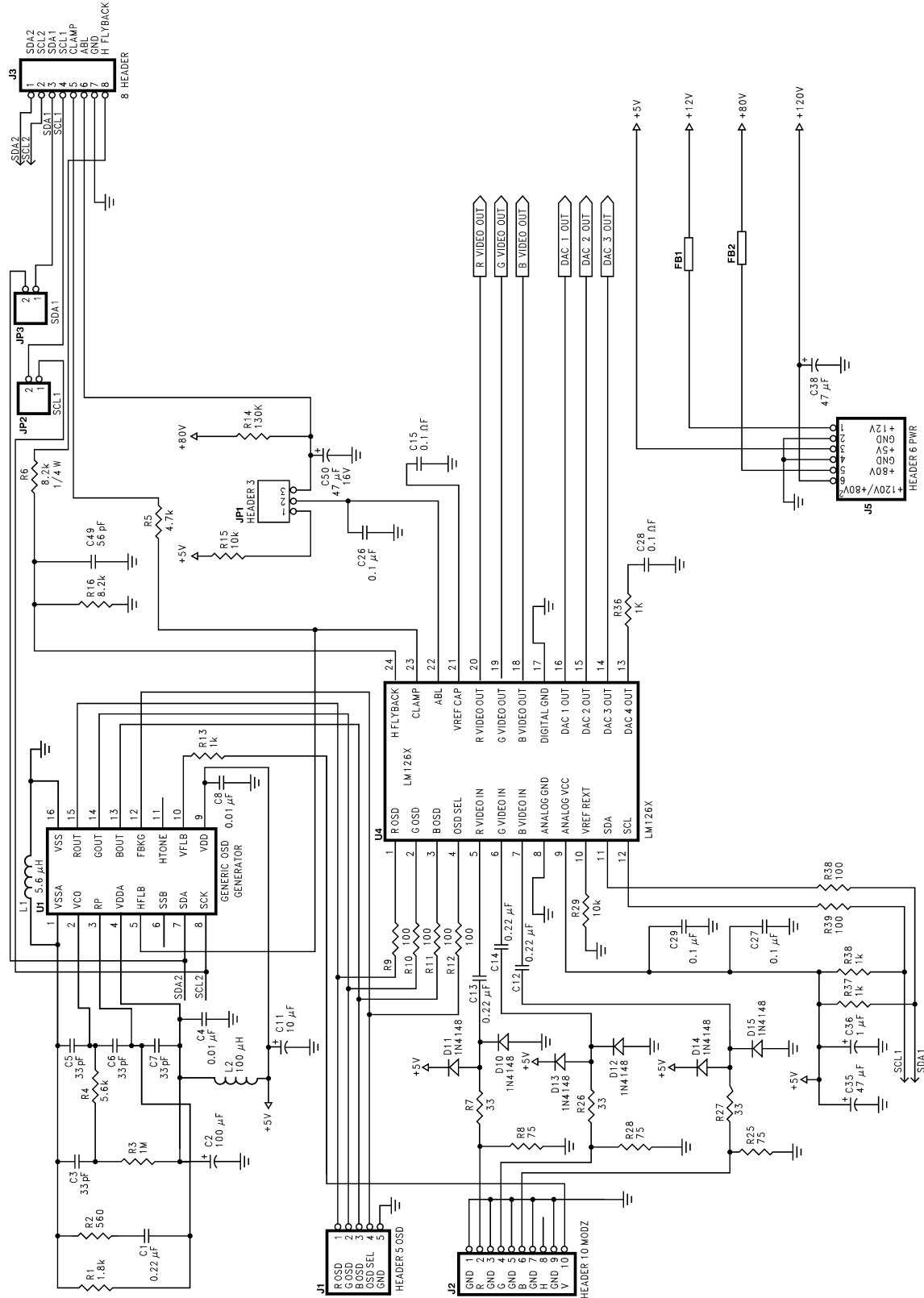
NSC Demonstration Board

Figure 13 shows the routing and component placement on the NSC LM126X/246X demonstration board. The schematic of the board is shown in Figures 11, 12. This board provides a good example of a layout that can be used as a guide for future layouts. Note the location of the following components:

- C16, C19—V_{CC} bypass capacitor, located very close to pin 4 and the ground plane near the device.
- C20—V_{BB} bypass capacitors, located close to pin 8 and ground.
- C46, C47, C48—V_{CC} bypass capacitors, near LM2468 V_{CC} clamp diodes. Very important for arc protection.

The routing of the LM2468 video outputs to the CRT is very critical to achieving optimum performance. Figure 13 shows the routing and component placement from pin 3 of the LM2468 to the blue cathode. Note that the components are placed so that they almost line up from the output pin of the LM2468 to the blue cathode pin of the CRT connector. This is done to minimize the length of the video path between these two components. Note also that D8, D9, R24, and D6 are placed to minimize the size of the video nodes that they are attached to. This minimizes parasitic capacitance in the video path and also enhances the effectiveness of the protection diodes. The anode of protection diode D8 is connected directly to a section of the ground plane that has a short and direct path to the LM2468 ground pins. The cathode of D9 is connected to V_{CC} very close to decoupling capacitor C48 (near the center of Figure 13), which is connected to the same section of the ground plane as D8. The diode placement and routing is very important for minimizing the voltage stress on the LM2468 video outputs during an arc over event. Lastly, notice that S3 is placed very close to the blue cathode and is tied directly to the ground under the CRT connector.

APPLICATION HINTS (Continued)

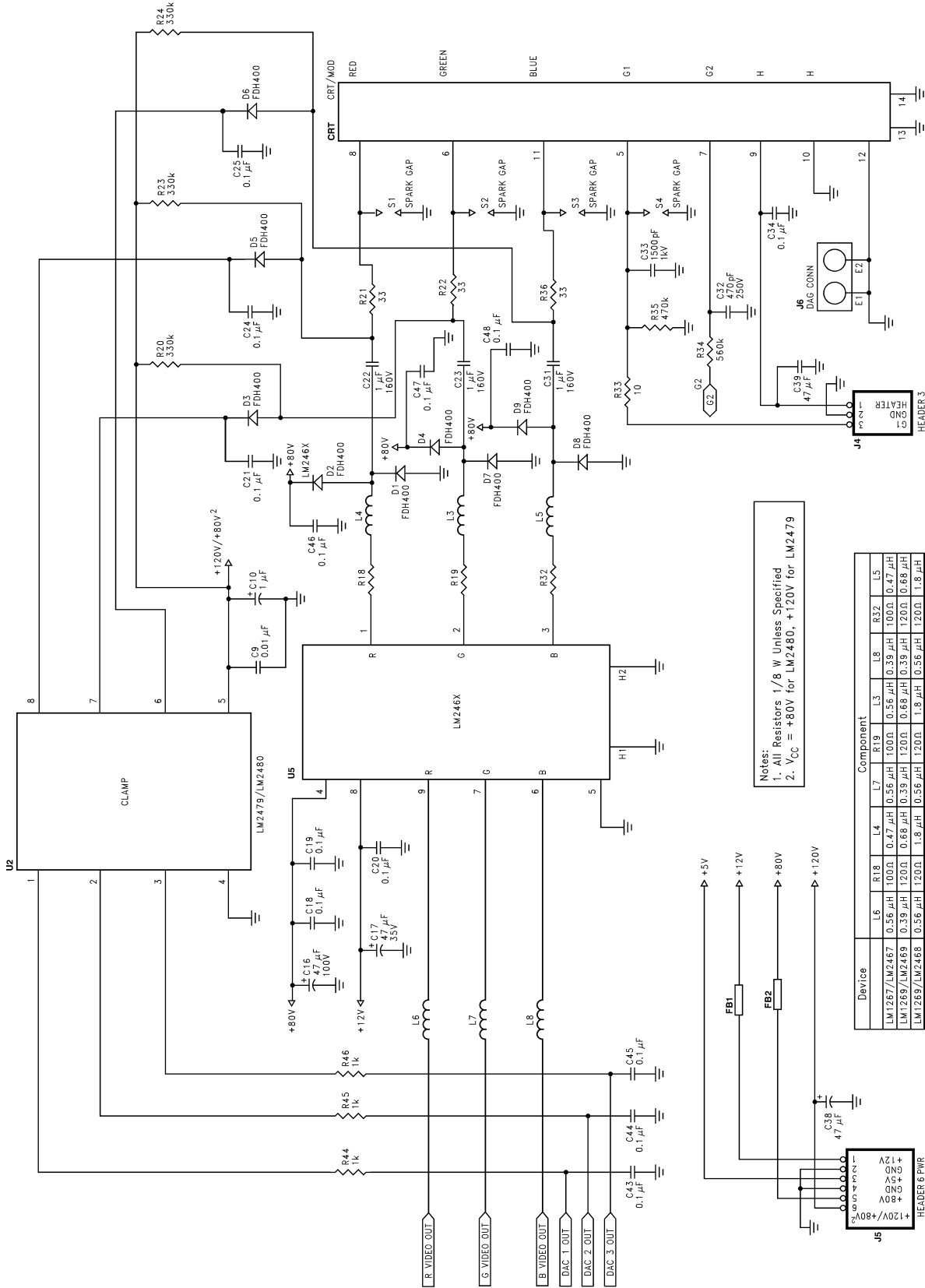


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FIGURE 11. LM1269/2468 Demonstration Board Schematic

APPLICATION HINTS (Continued)

LM2468



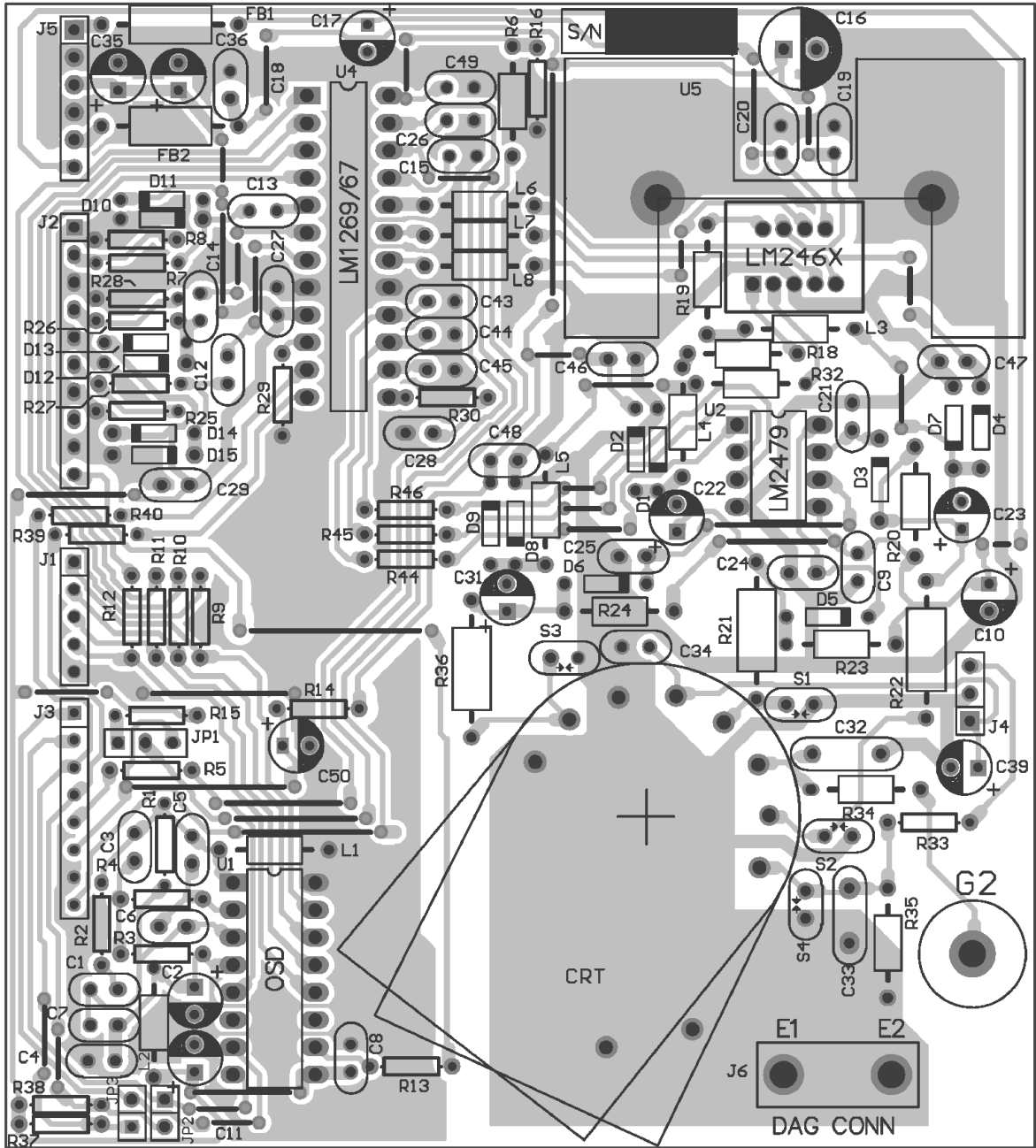
Notes:
 1. All Resistors 1/8 W Unless Specified
 2. V_{CC} = +80V for LM2480, +120V for LM2479

Device	L6	R18	L4	L7	R19	L3	L8	R32	L5
LM1267/LM2467	0.56 μH	100Ω	0.47 μH	0.56 μH	100Ω	0.39 μH	100Ω	0.47 μH	0.47 μH
LM1269/LM2469	0.39 μH	120Ω	0.66 μH	0.39 μH	120Ω	0.68 μH	0.39 μH	120Ω	0.68 μH
LM1269/LM2468	0.56 μH	120Ω	1.8 μH	0.56 μH	120Ω	1.8 μH	0.56 μH	120Ω	1.8 μH

FIGURE 12. LM1269/2468 Demonstration Board Schematic (continued)

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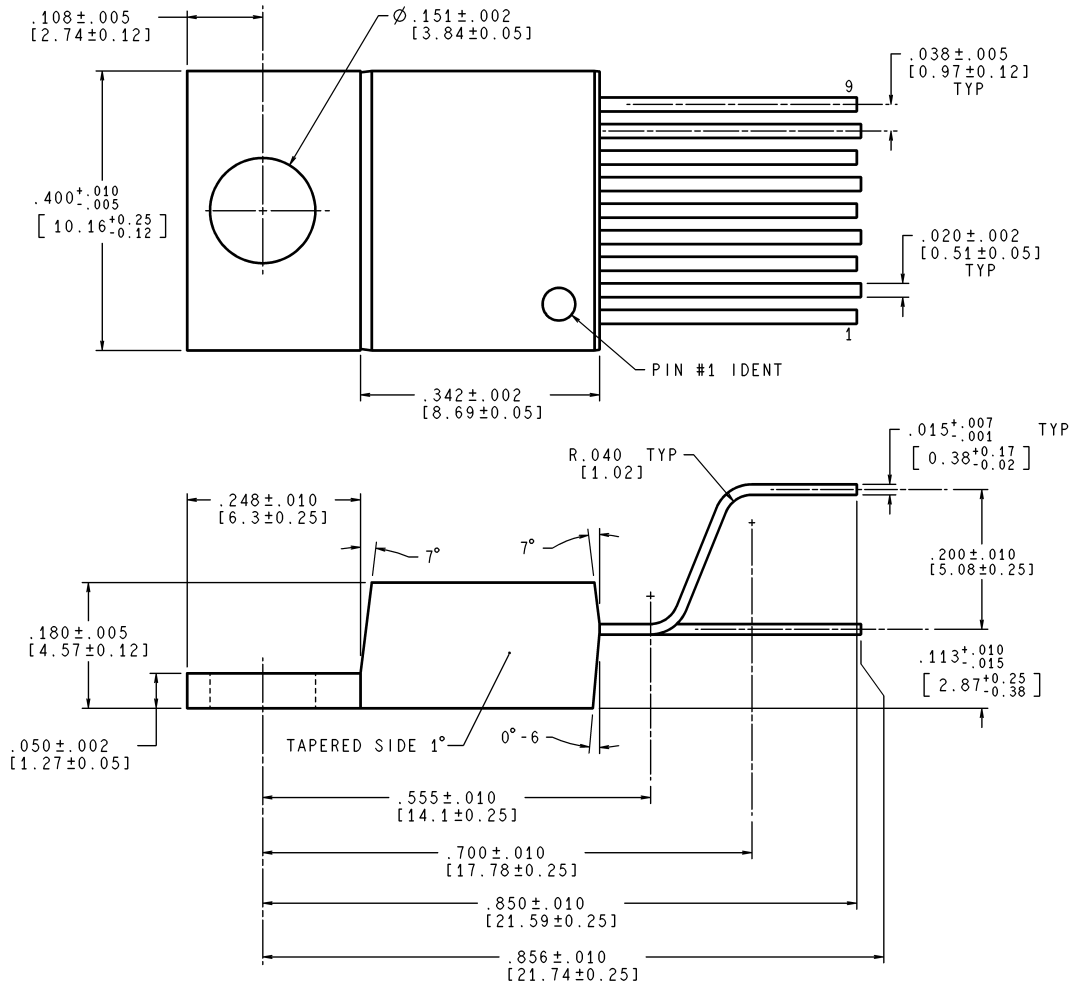
APPLICATION HINTS (Continued)



DS200135-17

FIGURE 13. NSC LM126X/246X Demo Board Layout

Physical Dimensions inches (millimeters) unless otherwise noted



CONTROLLING DIMENSION IS INCH
VALUES IN [] ARE MILLIMETERS

TA09A (Rev C)

Note: Information contained in this data sheet is preliminary and may be subject to change without notice.

NS Package Number TA09A
Order Number LM2468TA

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