National Semiconductor

April 1990

# MM58201 Multiplexed LCD Driver

## General Description

The MM58201 is a monolithic CMOS LCD driver capable of driving up to 8 backplanes and 24 segments. A 192-bit RAM stores the data for the display. Serial input and output pins are provided to interface with a controller. An RC oscillator generates the timing necessary to refresh the display. The magnitude of the driving waveforms can be adjusted with the $V_{TC}$ input to optimize display contrast. Four additional bits of RAM allow the user to program the number of backplanes being driven, and to designate the driver as either a master or slave for cascading purposes. When two or more drivers are cascaded, the master chip drives the backplane lines, and the master and each slave chip drive 24 segment lines. Synchronizing the cascaded drivers is accomplished by tying the RC OSC pins together and the BP1 pins together.

The MM58201 is packaged in a 40-lead dual-in-line package, or 44 lead plastic chip carrier package.

## Features

- Drives up to 8 backplanes and 24 segment lines
- Stores data for display
- Cascadable
- Low power
- Fully static operation

## Applications

- Dot matrix LCD driver
- Multiplexed 7-segment LCD driver
- Serial in/Serial out memory

## Block Diagram

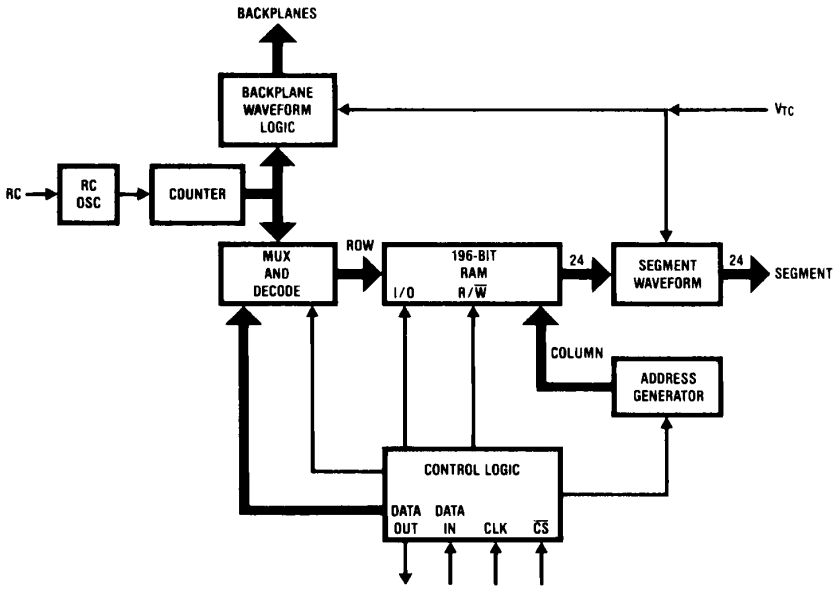


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**FIGURE 1**

RRD-B30M105/Printed in U. S. A.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Voltage at Any Pin | $V_{SS}$ −0.3V to $V_{SS}$ +18V |
| Operating Temperature Range | 0°C to 70°C |
| Storage Temperature Range | −65°C to +150°C |

| | |
|---|---|
| Power Dissipation at 25°C | |
| Molded DIP Package, board mount | 2.9W* |
| Molded DIP Package, socket mount | 2.6W** |
| *Molded DIP Package, board mount, derate 23.3m W/°C above 25°C | $\theta_{JA}$ = 43°C/W, |
| **Molded DIP Package, socket mount, derate 21.3m W/°C above 25°C | $\theta_{JA}$ = 47°C/W, |
| Operating $V_{DD}$ Range | $V_{SS}$ +7.0V to $V_{SS}$ +18.0V |
| Lead Temperature (Soldering, 10 seconds) | 300°C |

## DC Electrical Characteristics Min/max limits apply across temperature range unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Supply Current | | | | 0.3 | mA |
| $V_{IN(1)}$ | Logical "1" Input Voltage | | 0.45 $V_{DD}$ | | $V_{DD}$ +0.3 | V |
| $V_{IN(0)}$ | Logical "0" Input Voltage | | $V_{SS}$−0.3 | | 1.0 | V |
| $V_{OUT(0)}$ | Logical "0" Output Voltage | $I_{SINK}$ = 0.6 mA | | | 0.4 | V |
| $I_{OUT(1)}$ | Logical "1" Output Leakage Current | $V_{OUT}$ = $V_{DD}$ | 0 | | ±10 | μA |
| $I_{IN(1)}$ | Logical "1" Input Leakage Current | $V_{IN}$ = $V_{DD}$ | 0 | | 1.0 | μA |
| $I_{IN(0)}$ | Logical "0" Input Leakage Current | $V_{IN}$ = $V_{SS}$ | −1.0 | | 0 | μA |
| $V_{TC}$ | Input Voltage | | 4.5 | | $V_{DD}$+0.3 | V |
| $V_{TC}$ | Input Impedance | | 10 | | 30 | kΩ |
| $Z_{OUT}$ | Output Impedance | Backplane and Segment Outputs | | | 10 | kΩ |
| $Z_{OUT}$ | DC Offset Voltage | Between Any Backplane and Segment Output | 0 | | ±10 | mV |

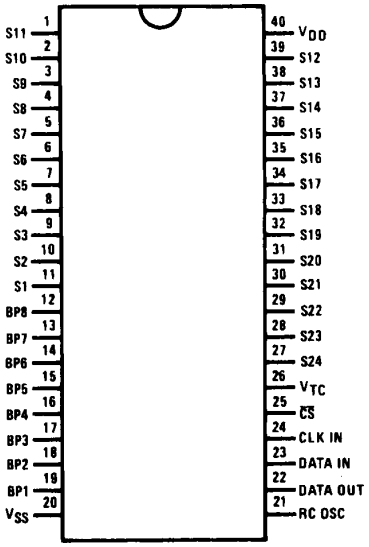
## AC Electrical Characteristics $T_A$ and $V_{DD}$ within operating range unless otherwise noted.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $f_{OSC}$ | Oscillator Frequency* | | 128$\eta$ | | 400$\eta$ | Hz |
| $f_{CLK\ IN}$ | Clock Frequency | | DC | | 100 | kHz |
| $t_{ON}$ | Clock Pulse Width | | 5.0 | | | μs |
| $t_{OFF}$ | Clock OFF Time | | 5.0 | | | μs |
| $t_S$ | Input Data Set-Up Time | | 2.0 | | | μs |
| $t_H$ | Input Data Hold Time | | 1.0 | | | μs |
| $t_{ACC}$ | Access Time | | 5.0 | | | μs |
| $t_r$ | Rise Time | Backplane, Segment Outputs $C_L$ = 2000 pF | | | 60 | μs |
| $t_f$ | Fall Time | Backplane, Segment Outputs $C_L$ = 2000 pF | | | 60 | μs |

* $\eta$ is the number of backplanes programmed.

## Connection Diagrams

**Dual-In-Line Package**

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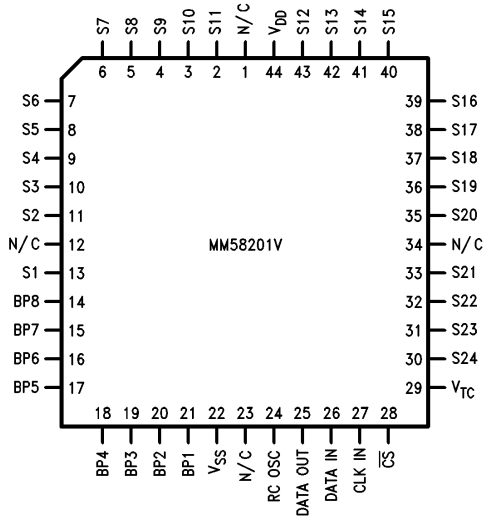
**Top View**

**Plastic Chip Carrier**

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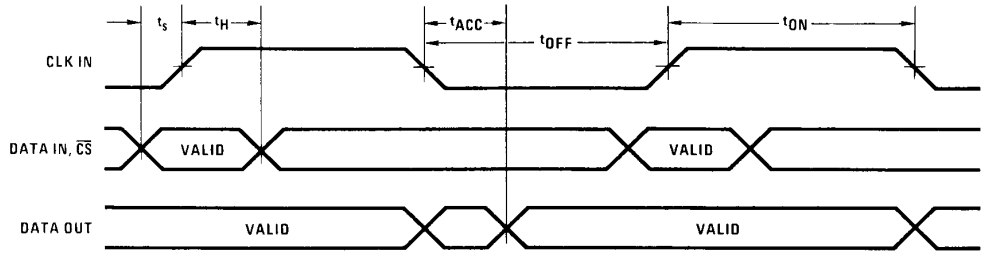
**Top View**

**FIGURE 2**

**Order Number MM58201N or MM58201V**
**See NS Package Number N40A or V44A**

## Switching Time Waveforms

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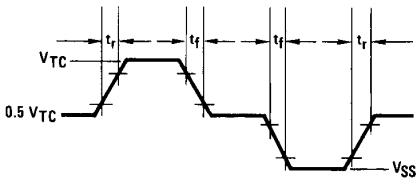
**Backplane Output**

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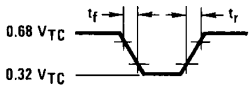
**Segment Output**

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## Functional Description

A functional diagram of the MM58201 LCD driver is shown in *Figure 1*. Connection diagrams are shown in *Figure 2*.

### SERIAL INPUTS AND OUTPUTS

A negative-going edge on the $\overline{CS}$ input initiates a frame. The $\overline{CS}$ input must then stay low for at least one rising edge of CLK IN, and may not be pulsed low again for the next 31 clocks. At least one clock must occur while $\overline{CS}$ is high. If CLK IN is held at a logic "1", $\overline{CS}$ is disabled. This allows the signal that drives $\overline{CS}$ to be used for other purposes when the MM58201 is not being addressed.

CLK IN latches data from the DATA IN input on its rising edge. Data from the DATA OUT pin changes on the falling edge of CLK IN and is valid before the next rising edge.

The first five bits of data following $\overline{CS}$ are the address bits *(Figure 3)*. The address selects the column where the operation is to start. Bit 1 is the MSB and bit 5 is the LSB. The sixth bit is the read/write bit. A logic "1" specifies a read operation and a logic "0" specifies a write operation. The next 24 bits are the data bits. The first data bit corresponds to the BP1 row of the display, the second data bit to the BP2 row, and so on. After the eighth and sixteenth data bits, the column pointer is incremented. When starting address 10110 or 10111 is specified, the column pointer increments from 10111 to 00000.

During a read or write cycle, the LCD segment outputs do not reflect the data in the RAM. To avoid disrupting the pattern viewed on the display, the read or write cycle time should be kept short. Since the LCD turn-on time can be as little as 30 ms, a clock rate of at least 10 kHz would be required in order to address the entire contents of the RAM within that time interval. The formula below can be used to estimate the minimum clock rate:

$$f_{CLK\ IN} = \frac{30}{(t_{LCD} - 7t_s)}$$

where $t_s$ is the processor's set-up time between each read or write cycle, and $t_{LCD}$ is the minimum turn-on or turn-off time of the LCD as specified by the LCD manufacturer.

The DATA OUT output is an open drain N-channel device to $V_{SS}$ *(Figure 4)*. With an external pull-up this configuration allows the controller to operate at a lower supply voltage, and also permits the DATA OUT output to be wired in parallel with the DATA OUT outputs from any other drivers in the system.

To program the number of backplanes being driven and the M/$\overline{S}$ bit, load address 11000, a write bit, three bits for the number of backplanes (Table I), and the M/$\overline{S}$ bit. The remaining 20 data bits will be ignored but it is necessary to provide 21 more clocks before initiating another frame.

**TABLE I. Backplane Select**

| Number of Backplanes | B2 | B1 | B0 |
|---|---|---|---|
| 2 | 0 | 0 | 1 |
| 3 | 0 | 1 | 0 |
| 4 | 0 | 1 | 1 |
| 5 | 1 | 0 | 0 |
| 6 | 1 | 0 | 1 |
| 7 | 1 | 1 | 0 |
| 8 | 1 | 1 | 1 |

### RC OSC Pin

This oscillator generates the timing required for multiplexing the liquid crystal display. The oscillator operates at a frequency that is $4\eta$ times the refresh rate of the display, where $\eta$ is the number of backplanes programmed. Since the refresh rate should be in the range from 32 Hz to 100 Hz, the oscillator frequency must be:

$$128\eta \leq f_{OSC} \leq 400\eta$$

The frequency of oscillation is related to the external R and C components in the following way:

$$f_{OSC} = \frac{1}{1.25\ RC} \pm 30\%$$

The value used for the external resistor should be in the range from 10 k$\Omega$ to 1 M$\Omega$.

The value used for the external capacitor should be less than 0.005 $\mu$F.

### $V_{TC}$ Pin

The $V_{TC}$ pin is an analog input that controls the contrast of the segments on the LCD. If eight backplanes are being driven ($\eta = 8$), a voltage of typically 8V is required at 25°C. The voltage for optimum contrast will vary from display to display. It also has a significant negative temperature coefficient.

The voltage source on the $V_{TC}$ input must be of relatively low impedance since the input impedance of $V_{TC}$ ranges from 10 k$\Omega$ to 30 k$\Omega$. A suitable circuit is shown in *Figure 5*.

In a standby mode, the $V_{TC}$ input can be set to $V_{SS}$. This reduces the supply current to less than 300 $\mu$A per driver.

### BACKPLANE AND SEGMENT OUTPUTS

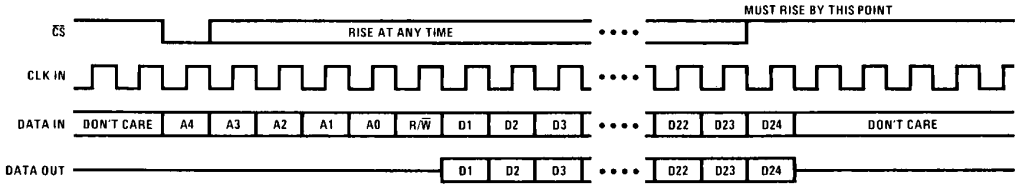
Connect the backplane and segment outputs directly to the LCD row and column lines. The outputs are designed to drive a display with a total ON capacitance of up to 2000 pF.

The output structure consists of transmission gates tapped off of a resistor string driven by $V_{TC}$ *(Figure 6)*.

A critical factor in the lifetime of an LCD is the amount of DC offset between a backplane and segment signal. Typically, 50 mV of offset is acceptable. The MM58201 guarantees an offset of less than 10 mV.

The BP1 output is disabled when the M/$\overline{S}$ bit is set to zero. This allows the BP1 output from the master chip to be connected directly to it so that synchronizing signals can be generated. Synchronization occurs once each refresh cycle, so the cascaded chips are assured of remaining synchronized.

## Functional Description (Continued)




| | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 | S9 | S10 | S11 | S12 | S13 | S14 | S15 | S16 | S17 | S18 | S19 | S20 | S21 | S22 | S23 | S24 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BP1 | | | | | | | | | | | | | D1 | D9 | D17 | | | | | | | | | | B2 |
| BP2 | | | | | | | | | | | | | D2 | D10 | D18 | | | | | | | | | | B1 |
| BP3 | | | | | | | | | | | | | D3 | D11 | D19 | | | | | | | | | | B0 |
| BP4 | | | | | | | | | | | | | D4 | D12 | D20 | | | | | | | | | | M/S |
| BP5 | | | | | | | | | | | | | D5 | D13 | D21 | | | | | | | | | | |
| BP6 | | | | | | | | | | | | | D6 | D14 | D22 | | | | | | | | | | |
| BP7 | | | | | | | | | | | | | D7 | D15 | D23 | | | | | | | | | | |
| BP8 | | | | | | | | | | | | | D8 | D16 | D24 | | | | | | | | | | |
| A4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| A3 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
| A2 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| A1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 |
| A0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

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Diagram above shows where data will appear on display if starting address 01100 is specified in data format.

**FIGURE 3. Data Format**

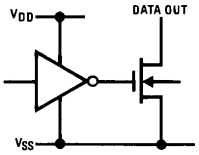


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**FIGURE 4. DATA OUT Structure**

## Functional Description (Continued)

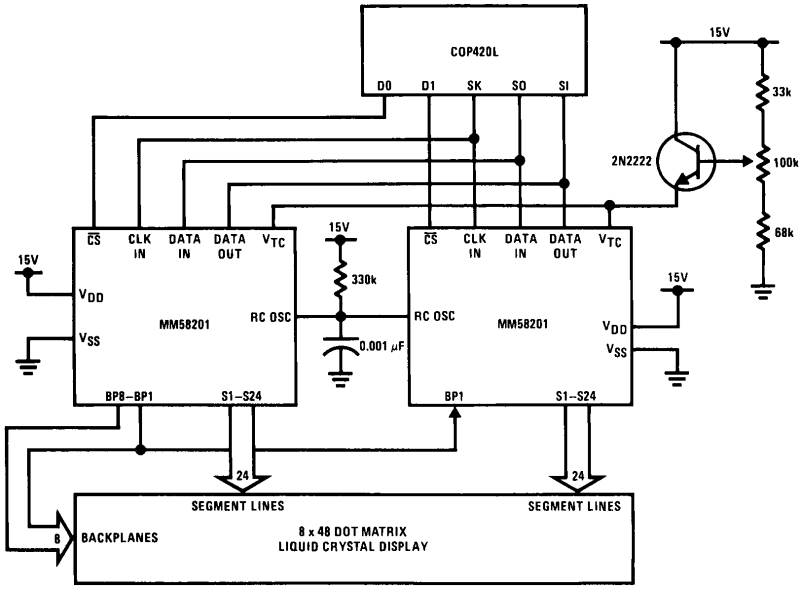


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**FIGURE 5. Typical Application**

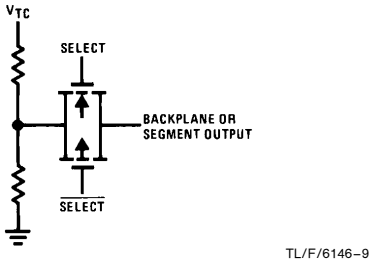


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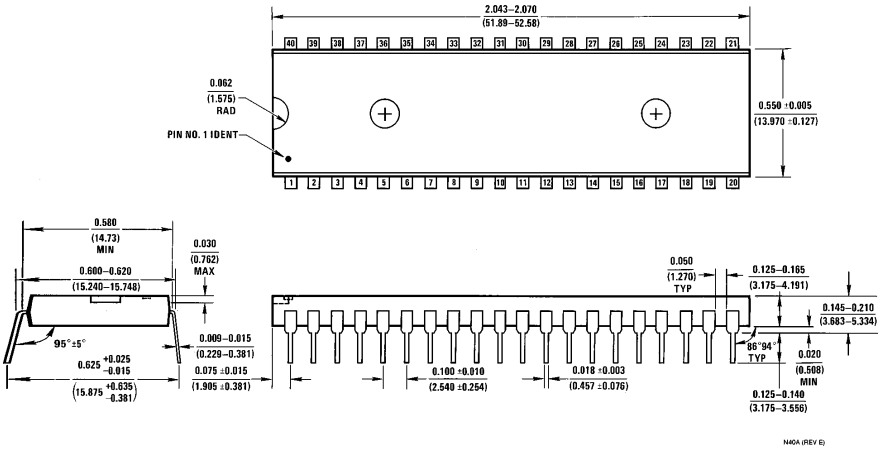
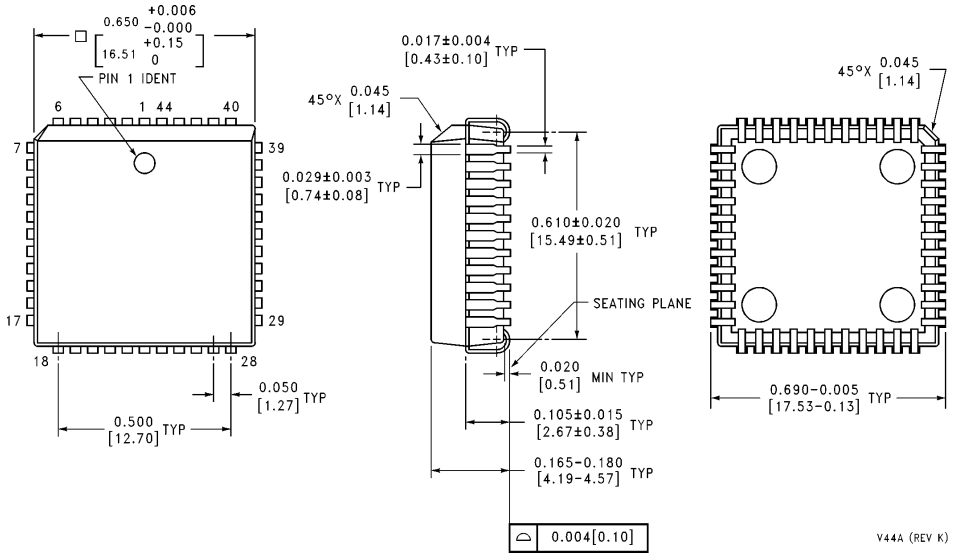
**FIGURE 6. Structure of LCD Outputs**

## Physical Dimensions inches (millimeters)




**Molded Dual-In-Line Package (N)**
**Order Number MM58201N**
**NS Package Number N40A**

## Physical Dimensions inches (millimeters) (Continued)




**Plastic Chip Carrier (V)**
**Order Number MM58201V**
**NS Package V44A**

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