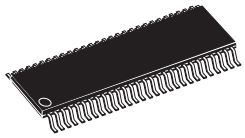
STLVDS385B

+ 3.3 V programmable LVDS transmitter 24-bit flat panel display (FPD) link-85 MHz

Features

- 20 to 85 MHz shift clock support
- Best-in-class set & hold times on Txinputs
- Tx power consumption < 130 mW (typ) @85 MHz grayscale
- Tx power-down mode < 200 µW (max)
- Supports VGA, SVGA, XGA and single/dual pixel SXGA.
- Narrow bus reduces cable size and cost
- Up to 2.38 Gbps throughput
- Up to 297.5 megabytes/sec. bandwidth
- 345 mV (typ) swing LVDS devices for low EMI
- PLL requires no external components
- Compatible with TIA/EIA -644 LVDS standard



TSSOP56

Description

The STLVDS385B transmitter converts 28 bits of LVCMOS/LVTTL data into four LVDS (low voltage differential signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 85 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 595 Mbps per LVDS data channel. Using a 85 MHz clock, the data throughput is 297.5 Mbytes/sec. The transmitter can be programmed for rising edge strobe or falling edge strobe through a dedicated pin. A rising edge or falling edge strobe transmitter will inter operate with a falling edge strobe receiver without any translation logic.

Table 1. Device summary

Order code	Temperature range	Package	Packaging
STLVDS385BTR	- 10 to 70 °C	TSSOP56 (tape and reel)	2000 parts per reel

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1 Pin configuration

Figure 1. Pin configuration

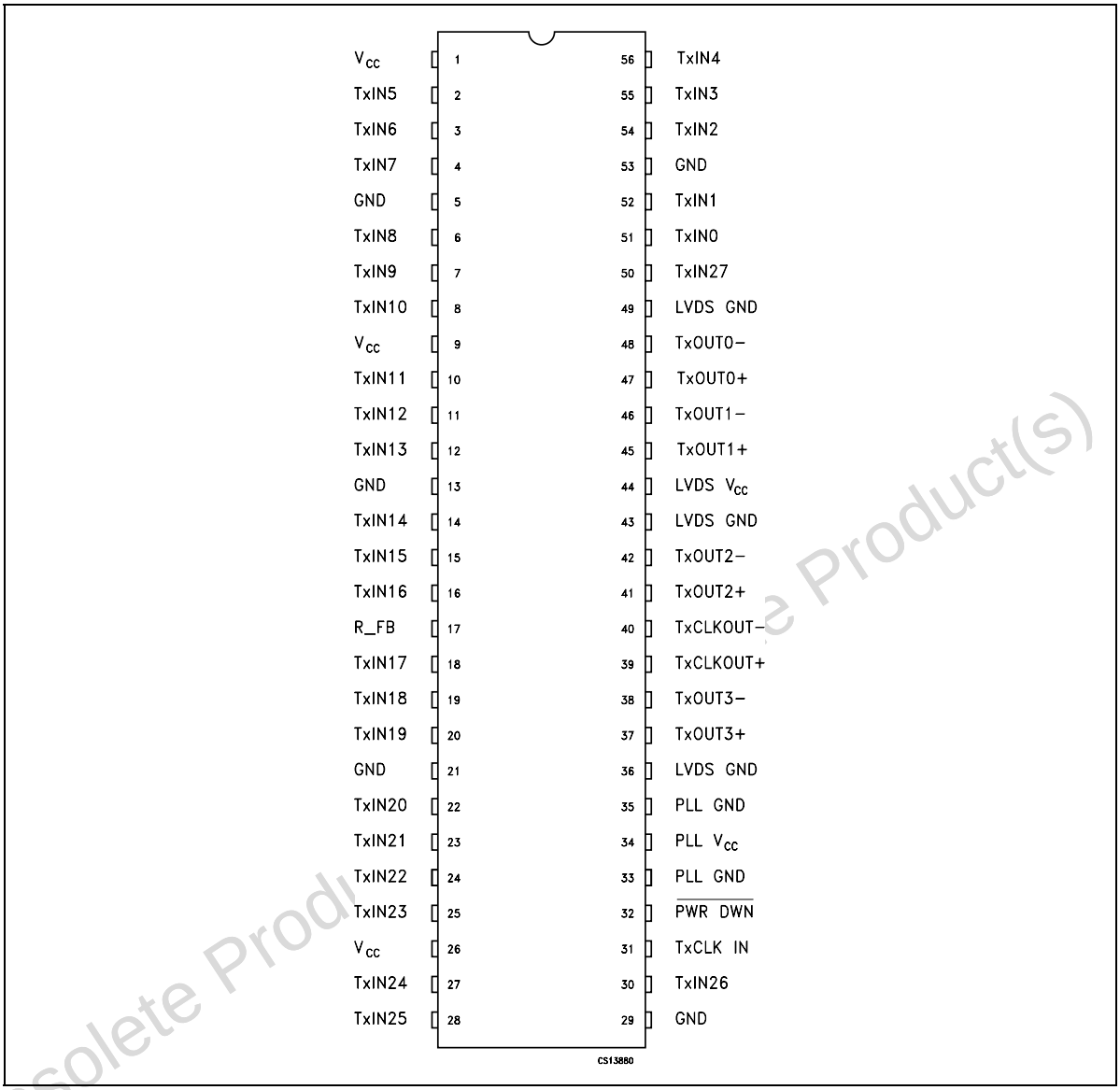


Table 2. Pin description

Pin n°	Symbol	Name and function
1, 9, 26	V_{CC}	Power supply pins for TTL inputs
2, 3, 4, 6, 7, 8, 10, 11, 12, 14, 15, 16, 18, 19, 20, 22, 23, 24, 25, 27, 28, 30, 50, 51, 52, 54, 55, 56	T_XIN	TTL level input. This includes: 8 red, 8 green, 8 blue and 4 control lines- FPLINE, FPFRAME, and DRDY (also referred to as HSYNC, VSYNC, data enable)
5, 13, 21, 29	GND	Ground pins for TTL inputs
17	R_FB	Programmable strobe select
31	TxCLKIN	TTL level clock input. Pin name TxCLK IN
32	PWRDWN	TTL level input. When asserted (low input) tri-states the outputs, ensuring low current at power down
33, 35	PLL GND	Ground pins for PLL
34	PLL V_{CC}	Power supply pin for PLL
36, 43, 49	LVDS GND	Ground pins for LVDS outputs
37, 41, 45, 47	TxOUT+	Positive LVDS differential data output
38, 42, 46, 48	TxOUT-	Negative LVDS differential data output
39	TxCLK OUT+	Positive LVDS differential clock output
40	TxCLK OUT-	Negative LVDS differential clock output
44	LVDS V_{CC}	Power supply pin for LVDS outputs

Table 3. Programmable transmitter

Pin	Condition	Strobe status
R_FB	R_FB = V_{CC}	Rising edge strobe
R_FB	R_FB = GND or NC	Falling edge strobe

2 Maximum ratings

Table 4. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage	- 0.3 to 4	V
V_I	CMOS/TTL input voltage	- 0.5 to (V_{CC} + 0.3)	V
V_{DO}	LVDS driver output voltage	- 0.3 to (V_{CC} + 0.3)	V
I_{OSD}	LVDS output short circuit duration	Continuous	
ESD	HBM	7	kV
	EIAJ	500	V
I_{LATCH}	Latch up tolerance	± 300	mA
T_J	Junction temperature	+ 150	°C
T_{STG}	Storage temperature range	- 65 to + 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage	3.0	3.3	3.6	V
T_A	Operating free air temperature	0		70	°C
ΔV_{CC}	Supply noise voltage			100	mV_{PP}
$f_{TxCLKIN}$	TxCLKIN frequency	20		85	MHz

Table 6. Recommended transmitter input characteristics (V_{CC} = 3.3 V, T_J = - 10 to 70 °C unless otherwise noted. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{CIT}	TxCLK IN transition time (*Figure 6*)	1.0		6.0	ns
t_{CIP}	TxCLK IN period (*Figure 7*)	11.76	T	50	ns
t_{CIH}	TxCLK IN high time (*Figure 7*)	0.35T	0.5T	0.65T	ns
t_{CIL}	TxCLK IN low time (*Figure 7*)	0.35T	0.5T	0.65T	ns
t_{XIT}	TxIN transition time	1.5		6.0	ns

3 Electrical characteristics

Table 7. LVCMOS/LVTTL DC specifications (V_{CC} = 3.3 V, T_J = -10 to 70 °C unless otherwise noted. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IH}	High level input voltage		2.0		V_{CC}	mV
V_{IL}	Low level input voltage		GND		0.8	mV
V_{CL}	Input clamp voltage	I_{CL} = -18mA		-0.79	-1.5	V
I_I	Input current	V_I =0.4 V, 2.5 or V_{CC}			10	µA
		V_I = GND	-10	0		µA

Table 8. LVDS DC specifications (V_{CC} = 3.3 V, T_J = - 10 to 70 °C unless otherwise noted. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OD}	Differential output voltage	R_L = 100Ω	250	345	450	mV
ΔV_{OD}	Change in V_{OD} between complimentary output states	R_L = 100Ω			35	mV
V_{OS}	Offset voltage (*Note 2*)	R_L = 100Ω	1.125	1.25	1.375	V
ΔV_{OS}	Change in V_{OS} between complimentary output states	R_L = 100Ω			35	mV
I_{OS}	Output short circuit current	V_O = 0, R_L = 100Ω		-3.5	-5	mA
I_{OZ}	Output tri-state current	$\overline{\text{Power-down}}$ = 0, V_O = 0 or V_{CC}		±1	±10	µA

Table 9. Transmitter supply current (V_{CC} = 3.3 V, T_J = - 10 to 70 °C unless otherwise noted. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions		Min.	Typ.	Max.	Unit
ICCTW	Transmitter supply current worst case	R_L = 100Ω, C_L = 5pF, worst case pattern (*Figure 2*, *Figure 4*)	f = 32.5 MHz		31	45	mA
			f = 40 MHz		32	50	
			f = 65 MHz		37	55	
			f = 85 MHz		42	60	
ICCTG	Transmitter supply current 16 grayscale	R_L = 100Ω, C_L = 5pF, 16 grayscale pattern (*Figure 2*, *Figure 4*)	f = 32.5 MHz		29	38	mA
			f = 40 MHz		30	40	
			f = 65 MHz		35	45	
			f = 85 MHz		39	50	
ICCTZ	Transmitter supply current power down	$\overline{\text{Power-down}}$ = low driver outputs in tri-state under power-down mode			10	55	µA

Table 10. Transmitter switching characteristics (V_{CC} = 3.3 V, T_J = -10 to 70 °C unless otherwise noted. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{LLHT}	LVDS low-to-high transition time (*Figure 5*)			0.75	1.5	ns
t_{LLLT}	LVDS high-to-low transition time (*Figure 5*)			0.75	1.5	ns
t_{TPP0}	Transmitter output pulse position for bit 0 (*Figure 12* - *Note 3*)	f = 40 MHz	-0.25	0	0.25	ns
t_{TPP1}	Transmitter output pulse position for bit 1		3.32	3.57	3.82	ns
t_{TPP2}	Transmitter output pulse position for bit 2		6.89	7.14	7.39	ns
t_{TPP3}	Transmitter output pulse position for bit 3		10.46	10.71	10.96	ns
t_{TPP4}	Transmitter output pulse position for bit 4		14.04	14.29	14.54	ns
t_{TPP5}	Transmitter output pulse position for bit 5		17.61	17.86	18.11	ns
t_{TPP6}	Transmitter output pulse position for bit 6		21.18	21.43	21.68	ns
t_{TPP0}	Transmitter output pulse position for bit 0 (*Figure 12* - *Note 3*)	f = 65 MHz	-0.20	0	0.20	ns
t_{TPP1}	Transmitter output pulse position for bit 1		2.00	2.20	2.40	ns
t_{TPP2}	Transmitter output pulse position for bit 2		4.20	4.40	4.60	ns
t_{TPP3}	Transmitter output pulse position for bit 3		6.39	6.59	6.79	ns
t_{TPP4}	Transmitter output pulse position for bit 4		8.59	8.79	8.99	ns
t_{TPP5}	Transmitter output pulse position for bit 5		10.79	10.99	11.19	ns
t_{TPP6}	Transmitter output pulse position for bit 6		12.99	13.19	13.99	ns
t_{TPP0}	Transmitter output pulse position for bit 0 (*Figure 12* - *Note 3*)	f = 85 MHz	-0.20	0	0.20	ns
t_{TPP1}	Transmitter output pulse position for bit 1		1.48	1.68	1.88	ns
t_{TPP2}	Transmitter output pulse position for bit 2		3.16	3.36	3.56	ns
t_{TPP3}	Transmitter output pulse position for bit 3		4.84	5.04	5.24	ns
t_{TPP4}	Transmitter output pulse position for bit 4		6.52	6.72	6.92	ns
t_{TPP5}	Transmitter output pulse position for bit 5		8.20	8.40	8.60	ns
t_{TPP6}	Transmitter output pulse position for bit 6		9.88	10.08	10.28	ns
t_{STC}	TxIN setup to TxCLK IN (*Figure 7*)		2.5			ns
t_{HTC}	TxIN hold to TxCLK IN (*Figure 7*)		0			ns
t_{CCD}	TxCLK IN to TxCLK OUT delay (*Figure 8*)	T_A = 25°C, V_{CC} = 3.3V	3.8		6.3	ns
t_{CCD}	TxCLK IN to TxCLK OUT delay (*Figure 8*)		2.8		7.1	ns
t_{JCC}	Transmitter jitter cycle-to-cycle (*Figure 12* - *Note 4*)	f = 85 MHz		110	150	ps
		f = 65 MHz		210	230	
		f = 40 MHz		350	370	

Table 10. Transmitter switching characteristics (continued) (V_{CC} = 3.3 V, T_J = -10 to 70 °C unless otherwise noted. Typical values are referred to T_A = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
t_{PLLS}	Transmitter phase lock loop set (*Figure 9*)				10	ms
t_{PDD}	Transmitter power down delay (*Figure 11*)				100	ns

Note: 1 Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

2 V_{OS} previously referred as V_{CM}.

3 The minimum and maximum limits are based on statistical analysis of the device performance over process, voltage, and temperature range. This parameter is functionality tested only on automatic test equipment (ATE).

4 The limits are based on bench characterization of the device's jitter response over the power supply voltage range. Output clock jitter is measured with a cycle-to-cycle jitter of ± 3 ns applied to the input clock signal while data inputs are switching. A jitter event of 3 ns, represents worse case jump in the clock edge from most graphics controller VGA chips currently available.

5 The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

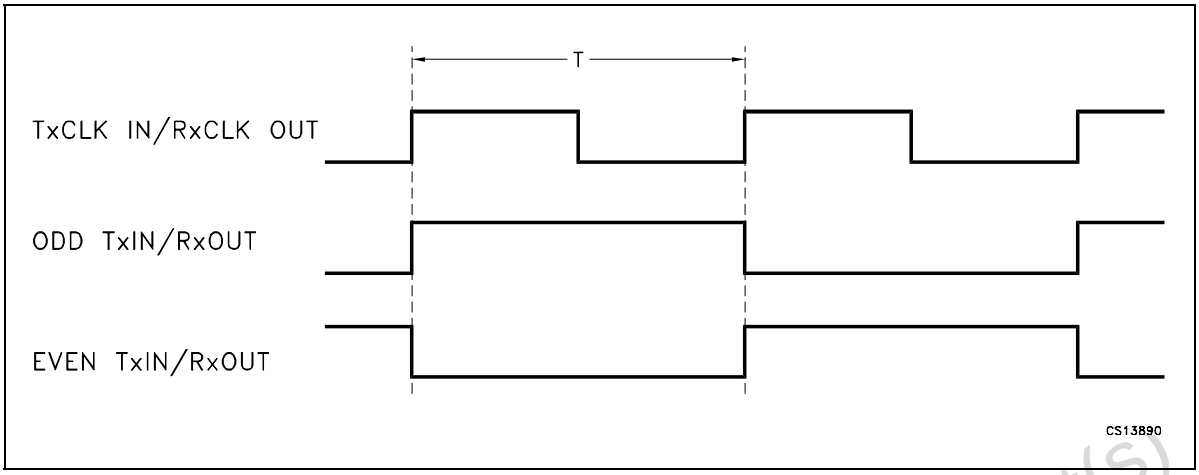
6 The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

7 Figure 2, Figure 3 show a falling edge data strobe (TxCLK IN/RxCLK OUT).

8 Recommended pin to signal mapping. Customer may choose to define differently.

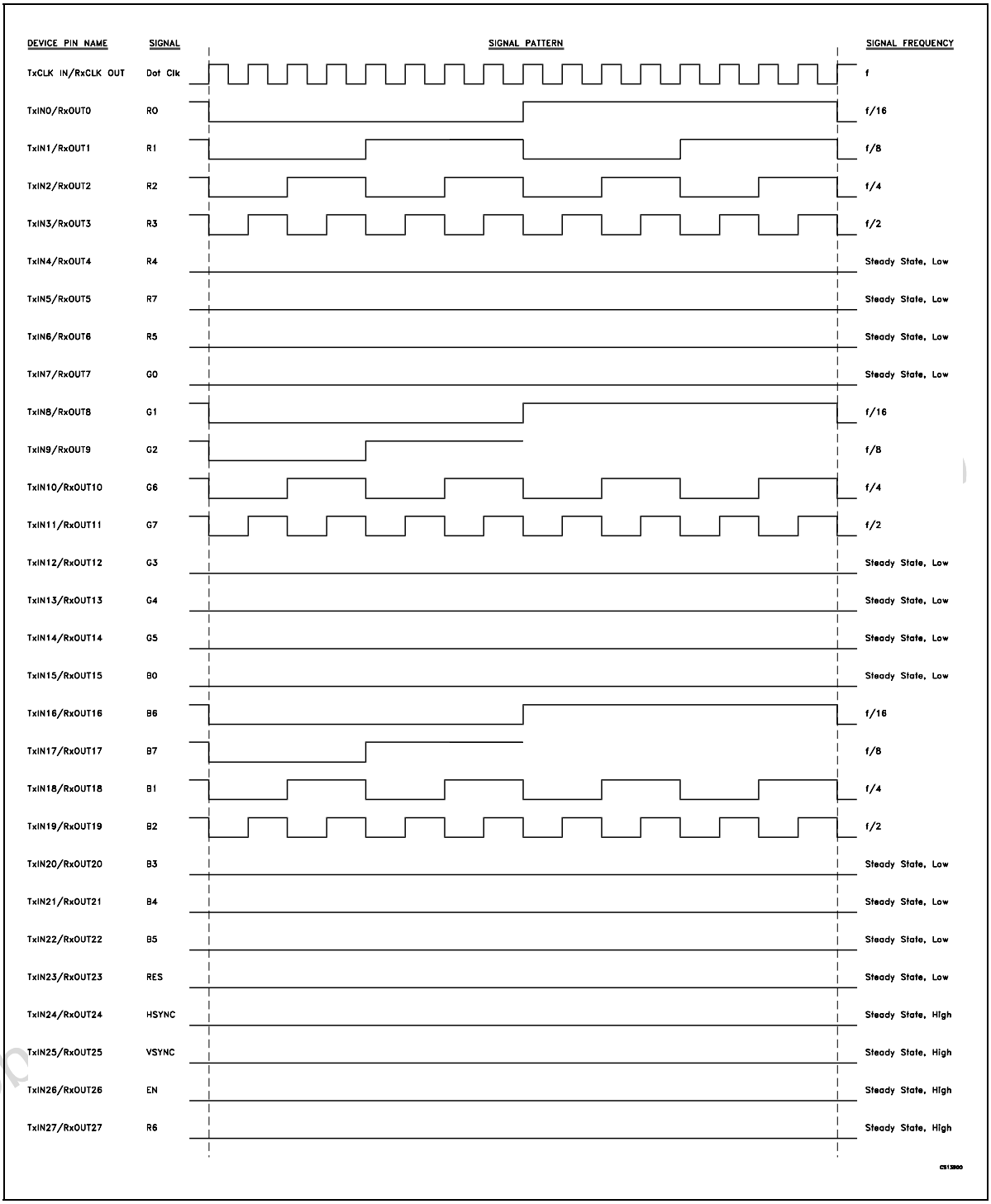
4 AC timing diagrams

Figure 2. Worst case test pattern (1)



1. The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Figure 3. 16 grayscale test patter (1) (2) (3)



1. The 16 grayscale test pattern tests device power consumption for a “typical” LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.
2. *Figure 2*, *Figure 3* show a falling edge data strobe (TxCLK IN/RxCLK OUT).
3. Recommended pin to signal mapping. Customer may choose to define differently.

Figure 4. (Transmitter) LVDS output load

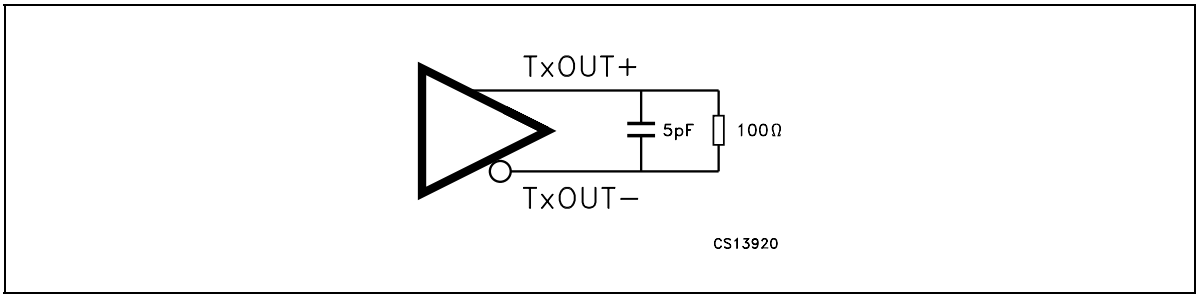


Figure 5. (Transmitter) LVDS transition time

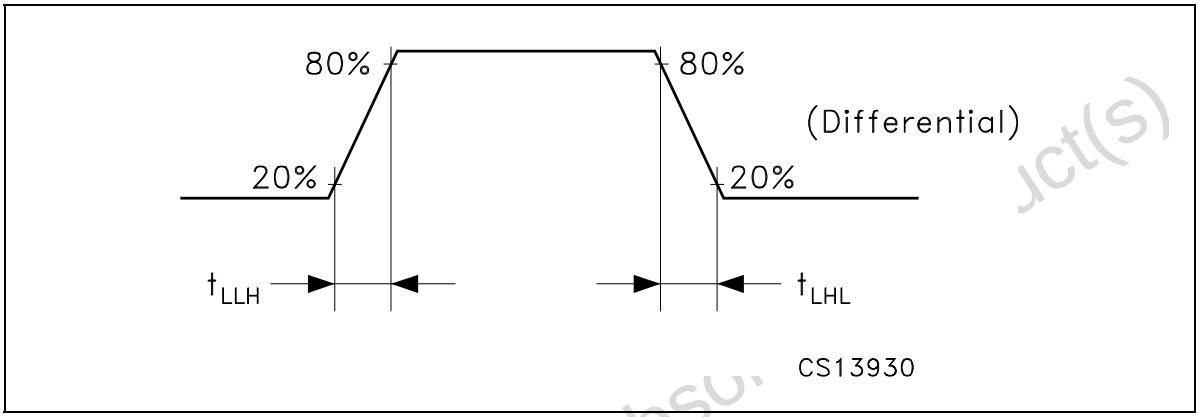


Figure 6. (Transmitter) input clock transition time

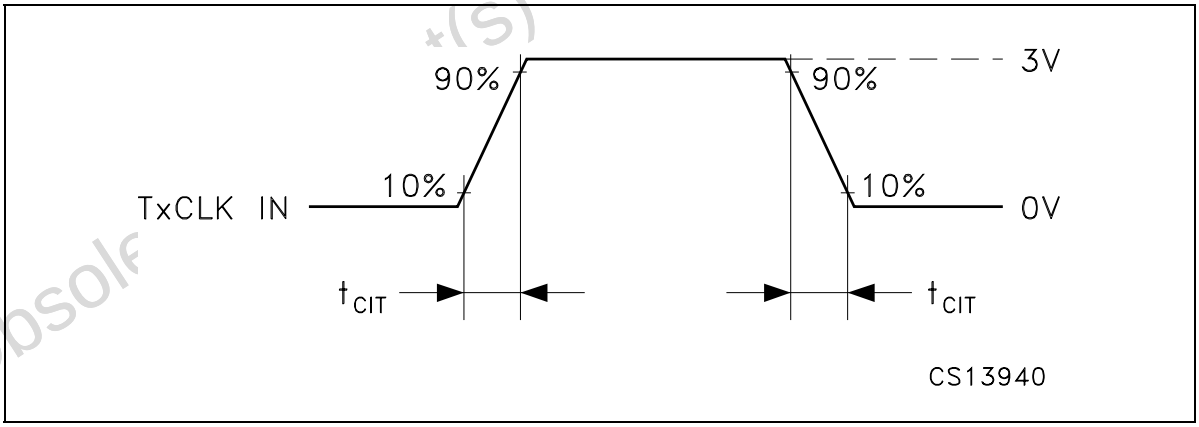


Figure 7. (Transmitter) setup/hold and high/low times (falling edge strobe)

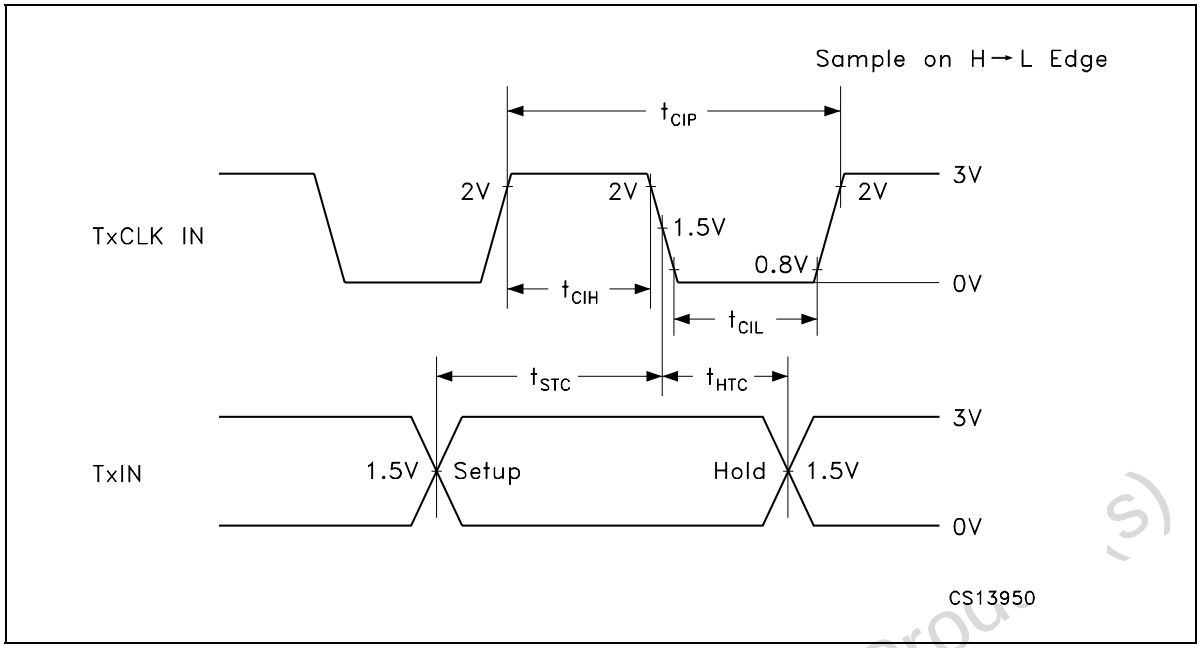


Figure 8. (Transmitter) clock in to clock out delay

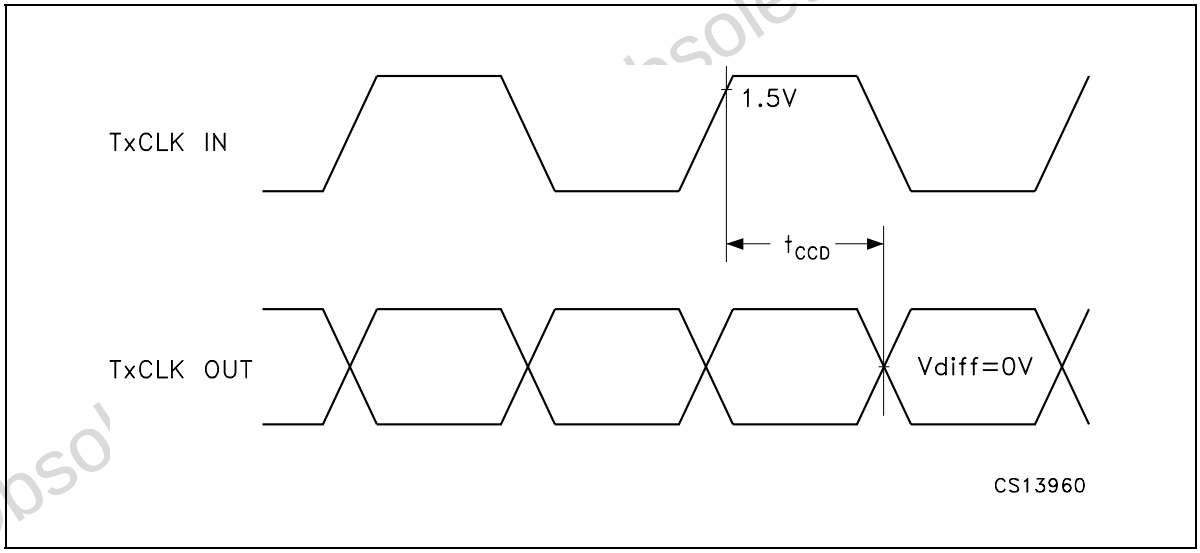


Figure 9. (Transmitter) phase lock loop set time

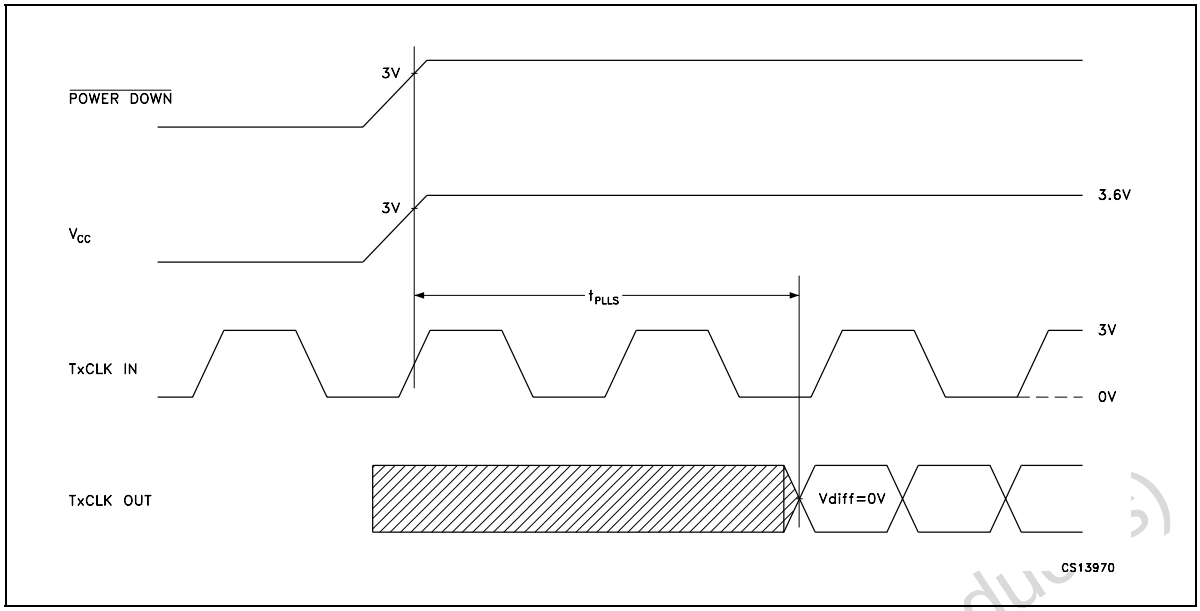


Figure 10. 28 parallel TTL data inputs mapped to LVDS outputs

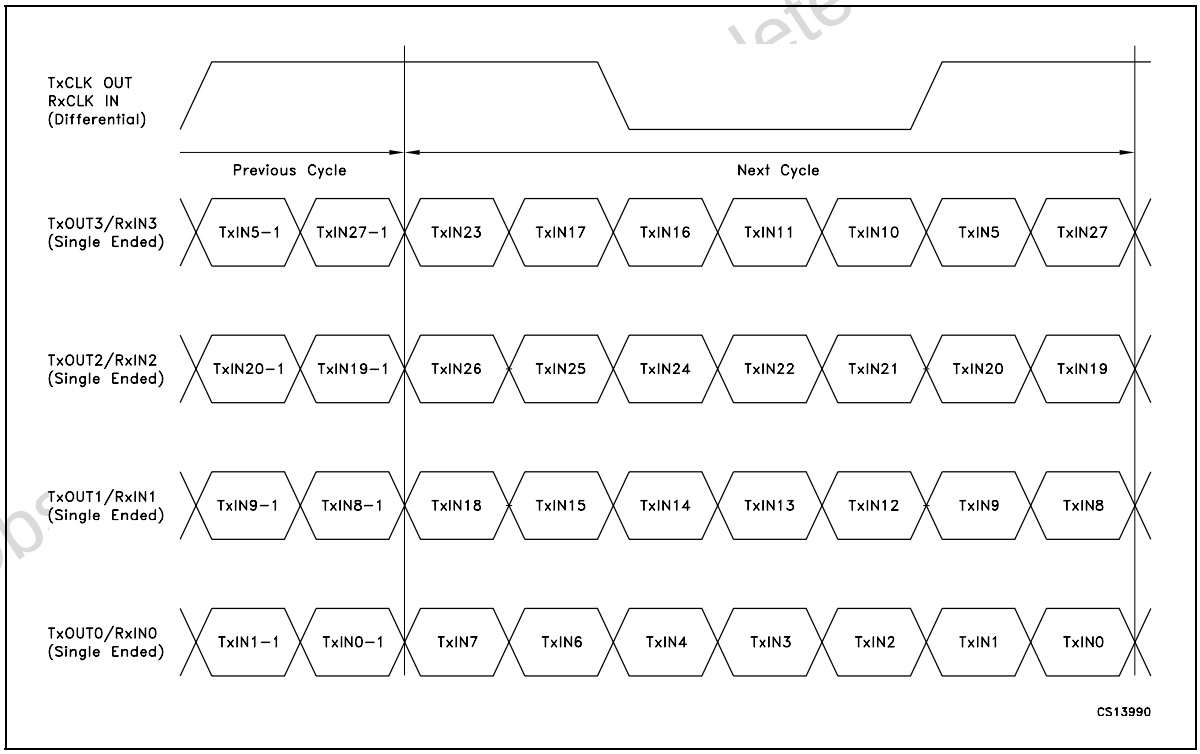


Figure 11. Transmitter power down delay

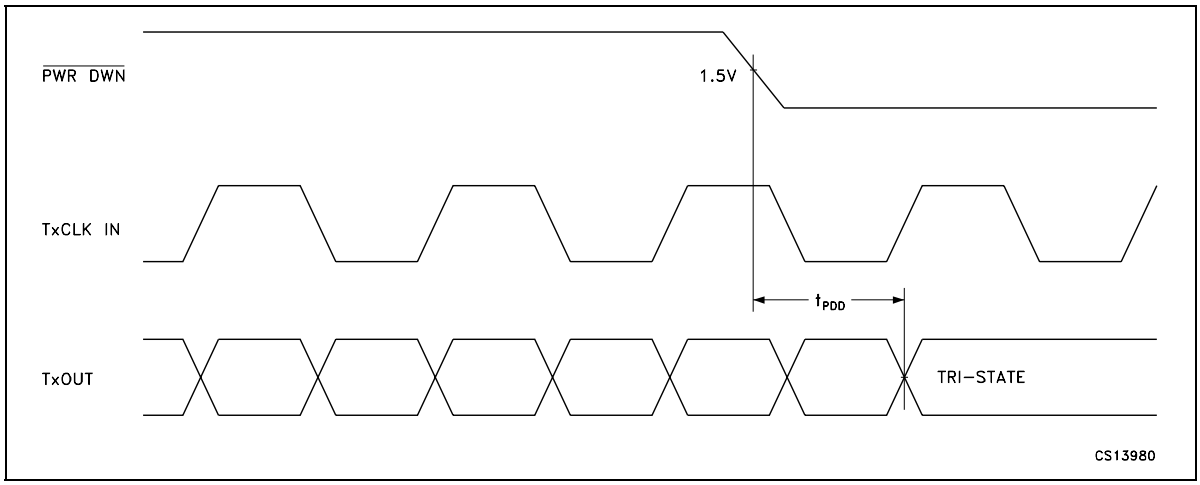
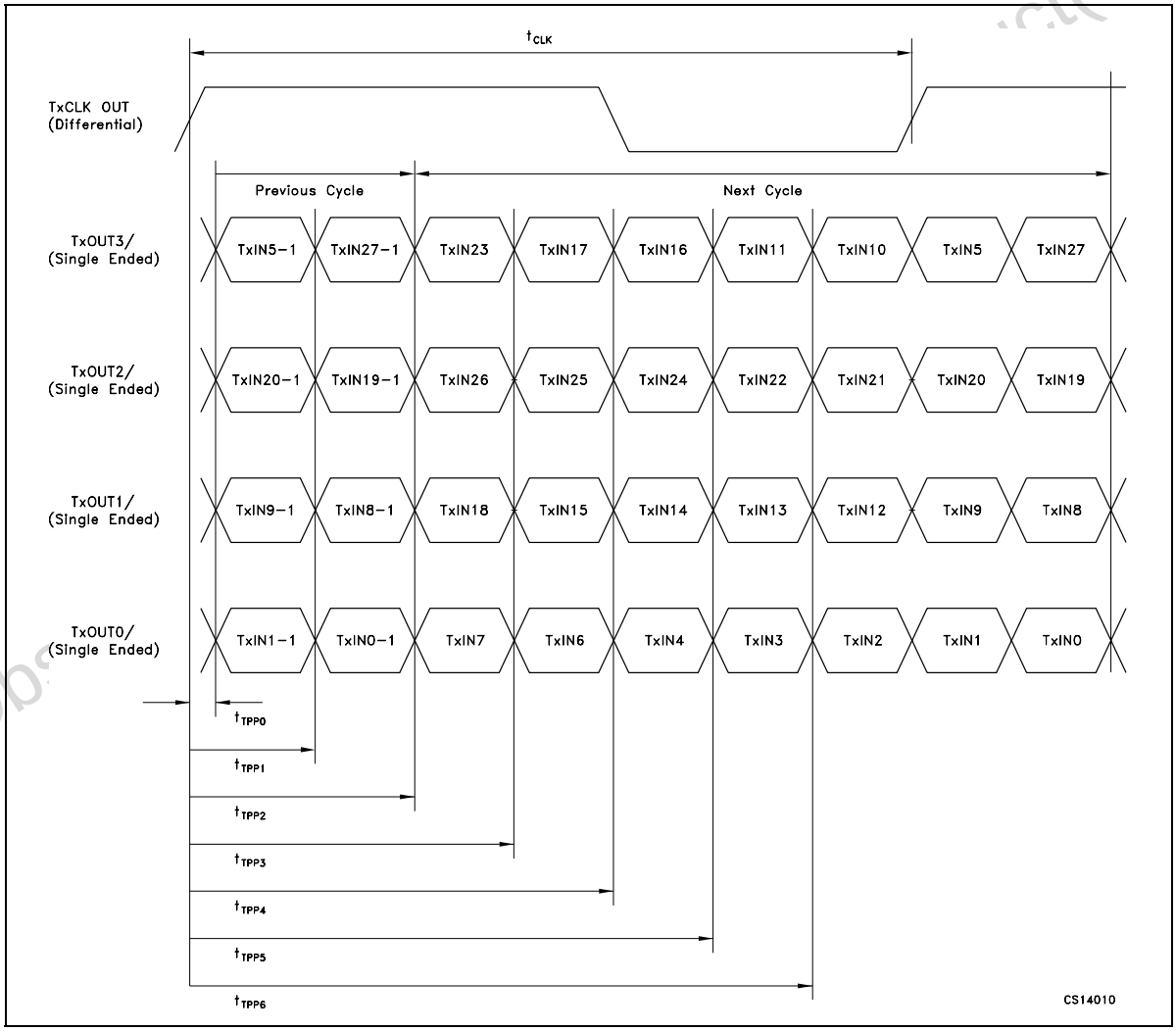


Figure 12. Transmitter LVDS output pulse position measurement



5 Package mechanical data

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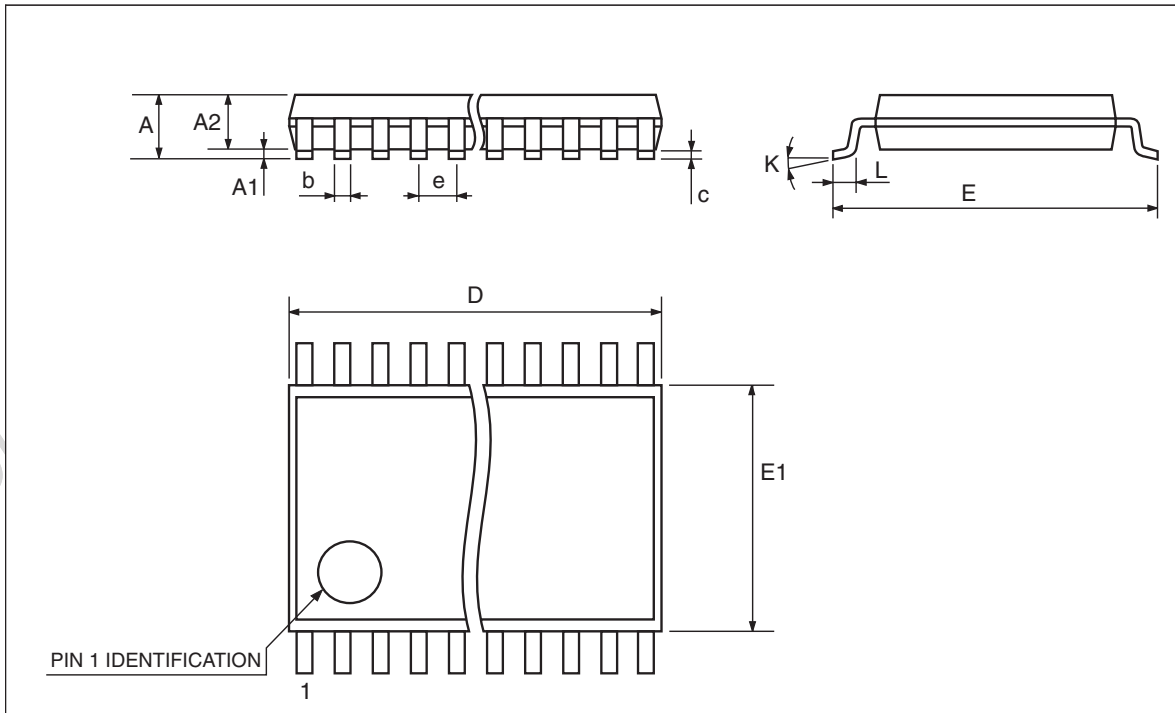
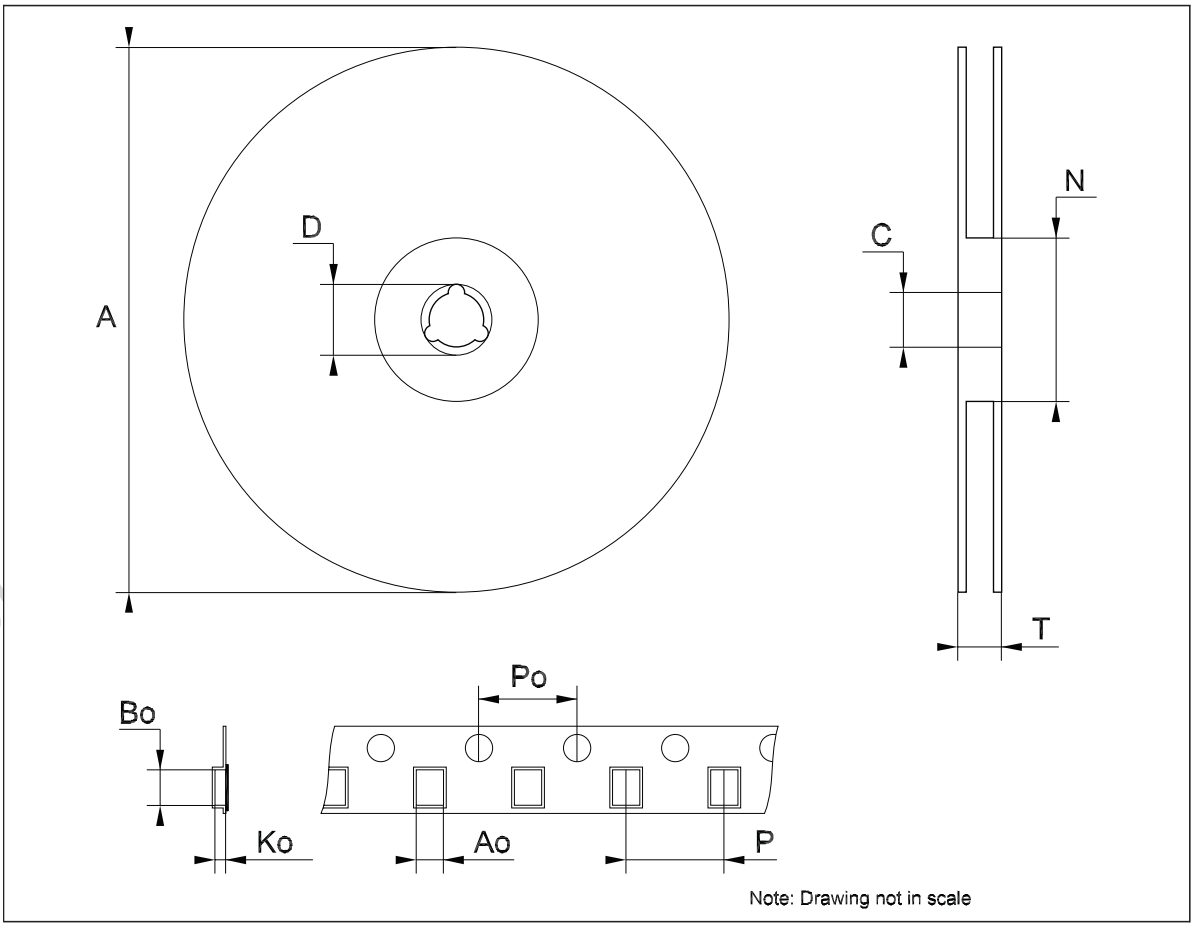
TSSOP56 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	13.9		14.1	0.547		0.555
E	7.95		8.25	0.313		0.325
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.45		0.75	0.020		0.030



Tape and reel TSSOP56 mechanical data

Dim.	mm.			inch.		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			30.4			1.197
Ao	8.7		8.9	0.342		0.350
Bo	17.2		17.4	0.677		0.685
Ko	1.4		1.6	0.055		0.063
Po	3.9		4.1	0.153		0.161
P	11.9		12.1	0.468		0.476



Note: Drawing not in scale

6 Revision history

Table 11. Document revision history

Date	Revision	Changes
21-Jun-2004	1	First release.
26-Jan-2009	2	Modified *Table 1 on page 1*.

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