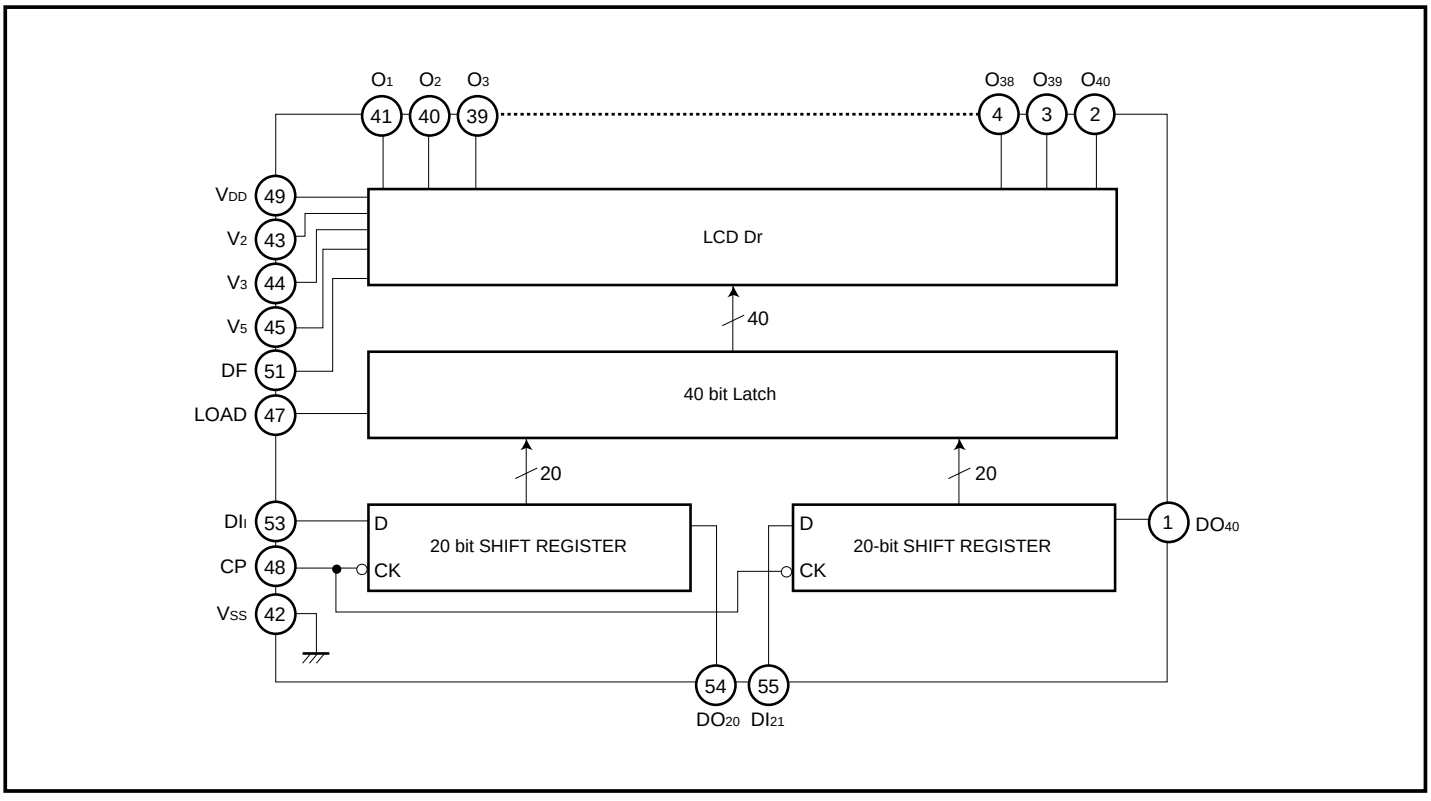
LCD segment driver
BU9706KS

The BU9706KS is a 40-output LCD segment driver provided with a 40-bit shift register and a 40-bit latch.
As the 40-bit shift register can be divided into two 20-bit sections, it can be used efficiently, based on the number of segments and the character configuration.
Also, by using a number of BU9706KS drivers, it is possible to configure an LCD segment driver of more than 80 bits.
As the liquid crystal drive voltage can be set externally to any value, it can be used as a driver IC for both static and dynamic drive in various types of liquid crystal display panels.

●Features

1) 40-bit shift register and 40-bit latch enable serial input - parallel output.
2) Shift register can be divided into two 20-bit sections.
3) Power supply voltage: 3.5 to 6V.
4) LCD drive voltage: 3 to 6V.
5) Can accommodates duty of 1 / 8 to 1 / 16.
6) Can be used as a driver IC for static drive by setting the liquid crystal drive voltage externally (V3 = V_{DD}, V2 = V5 = V_{SS}, connect DF as LCD common).

●Block diagram



●Absolute maximum ratings (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	– 0.3 ~ + 6.5	V
LCD power supply voltage*	$V_{DD} – V_5$	0 ~ + 6.5	V
Input voltage	V_{IN}	V_{SS} – 0.3 ~ V_{DD} + 0.3	V
Power dissipation	Pd	500	mW
Operating temperature	Topr	– 20 ~ + 70	°C
Storage temperature	Tstg	– 55 ~ + 125	°C

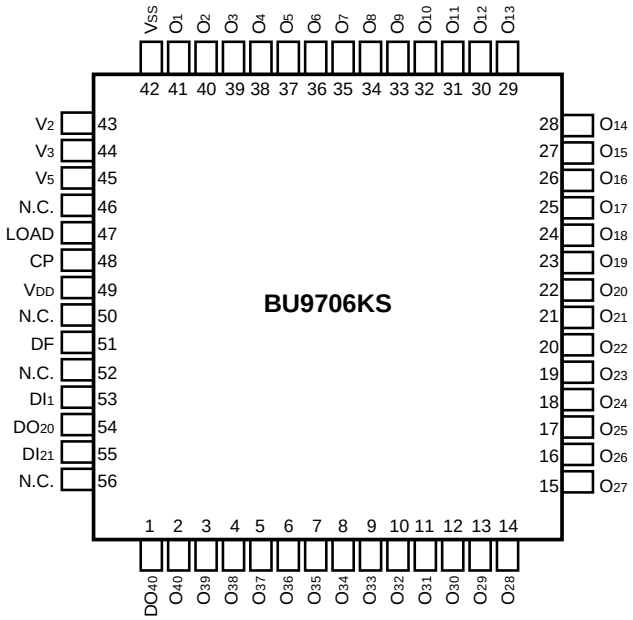
∗ The LCD power supply voltage must satisfy the condition of $V_{DD} > V_2 \geqq V_3 > V_5 \geqq V_{SS}$.

●Recommended operating conditions (Ta = 25°C, V_{SS} = 0V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.5	—	6.0	V
LCD power supply voltage*	$V_{DD} – V_5$	3.0	—	6.0	V
Input voltage	V_{IN}	0	—	V_{DD}	V

∗ The LCD power supply voltage must satisfy the condition of $V_{DD} > V_2 \geqq V_3 > V_5 \geqq V_{SS}$.

●Pin assignments



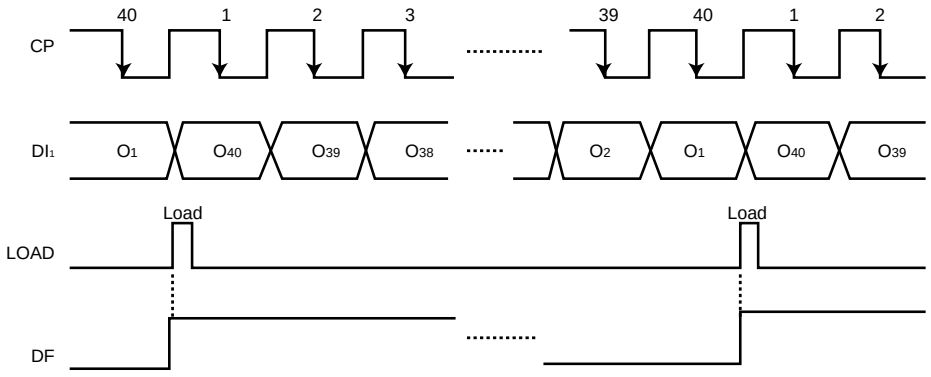
●Pin descriptions

Pin No.	Pin name	I / O	Function
2 ~ 41	O_{40} ~ O_1	O	Output pin for the liquid crystal driver. V_{DD}, V_2, V_3 or V_5 is output depending on the latch content and the DF signal. Refer to the truth table for the output level.
43 ~ 45	V_2 ~ V_5	—	Power supply pin for liquid crystal drive
49	V_{DD}	—	Logic power supply pin and liquid crystal drive power supply pin
42	V_{SS}	—	Logic power supply pin
53	DI_1	I	Data input pin for the shift register (1 to 20 bits). Data is read to the first bit of the shift register at the clock signal falling edge.
54	DO_{20}	O	Data output pin for the shift register (1 to 20 bits). Data is output in synchronization with the clock signal falling edge. A 40-bit shift register is accomplished by connecting pins 54 and 55.
55	DI_{21}	I	Data input pin for the shift register (21 to 40 bits). Data is read to the 21st bit of the shift register at the clock signal falling edge.
1	DO_{40}	O	Data output pin for the shift register (21 to 40 bits). Data is output in synchronization with the clock signal falling edge. It is used to configure an LCD driver with more than 40 bits by connecting it to the DI pin of the BU9706KS at the next stage.
48	CP	I	Clock signal input pin for the shift register. The contents of the shift register are shifted by 1 bit only at the clock signal falling edge.
47	LOAD	I	Latch signal input pin for the 40-bit latch. The contents of the shift register are transferred to O_1 to O_{40} at LOAD = "H" and the data is latched at LOAD = "L". While LOAD = "L", the latched data is held even if the contents of the shift register change.
51	DF	I	Input pin for the signal which produces AC for LCD drive.

●LCD drive output pin truth table

Latch data	DF	O_n terminal voltage
H	H	V_5
H	L	V_{DD}
L	H	V_3
L	L	V_2

●Timing chart



• Shifted at CP input falling.
• When the LOAD input state becomes "H", the contents of the shift register are transferred to the segment outputs O_1 to O_{40}, and when it is "L", the data is latched.

Fig.1

●Electrical characteristics (unless otherwise noted, Ta = 25°C, V_{DD} = 5 V)

DC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input high level voltage*1	V_{IH}	4.0	—	—	V	—
Input low level voltage*1	V_{IL}	—	—	1.0	V	—
Input high level current*1	I_{IH}	—	—	1	μA	$V_{IH} = V_{DD}$
Input low level current*1	I_{IL}	—	—	– 1	μA	V_{IL} = 0V
Output high level voltage*2	V_{OH}	4.2	—	—	V	I_O = – 40μA
Output low level voltage*2	V_{OL}	—	—	0.4	V	I_O = 0.4mA
ON resistance*3*4	R_{ON}	—	—	5	kΩ	$\lvert V_{IN} - V_O \rvert$*5 = 0.25V
Current dissipation	I_{DD}	—	—	0.5	mA	CP = DC No load

∗1 Applied to DF, LOAD, CP, DI_1 and DI_{21} pins

∗2 Applied to DO_{20} and DO_{40} pins

∗3 Applied to O_1 to O_{40} pins

∗4 V_{DD} = 5V, V_2 = 2 / 3 V_{DD}, V_3 = 1 / 3 V_{DD}, V_5 = 0V

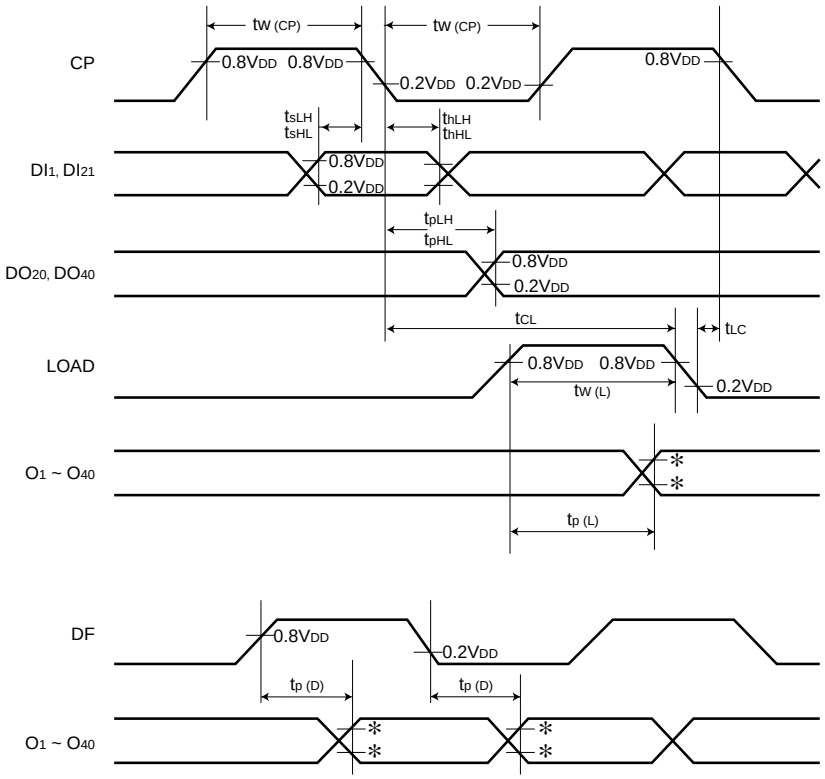
∗5 $V_{IN} = V_{DD}$, V_2, V_3, V_5, $V_o = O_n$ pin voltage

AC characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Propagation delay time 1	t_{pLH}, t_{pHL}	—	—	250	ns	CP → DO_n delay time
Propagation delay time 2*	$t_{p\,(L)}$	—	—	250	ns	Load → O_n delay time
Propagation delay time 3*	$t_{p\,(D)}$	—	—	250	ns	DF → O_n delay time
DI → CP setup time	t_{sLH}, t_{sHL}	50	—	—	ns	—
CP → DI hold time	t_{hLH}, t_{hHL}	50	—	—	ns	—
CP pulse width	$t_{w\,(CP)}$	125	—	—	ns	—
Load pulse width	$t_{w\,(L)}$	125	—	—	ns	—
CP → load time	t_{CL}	250	—	—	ns	—
LOAD → CP time	t_{LC}	0	—	—	ns	—
Maximum clock frequency	f_{CP}	3.3	—	—	MHz	DUTY = 50%

∗ V_{DD} = 5V, V_2 = 2 / 3V_{DD}, V_3 = 1 / 3V_{DD}, V_5 = 0V

○ Not designed for radiation resistance.



✻ $t_{p\,(L)}$ and $t_{p\,(D)}$ are times required before the O_1 to O_{40} output amplitude becomes 80% and 20% respectively.

Fig.2 AC characteristics waveform

●Application example

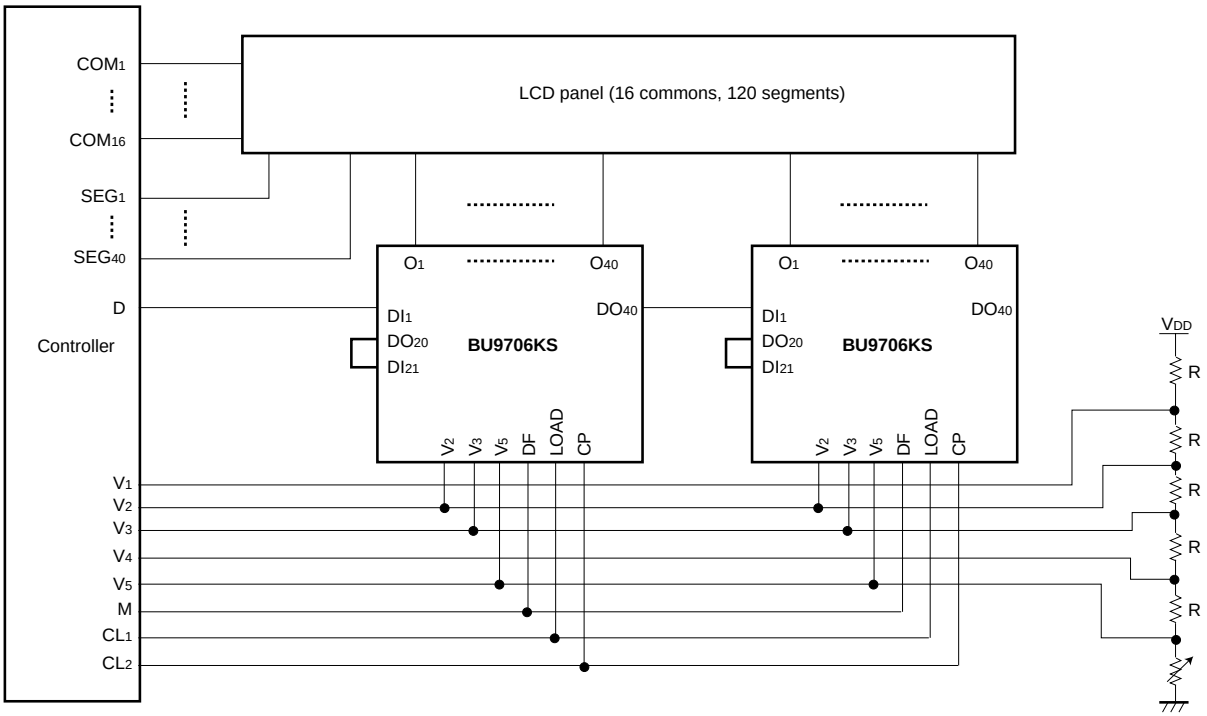
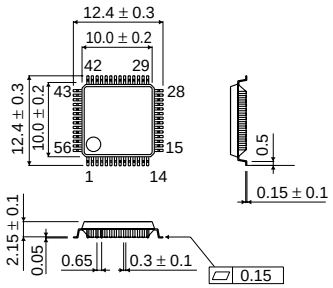


Fig.3

●External dimensions (Units: mm)



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