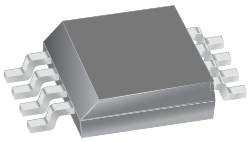
Automotive Quasi-Resonant Flyback Control IC

Features and Benefits

- Multiple output regulator
- 7 to 40 V input supply
- Low EMI conducted and radiated emissions
- Adaptive quasi-resonant turn on/off control
- Minimal number of external components
- Enable input which can be driven with respect to the battery voltage

Package: 8-pin narrow SOIC (suffix L)



Approximate Scale 1:1

Description

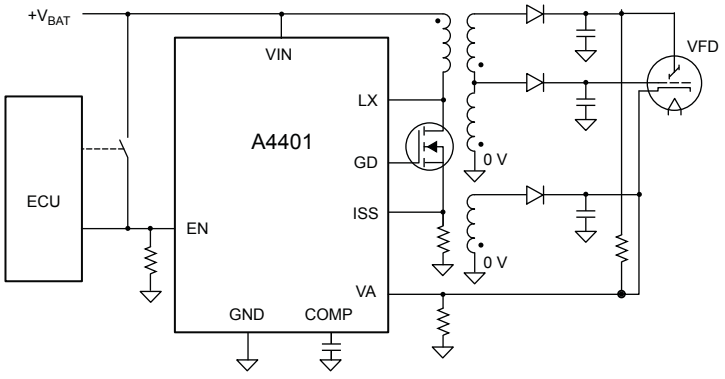
This device provides all the necessary control functions to provide the power rails for driving a vacuum fluorescent display (VFD) using minimal external components. The power supply is based on a quasi-resonant, discontinuous flyback converter, operating near the critical conduction boundary. A novel adaptive turn-on control scheme is used to optimize the turn-on and turn-off phase of the MOSFET, to reduce EMI emissions while minimizing switching losses.

The converter is self-oscillating, operating at switching frequencies depending on the input voltage, load, and external components. An onboard linear regulator that is powered directly from the battery provides the housekeeping supply, avoiding the need for complex bias supplies.

Internal diagnostics provide comprehensive protection against overloads, input undervoltage, and overtemperature conditions.

The A4401 is supplied in an 8-pin narrow SOIC package (suffix L), which is lead (Pb) free, with 100% matte-tin leadframe plating.

Typical Application



Selection Guide

Part Number	Packing
A4401KLTR-T	Tape and reel, 3000 pieces/reel

Absolute Maximum Ratings*

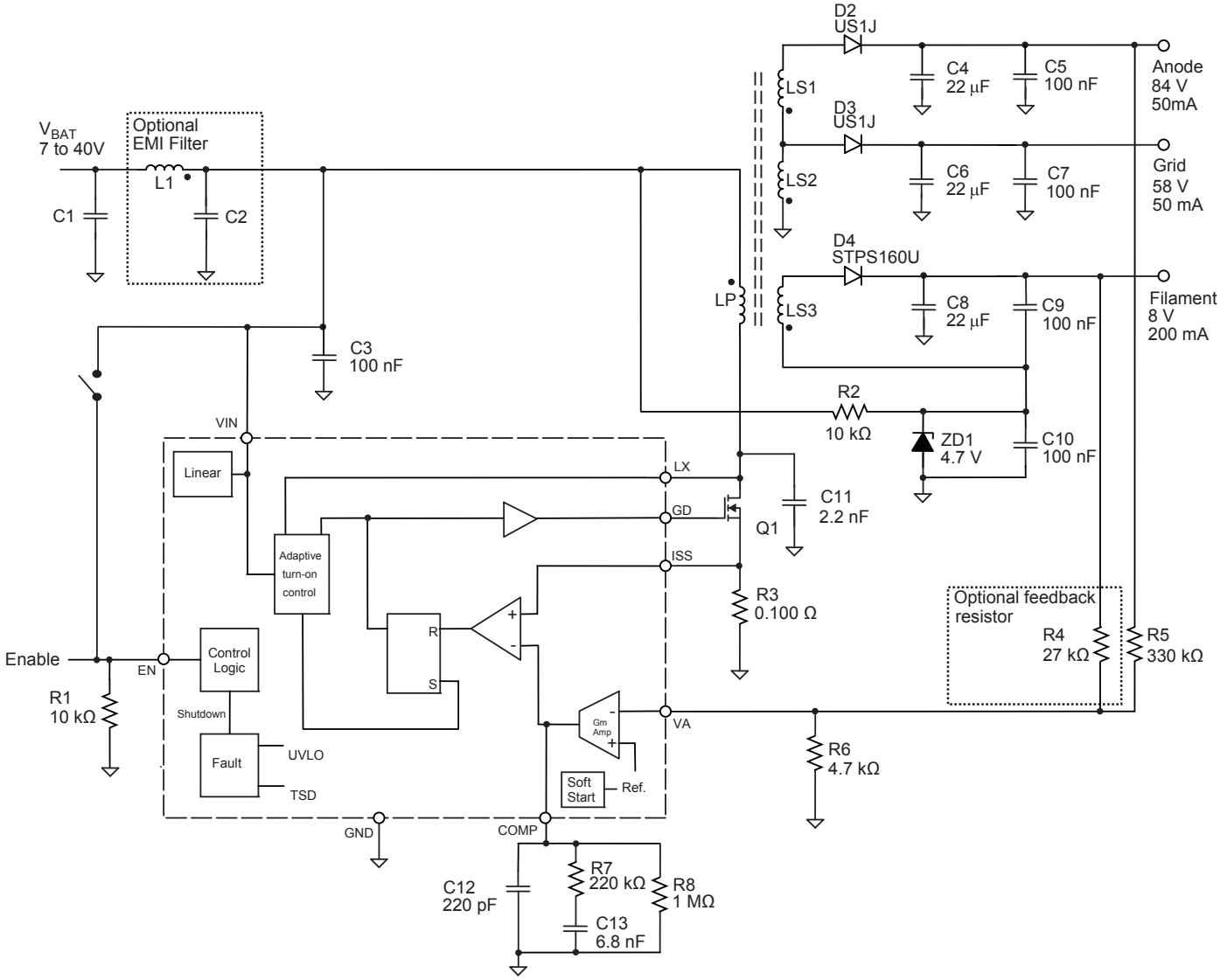
Characteristic	Symbol	Notes	Rating	Units
VIN Pin Voltage	V_{IN}		–0.3 to 40	V
LX Pin Voltage	V_{LX}		–0.6 to 60	V
ISS Pin Voltage	V_{ISS}		–1 to 1	V
EN Pin Voltage	V_{EN}		–0.3 to 40	V
VA Pin Voltage	V_{VA}		–0.3 to 5	V
ESD Rating – Human Body Model		AEC-Q100-002; all pins	2000	V
ESD Rating – Charged Device Model		AEC-Q100-011; all pins; inside	500	V
		AEC-Q100-011; all pins; corner	750	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	ºC
Junction Temperature	T_J		–40 to 150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

* With respect to ground

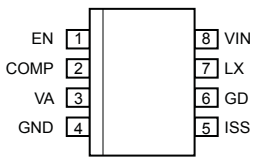
Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	4-layer PCB based on JEDEC standard	80	ºC/W

*Additional thermal information available on Allegro website.

Functional Block Diagram



Pin-out Diagram



Number	Name	Description
1	EN	Enable input; active high
2	COMP	Compensation node for Gm amplifier stage
3	VA	Output voltage feedback input
4	GND	Ground reference connection; connect to negative terminal of battery supply
5	ISS	MOSFET, Q1, current sense input
6	GD	MOSFET gate drive output
7	LX	Regulator switching node: MOSFET drive output
8	VIN	Supply input to power control circuit, MOSFET driver, and reference voltages

ELECTRICAL CHARACTERISTICS[1,2] valid at T_J = –40°C to +150°C, V_{IN} = 7 to 40 V (unless noted otherwise)

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Units
General						
VIN Quiescent Current	I_{INOFF}	EN = Low	–	–	10	µA
	I_{INON}	EN = High, no MOSFET switching	–	2.3	3.3	mA
LX Leakage Current	I_{LXLEAK}	EN = Low, V_{LX} = 40 V	–	–	1	µA
LX Input Bias Current	I_{LX}	EN = High, V_{LX} = 60 V	–	–	145	µA
Minimum Frequency	f_{SW}		25	35	45	kHz
Soft Start	t_{SS}		5	10	15	ms
Gate Drive						
Drive High Voltage, V_{IN} > 10 V	V_{GDH}		–	8.4	9.5	V
Drive High Voltage, 10 V > V_{IN} > 7 V			–	V_{IN} – 0.5	V_{IN} – 0.25	V
Rise Time, V_{IN} > 10 V	t_r	C_{LOAD} = 1 nF, 10% to 90% of V_{GS}= 9 V	–	60	–	ns
Rise Time, 10 V > V_{IN} > 7 V		C_{LOAD} = 1 nF, 10% to 90% of V_{GS}, V_{IN} = 7 V	–	90	–	ns
Fall Time, V_{IN} > 10 V	t_f	C_{LOAD} = 1 nF, 90% to 10% of V_{GS} = 0 V	–	30	–	ns
Fall Time, 10 V > V_{IN} > 7 V		C_{LOAD} = 1 nF, 90% to 10% of V_{GS}, V_{IN} = 7 V	–	40	–	ns
Current Sense Input						
Maximum Sense Voltage (Current Limit)	V_{CL}		600	800	1000	mV
Sense Input Bias Current	I_{ISS}	V_{ISS} = –300 mV to 1 V	–	–	10	µA
Current Sense Blanking	t_{BLANK}		100	145	190	ns
Reference Supply						
Reference Voltage Tolerance	V_{REF}		1.180	1.205	1.230	V
Operational Transconductance Amplifier						
Output Impedance	Z_{OP}		10	–	–	MΩ
Gm Constant[3]	K_{Gm}		–	470	–	µS
Output Source Current	I_{SRC}	V_{COMP} = 1.4 V, V_A = 1.06 V, T_A = 25°C	–30	–25	–20	µA
Output Sink Current	I_{SIN}	V_{COMP} = 1.4 V, V_A= 1.36 V, T_A = 25°C	20	25	30	µA
Input Bias Current	I_{BIAS}		–	–100	–	nA
Enable Input						
EN Input Low Voltage	V_{IL}		–	–	0.8	V
EN Input High Voltage	V_{IH}		2.4	–	–	V
EN Input Hysteresis	V_{Ihys}		200	500	–	mV
EN Input Current	I_{INL}	V_{IN} = 0 V	–10	–	10	µA
	I_{INH}	V_{IN} = 14 V	–	–	50	µA
		V_{IN} = 40 V	–	–	200	µA
Protection						
VIN Turn-On Threshold	V_{UVON}	Voltage rising	5.4	–	7	V
VIN Turn-Off Threshold	V_{UVOFF}	Voltage falling	4.9	–	6.5	V
Undervoltage Hysteresis	V_{UVhys}		–	0.5	–	V
Overtemperature Shutdown	T_{JSD}	Temperature increasing	–	165	–	°C
Overtemperature Hysteresis	T_{JSDhys}		–	15	–	°C

[1]For input and output current specifications, negative current is defined as coming out of (sourcing) the specified device pin.
[2]Specifications over operating temperature range are assured by design and characterization.
[3]Guaranteed by design.

Functional Description

Basic Operation

A peak current-mode control scheme is used to regulate one of the converter outputs, which will typically be the highest output voltage. The regulated output voltage is potentially divided down and fed into a Gm stage, where the resulting error signal acts as the control reference. This reference signal is compared against the signal that is produced by the inductor magnetization current flowing through the sense resistor.

As shown in figure 1, at the beginning of a switching cycle, the external MOSFET, Q1, is turned on. After the sense resistor signal reaches the control reference amplitude, the PWM comparator resets the synchronous rectification (SR) latch and turns off the MOSFET.

When the MOSFET is turned off, the voltage on the LX node rises until the voltage clamps at the battery voltage, V_{BAT}, plus the reflected output voltage, $V_{OUT(RFL)}$. The secondary rectification diodes are forward biased and the energy stored in the coupled inductor is released to the output circuits. During this period, the current through the inductor decreases linearly. As the current falls to 0 A, a resonance is set up between the primary magnetizing inductance and any capacitance appearing between the drain and ground. A damped voltage ringing occurs, which resonates around the battery voltage, V_{BAT}. As the resonant ring swings negative, the adaptive turn-on circuit monitors to detect the point at which the voltage reaches a minimum. At this point the MOSFET is commanded on, thereby minimizing the turn-on losses. Also, the relatively slow resonant dV/dt helps to reduce EMI.

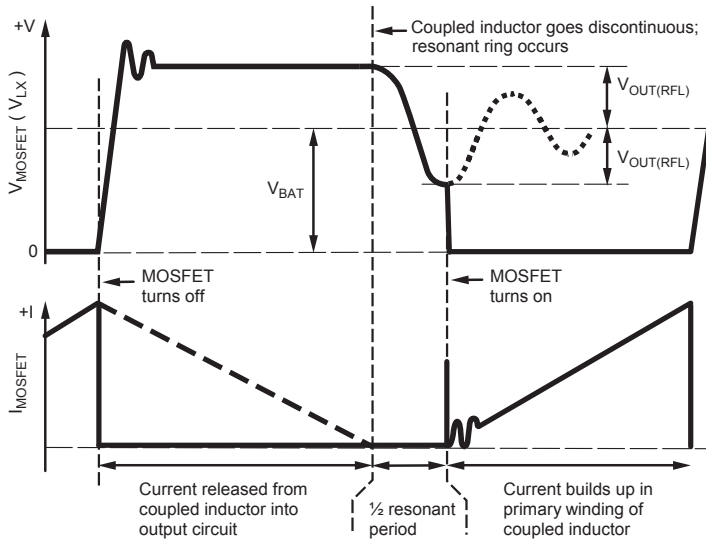


Figure 1. External MOSFET voltage and current

In most applications, the converter will be operated with a battery input voltage of 13.5 V. To optimize the performance of the regulator at this voltage, the magnetics can be designed to force 0 V across the MOSFET at turn-on. This minimizes switching losses and perhaps more importantly reduces EMI caused by voltage ringing due to the drain to ground capacitor resonating with the primary inductance. The voltage resonance at the MOSFET turn-off can be reduced by a simple low-loss R-C snubber, as described in the Electromagnetic Interference section.

If a small enough load is applied to the outputs, and the output of the Gm stage falls below a certain level, the converter will enter a burst mode of operation. Burst mode reduces switching losses while maintaining regulation of the outputs.

During startup, assuming the battery voltage is above the turn-on threshold and the EN input is enabled, the controller turns on. A soft start circuit controls the reference voltage, limiting the amount of current drawn on the input and the amount of charge transferred to the output, preventing voltage overshoot. During the initial phase of the soft start, very little or no voltage is present on the output. This means that there will be no resonant phase and the converter will operate in continuous-conduction mode. The converter effectively operates in constant-current mode until regulation is achieved.

In the event of an overload, the current demand signal produced by the Gm amplifier restricts the output current by introducing pulse-by-pulse current limiting.

Regulation Voltage

The feedback resistors, R5 and R6, determine the voltage of the output rail to which they are connected, according to the following formula:

$$V_{OUT} = \frac{V_{REF} \times (R5 + R6)}{R6} \quad , \tag{1}$$

where R6 should be approximately 5 kΩ.

The internal 1.2 V reference has a ±2% worst case tolerance, plus there is an input bias current, I_{BIAS}, on the feedback node, VA, that has a small influence. This current flows into the ground referenced resistor, R6, creating a small voltage offset.

In applications where the main control output (anode or grid) can run at relatively light loads (relative to the filament load), it may be necessary to "mix" the feedback signal. This involves adding an additional feedback from the filament output to the VA input. Note that this only applies to DC filament outputs.

R3 Current Sense Resistor Selection

To determine the resistance value, the maximum peak current needs to be determined. First determine the average input current, I_{AV}, as follows:

$$I_{AV} = \frac{P_{OUT}(max)}{\eta\% \times V_{IN}(max)} \quad , \tag{2}$$

where P_{OUT} is the output power. Then, the peak current through the sense resistor:

$$I_{PK} = \frac{2 \times I_{AV}}{D(max)} \quad , \tag{3}$$

where D is limited to 0.7, or can be precisely found as described in the Magnetics Design section. Note that a D of 0.7 is chosen in order to achieve 0 V switching with a V_{BAT} of 13.5 V.

To determine the sense resistor value, assume that the minimum sense voltage before current limiting occurs is 600 mV. A reasonable maximum voltage to select during normal operation would be 500 mV. Then, the resistor value can be found as follows:

$$R_{SENSE} = \frac{500\ mV}{I_{PK}} \quad . \tag{4}$$

The power losses in the resistor can be found by first determining the rms current through it:

$$I_{RMS} = I_{PK} \times \left(\frac{D(max)}{3} \right)^{1/2} \quad . \tag{5}$$

Then, the losses in sense resistor are:

$$P_{RDS} = I^2_{RMS} \times R_{SENSE} \quad . \tag{6}$$

The power rating of the resistor can be selected based on the power dissipation. When selecting a resistor it is worth noting that the maximum power rating is valid up to 70°C and derates linearly to 0 W at a temperature of typically between 120°C and 140°C. Check the resistor manufacturer guidelines.

Note that is imperative that this resistor be a low inductance type; avoid wire wound. Standard surface mount devices are usually acceptable.

Soft Start

When power is initially applied, assuming the input voltage turn-on threshold is reached, and the EN input is enabled, the controller is initiated and the MOSFET, Q1, is turned on for the first switching cycle. Initially, while the output volts are rising towards the target regulation point set by the soft start circuit, the MOSFET will run at current limit.

During a soft start cycle, the reference voltage is ramped from 0 to 1.2 V in 32 steps over a period of 10 ms under the control of a DAC. This forces the output of the amplifier to vary between 0.8 and 1.5 V, which in turn reduces the effects of inrush current and voltage overshoot on the outputs.

If there is a special requirement for larger output capacitors, and the onboard soft start is insufficient, an external soft start can be introduced. This can be implemented by "pulling" down the amplifier output (COMP pin) and then "releasing" it gradually over the duration of the new soft start period. The pull-down circuit has to be capable of sinking at least 30 µA.

Q1 MOSFET Selection

In general, the higher the R_{DS} and the smaller the package, the lower the cost of the MOSFET, Q1. On the basis of selecting a MOSFET to minimize cost, it is important to understand the power losses associated with it.

When selecting the R_{DS}, it is important to consider its value at minimum battery voltage, as it tends to increase with low V_{GS} values. Below a battery voltage, V_{BAT}, of 10 V, the actual drive amplitude, V_{GS}, is V_{BAT} minus 500 mV (worst case). MOSFET suppliers usually quote the variation of R_{DS} with V_{GS} amplitude. Another factor that influences the "real" R_{DS} is the operating temperature. At a temperature of 140°C, this figure is increased by approximately 1.8. Again, manufacturers will provide this information.

Worst case losses will occur at minimum battery voltage and maximum load. These can be considered in terms of static losses, switching turn-off losses, and switching turn-on losses:

Static Losses The rms current, I_{RMS}, that flows in the MOSFET is identical to the current that flows in the sense resistor previously calculated. Therefore:

$$P_{STATIC} = \left[I_{PK} \times \left(\frac{D(\max)}{3} \right)^{1/2} \right]^2 \times R_{DS} \quad . \tag{7}$$

Switching Turn-Off Losses Assume that the turn-off threshold, V_{TH}, is similar to where the Miller "plateau" effect takes place. Figure 2 illustrates how an approximation can be made in terms of the turn-off losses. The duration of the t_{loss} region is determined by how long the driver takes to remove the Miller (gate to drain) charge. The Miller charge, Q_{GD}, is quoted in the MOSFET datasheet.

The driver capability can be found from data in the Electrical Characteristics table, as follows. At turn-off, the driver can shift a charge of (7 V – 0.5 V) × 1 nF, in 40 ns. The drive current required to do this is:

$$I_{DRIVE} = \frac{6.5\ \text{V} \times 1\ \text{nF}}{40\ \text{ns}} = 163\ \text{mA} \tag{8}$$

Then, the time, t_{LOSS}, taken to shift the Miller charge can be found:

$$t_{LOSS} = \frac{Q_{GD}}{I_{DRIVE}} \quad . \tag{9}$$

The turn-off switching loss can now be estimated:

$$P_{TURNOFF} = I_{PK} \times \frac{V_{DS}}{2} \times t_{LOSS} \times f_{SW}(\min) \quad , \tag{10}$$

where $f_{SW}(min)$ is specified in the Electrical Characteristics table and the peak current, I_{PK}, is identical to the current that flows in the sense resistor, the calculation of which is shown in the Current Sense Resistor Selection section. V_{DS} is calculated in the next section.

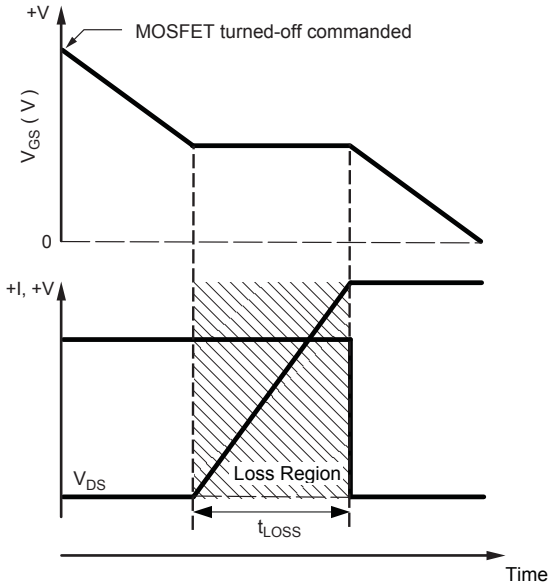


Figure 2. MOSFET, Q1, loss approximations

Switching Turn-On Losses The turn-on losses are determined by the amount of energy the resonant capacitor, C11, has to discharge into the MOSFET. At low battery voltage, the resonant swing should force the volts across the capacitor to only a few volts, making this loss negligible.

Total Losses The total MOSFET power loss can be estimated as follows:

$$P_{TOTAL} = P_{STATIC} + P_{TURNOFF} \quad . \tag{11}$$

The thermal resistance, $R_{\theta JA}$, can be determined by two methods. One is by estimating a maximum junction temperature, T_J(max). The other is to test for the operating junction temperature, using the given device package mounted on a printed circuit board with copper trace area connected to the device. $R_{\theta JA}$ is then calculated as follows:

$$R_{\theta JA} = \frac{T_J - T_A}{P_{TOTAL}} \quad . \tag{12}$$

The drain-to-source rating, V_{DS}, is the sum of the maximum input voltage, V_{BAT}(max), plus the reflected output voltage. Adequate margin should also be added, to allow for tolerancing effects and parasitic voltage ring. It can be calculated as follows:

$$V_{DS} = \left(V_{OUT} \times \frac{N_P}{N_{OUT}} \right) + V_{BAT}(\max) \quad . \tag{13}$$

D2, D3, and D4 Output Diodes Selection

For the low voltage outputs such as the filament supply, it is recommended that a Schottky diode be used. For the higher voltage rails, ultrafast rectifier diodes are recommended.

For each output, estimate the maximum reverse voltage, V_{RRM}, and the maximum average current that the diode is subjected to. The V_{RRM} rating should exceed at least 20% of the maximum V_{DIODE} voltage, calculated as follows:

$$V_{DIODE} = V_{BAT}(\max) \times \frac{N_{S1}}{N_P} + V_{OUT} \quad . \tag{14}$$

The maximum average current through the diode is simply the maximum load current. The diode should be rated to handle this current with some margin.

In addition, the diode should be able to handle the power dissipation. The majority of the power loss is simply the static loss:

$$P_{STATIC} = V_f \times I_{LOAD} \quad . \tag{15}$$

The forward voltage drop, V_f, can be found from the diode characteristics at maximum load.

C1 Input Capacitor Selection

In the interests of cost and performance, it is recommended that ultralow impedance electrolytic capacitors be used. The ratio of the source impedance to the impedance of the input capacitor will determine how much of the input current is drawn from the input capacitor. For example, if the source impedance is relatively high, then the input capacitor would have to supply the triangular current that flows through the primary winding, the MOSFET Q1, and the current sense resistor. This rms current was worked out in the Current Sense Resistor Selection section.

Electrolytic capacitors experience heating effects caused by the rms current flowing through the ESR of the device. The maximum rms current is normally quoted at 100 kHz and 105°C. Frequency correction factors for the ripple current are provided when the operating frequencies are less than 100 kHz. A 50 VDC rating should be adequate for most applications.

C4, C6, and C8 Output Capacitors Selection

The overall equivalent capacitance on the output should not be less 22 µF (see Control Loop section

for more information). The current that flows in and out of the capacitor is similar to the current that flows through the corresponding rectifier diode.

Worst case power dissipation due to the ESR will occur at V_{BAT}(min) and maximum load. The duty cycle under these conditions is a maximum of 0.7.

The rms current in the capacitor can be found as follows:

$$I_{RMS} = 4 \times I_{LOAD} \times \left(\frac{0.7}{3} \right)^{½} \quad . \tag{16}$$

When selecting a suitable capacitor, the rms current rating should have reasonable margin with respect to the above value. In addition, the current rating should be derated to take into account the frequency correction at values of less than 100 kHz.

The impedance of the output capacitor will affect the amount of voltage ripple and noise that appears on the output. The impedance is composed of two components: ESR and reactance, X_C. Even with a modest amount of capacitance on the output, the ESR will tend to dominate the overall impedance.

The ESR can be estimated by multiplying the capacitance reactance by the dissipation factor, DF (tan δ):

$$ESR = \frac{1}{2 \times \pi \times f_{SW} \times C_{OUT}} \times DF \quad . \tag{17}$$

Note that DF is normally quoted at 25°C, however, it is usually fairly constant as the temperature is increased.

The peak to peak voltage can then be found:

$$V_{pk\text{-}pk} = ESR \times I_{LOAD} \times 4 \quad . \tag{18}$$

The voltage rating should be chosen to provide at least a 20% margin above the maximum output voltage.

Control Loop

As the converter operates in discontinuous mode, the inductor does not feature in the power stage. The power stage effectively contains one pole formed by the output capacitors and loads.

In terms of "closing the loop," the optimal shaping components are shown in the Functional Block diagram, connected to the COMP pin. The control loop is optimized for an equivalent output capacitor of 22 µF. Larger capacitor values can be used, however, those will tend to reduce the bandwidth of the control loop. Smaller values should not be used, as they may cause instability issues.

Magnetics Design

The following are the known variables:

- Maximum output power, P_{OUT}.
- Minimum battery voltage, V_{BAT}(min).
- Minimum switching frequency, f_{SW}(min). This occurs at V_{BAT}(min) and maximum load. Note, it is recommended that the lowest possible switching frequency be used, in order to minimize switching losses and to shift the differential harmonics down the frequency spectrum. This is a compromise with the sizing of the magnetics and filtering components.
- Maximum duty cycle. This should typically not exceed 0.7, in order to avoid excessive losses in the secondary output circuits.
- Efficiency of converter, η%, at V_{BAT}(min). This will typically be between 80% and 85%.
- Resonant capacitor, C11, connected between the LX pin and ground. The resonant half period of 1 µs may be achieved with the parasitic capacitance that exists in the circuit. Fine tuning can be performed by adding additional capacitance.
- Known magnetic core set. Material selection should be based on performance at elevated temperature, and include consideration of flux density, losses, Curie temperature, and so forth.

- Magnetics sizing can be determined using techniques such as area product or geometric product, or by following manufacturers guidelines, usually in the form of nomograms.

To simplify the design process, the resonant switching transition is ignored and the calculations are based on the switcher operating at the boundary condition of continuous/discontinuous conduction. This is a reasonable assumption as the resonant period forms a small percentage of the overall period at minimum line voltage and maximum load (where the magnetics are designed because of worst case conditions).

The objective of the design is to achieve 0 V switching when V_{BAT} = 13.5 V (note that this voltage can be adjusted for any value). At V_{BAT} voltages of less than 13.5 V, 0 V switching is still achieved. In addition, the LX voltage is prevented from swinging negative as the MOSFET, Q1, is commanded on as soon as 0 V is reached.

To ensure that the reflected output voltage forces the LX node to 0 V, the following condition must be met:

$$n = \frac{V_{OUT}}{13.5} \quad , \tag{19}$$

where n is the step-up turns ratio from primary to controlled output.

Worst case conditions in terms of core saturation occur when V_{BAT} is at a minimum and duty cycle, D, a maximum:

$$D(\max) = \frac{V_{OUT}}{(V_{BAT}(\min) \times n) + V_{OUT}} \quad . \tag{20}$$

The primary magnetizing inductance can be determined from the following formula, which is derived by equating the input energy to the output energy times the efficiency:

$$L_{PRI} = \frac{\eta}{2 \times f_{SW}(\min) \times P_{OUT}} \times (V_{BAT}(\min) \times D(\max))^2 \quad . \tag{21}$$

Then, maximum peak current can be found:

$$I_{PEAK}(\max) = \frac{V_{BAT}(\min) \times D(\max)}{f_{SW}(\min) \times L_{PRI}} \quad . \tag{22}$$

The worst case operating flux density, B_{OP}, can be found from the ferrite core manufacturers datasheet, by taking the saturation flux density, B_{SAT}, at elevated temperatures and subtracting a margin, approximately 15% , to allow for operation in current limit mode or during startup.

After an appropriate magnetic core set has been selected, the number of turns required on the primary winding can be found:

$$N_P = \frac{V_{BAT}(\min) \times D(\max)}{f_{SW}(\min) \times B_{OP} \times A_e} \quad . \tag{23}$$

where A_e is the magnetics cross-sectional area in m^2.

The number of secondary turns can be derived through the turns ratio found previously:

$$N_{S1} = n \times N_P \quad . \tag{24}$$

If there is more than one output, the additional secondary windings are simply scaled from the main secondary as shown in the following formula:

$$N_{S2} = N_{S1} \times \frac{V_{OUT2}}{V_{OUT1}} \quad , \tag{25}$$

where:

N_{S2} is the quantity of turns in the additional windings,

V_{OUT1} is the output voltage from main winding, and

V_{OUT2} is the output voltage from any additional windings.

The total air gap, l_g, can be found. First, an approximate air gap, l_g(approx), is found before flux fringing is taken into account. Given:

$$\mu_O = 4\pi \times 10^{-6} \quad , \tag{26}$$

then:

$$I_g(\text{approx}) = \frac{\mu_O \times A_e \times N_P^2}{L_P} \quad . \qquad (27)$$

Because of flux fringing effects, the above air gap should be modified, according to the following formulas. Given:

$$F = \frac{I_g(\text{approx})}{A_e^{½}} \times \ln\left(\frac{2 \times G}{I_g(\text{approx})}\right) \quad . \qquad (28)$$

where l_g(approx) is the previously calculated approximate air gap, and G is the bobbin width (the effective winding width).

then the total air gap can now be found:

$$I_g = I_g(\text{approx}) \times (1+F) \quad . \qquad (29)$$

Note that most ferrite core manufacturers provide a limited number of air gap sizes. It is therefore recommended to select a standard size. Size is indicated in terms of the Al factor, which is expressed in L/N^2 units. The Al factor can be derived from the above two formulae.

To minimize flux leakage effects, it is recommended that the air gap should be located on the center limb. If, however, a distributed air gap is used, the air gap figure should be divided by two.

Some applications require an AC filament output. Typically this may be a center tapped winding with the center tap held at some bias voltage. During the MOSFET off-time, the output voltage of the control winding is simply reflected through the turns ratio of the magnetics.

During the on-time of the MOSFET, the windings are driven as a forward converter because there is no rectifying diode to isolate this action. The voltage during this interval is simply the battery voltage transformed by the turns ratio of the filament winding and the primary winding. This means that as the battery voltage varies, there will be a variation in the filament voltage. However, this variation will be less than those arising in other converter topologies because, during the MOSFET off-time, the voltage is regulated.

The voltage amplitude across the filament winding is:

$$V_{FIL} = V_{BAT} \times \frac{N_{SF}}{N_P} + V_{OUT1} \times \frac{N_{SF}}{N_{S1}} \quad , \qquad (30)$$

where:

N_{SF} is the number of turns on the filament winding,

N_{S1} is the number of turns on the main controlled output winding, and

V_{OUT1} is the output voltage of the main controlled output.

It is probably desirable to optimize the filament voltage at nominal battery conditions; for example, at V_{BAT} = 13.5 V.

Due to the low voltage out, the number of integer turn combinations is limited. So, the filament voltage may not be exact. The turns range may only be 2 or 3.

The magnetic wire sizing for each winding is determined by the ampere-turns ratio as a proportion of the total ampere-turns of all the windings. The amount of bobbin area available for the windings is influenced by the amount of insulation required, the winding construction technique, and the packing density of the circular wire. A conservative utilization factor is 0.5, that is, 50% of the bobbin window area filled with copper.

The rms current of each winding has to be determined. The worst case condition is at minimum input voltage and maximum load.

The primary winding current is identical to the current flowing in the current sense resistor (see the Current Sense Resistor Selection section). The current in each of the other output windings can be found as follows.

Given:

$$I_{PK} = \frac{2 \times I_{OUT}}{D'(\text{max})} \quad , \qquad (31)$$

where I_{OUT} is the maximum load current, and D'(max) is the duty cycle, limited to 0.3.

Then the rms current in the winding is:

$$I_{RMS} = I_{PK} \times \left(\frac{D'}{3} \right)^{½} \quad , \tag{32}$$

Because the number of turns has already been worked out, the ampere-turns factor can now be determined.

After all of the ampere-turns are known for each winding, the bobbin window can be apportioned to each winding. It is recommended that the current density in each winding should be kept below 5 A per mm^2.

Another consideration when selecting the wire gauge is the skin depth (depth within which the current flows), especially at higher frequencies. Skin depth can be calculated as:

$$\delta = \frac{75}{f_{SW}^{½}} \quad , \tag{33}$$

For example, if 45 kHz were the minimum frequency at minimum input voltage and maximum load, then to ensure maximum wire utilization for the first four switching harmonics, the switching frequency would be 180 kHz. The conduction depth at 180 kHz would equal 0.18 mm, therefore, the wire diameter should not exceed 0.36 mm. For any particular winding, if the current rating of the wire is insufficient even though the wire meets the skin depth criteria, multiple wires wound in parallel will be necessary.

It is recommended to locate the start and finish of each winding as close as possible on the bobbin. This minimizes the “loop area” and reduces the effects of noise pick-up.

When winding the high voltage windings, such as for the anode or grid, it is advisable to insert a layer of polyester insulating tape between each layer as well as between adjacent windings.

C11 Resonant Capacitor Selection

The resonance that occurs when the MOSFET, Q1, turns off is formed by the interaction of the primary magnetizing inductance and the capacitance between the LX node (the drain terminal of the MOSFET) and ground. The design is optimized for a half resonant period of 1 µs. This means the resonant capacitor value can be found from the following formula:

$$C_{RES} = \left(\frac{T_R}{\pi} \right)^2 \times \frac{1}{L_{PRI}} \quad , \tag{34}$$

where T_R is a half resonant period of 1 µs.

It is advisable to measure the half resonant period in the application, as the parasitic capacitance between the LX node and ground can be substantial and may even be sufficient to meet the requirements with very little additional capacitance.

PCB Layout Guidelines

The layout can be considered as two blocks: primary and secondary:

Primary Block To minimize parasitic noise appearing on the ground return, and at the LX and ISS nodes, as well as to maximize the effectiveness of the EMI

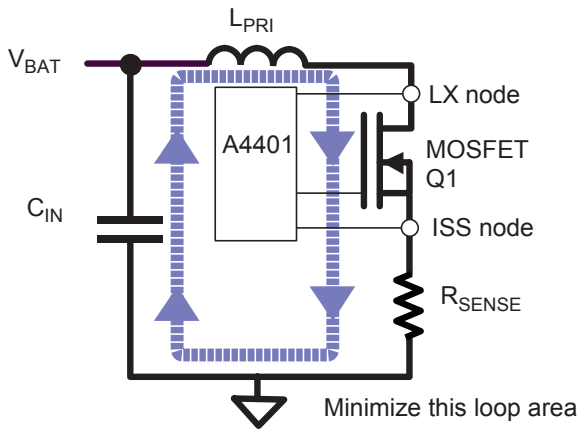


Figure 3. Main power loop

filtering, it is imperative that the "power loop" formed by the input filter, primary winding, MOSFET, Q1, and sense resistor is as short and "tight" as possible. This means components should be placed as close together as possible, and the loop area should be minimized, in order to reduce the effects of magnetic pickup and noise generation at higher frequencies. A ground plane is not necessary, however, a good star ground connection should be formed between the input filter capacitor and the sense resistor. Circuit traces should be as wide as possible, in order to minimize leakage inductance. Figure 3 illustrates the main power loop.

A local ground plane around the A4401 can be used to minimize ground bounce issues. This can be done with a simple connection from the ground pin of the A4401 to the star ground, being careful to avoid any connection between this local ground plane and the power loop.

The compensation components connected to the COMP pin, the filter capacitor connected to VIN, the feedback resistors connected to VA, and the resonant capacitor connected to LX should be located as close to their respective pins as possible. In addition, the length of the traces between those components and ground should be as short as possible.

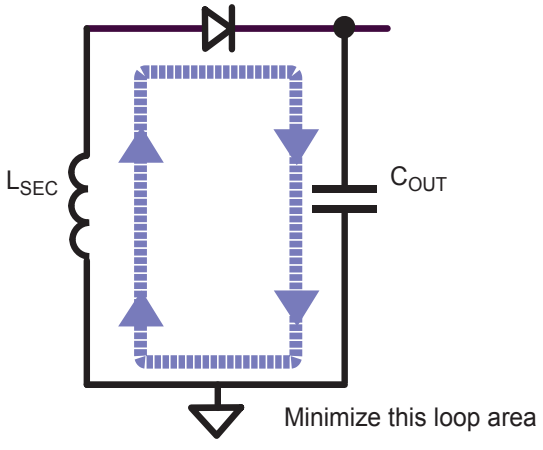


Figure 4. One of three output power loops

Secondary Block Each output power circuit should be laid out with identical principles relative to the primary side power circuit, that is, with each secondary winding, rectifying diode, and output capacitor positioned close together and forming a tight loop.

The high voltage output circuits should be kept well away from all the control circuitry. It is recommended that good connections be made between each of the local output grounds and the star ground. In addition, all of the output grounds should be connected together via wide traces and not ground planes. Figure 4 illustrates one of the output loops.

The feedback resistor connected to the regulated output rail should be located as close to the VA pin as possible. The PCB trace that connects the top of this resistor to the output rail should not be located near any of the output power loops or ground connections.

Electromagnetic Interference

Some of the previous sections provide information on reducing EMI in terms of input filter capacitance selection, magnetics design (to achieve zero voltage switching at nominal input voltage), and board layout. This section provides some additional advice on reducing EMI.

Effects of Magnetics Design on 0 V Switching Figure 5 illustrates a converter running at full power with V_{BAT} = 13.5 V. The upper trace is the voltage across LX and the lower trace is the voltage across the sense resistor (essentially the current through the primary winding and the MOSFET, Q1). The magnetic set in this case was designed to achieve 0 V switching at a V_{BAT} of 7 V.

It can be seen that at MOSFET turn-on there is a considerable sinusoidal ringing on the voltage sense, in the region of 3 MHz. In addition, there is a considerable ringing during the MOSFET turn-off, in the region of 6 MHz. These ringing effects are caused by the primary-to-secondary leakage inductance interacting with parasitic capacitance. These noise sources will probably have an impact on the conducted emissions and should therefore be suppressed.

By rescaling the magnetics so that 0 V switching is achieved with V_{BAT} = 13.5 V, the turn-on ringing is almost completely damped, as shown in Figure 6. Because the resonant capacitor, C11, had discharged to 0 V before switching, there was effectively little energy left.

The turn-off noise is also improved dramatically as well. It can be seen that the ringing amplitude is lower, dampens more quickly, and the ringing frequency is higher making it easier to snub (see the Radiated Emissions on the LX Node subsection). The reason for this effect is that a lower step-up ratio is required to achieve the output voltage. This improves the magnetic coupling coefficient and therefore the leakage inductance is reduced.

Running the system with a lower turns ratio means that the duty cycle is greater. The advantage of this is that the peak current is lower, resulting in lower turn-off switching losses and reduced harmonics of the input current, thus reducing the conducted emissions.

Radiated Emissions on LX Node A potential source of radiated emissions is turning off the MOSFET. A resonance is set up between the leakage inductance of the magnetics and the parasitic capacitance on the LX node. Assuming the magnetics are well designed in terms of reducing leakage inductance, this resonance should occur in the region of tens of megahertz. Another potential source of radiated emissions is turning off the output rectifying diodes. The following procedure can be applied to address both issues.

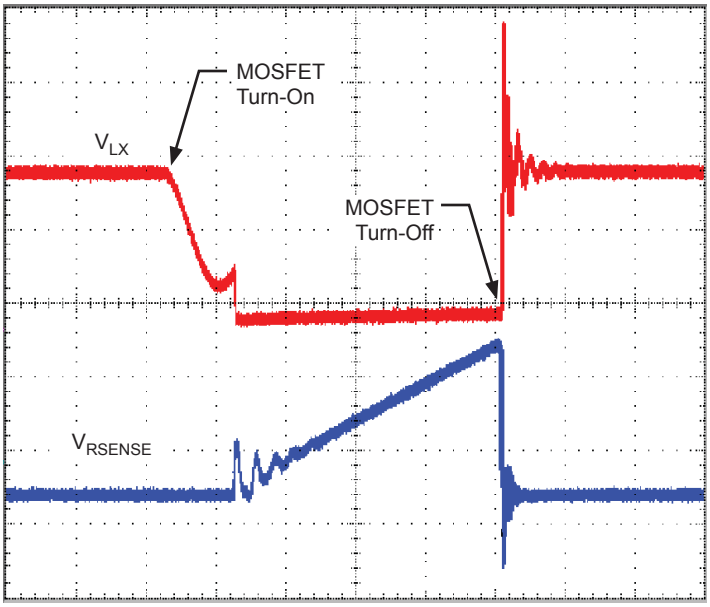


Figure 5. Voltages with 0 V switching of Q1 at V_{BAT} of 7 V

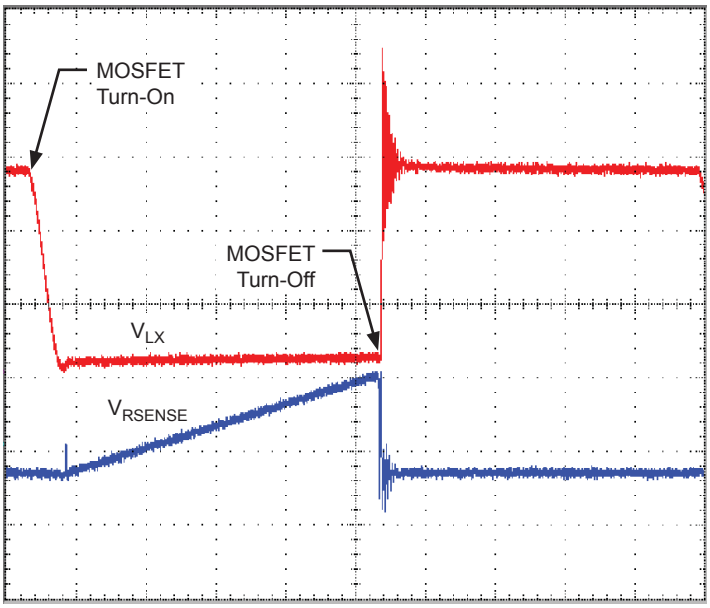


Figure 6. Voltages with 0 V switching of Q1 at V_{BAT} of 13.5 V

A simple low-loss R-C snubber can be deployed to dampen these oscillations. To do so, follow these simple steps to determine the component values required:

1. Measure the voltage resonant frequency, f_{RES}, on the LX node.
2. Add an additional capacitance (C11) between LX and ground until the resonant frequency is halved, $f_{RES}/2$:

$$f_{RES} = \frac{1}{2 \times \pi \times (L_{LEAK} \times C_{LEAK})^{½}} , \quad (35)$$

$$\frac{f_{RES}}{2} = \frac{1}{2 \times \pi \times (L_{LEAK} \times C_{NEW})^{½}} , \quad (36)$$

$$C_{NEW} = C_{LEAK} + C_{ADD} , \quad (37)$$

where:

C_{ADD} is the additional capacitance added,

C_{LEAK} is the parasitic capacitance, and

L_{LEAK} is the parasitic inductance.

Note that the value of the additional capacitance should be in the region of a few hundredths of picofarads.

3. Now to calculate component values that will result in $f_{RES}/2$, first calculate C_{LEAK}, given:

$$C_{LEAK} + C_{ADD} = 4 \times C_{LEAK} , \quad (38)$$

$$C_{LEAK} = \frac{C_{ADD}}{3} . \quad (39)$$

4. With C_{LEAK} solved, solve for L_{LEAK}
5. Finally, solve for the characteristic impedance of the parasitic components:

$$R_O = \left(\frac{L_{LEAK}}{C_{LEAK}} \right)^{½} . \quad (40)$$

R_O can be selected as the damping resistor value (not shown in functional block diagram). Typically a $^1/_8$ W resistor is adequate.

Figure 6 illustrates a converter running at full power with V_{BAT} = 13.5 V. The upper trace is the voltage across LX and the lower trace is the voltage across the sense resistor, R3. It can be seen that at turn-on, the noise is very low, as the resonant action introduces a very slow voltage slew which reaches 0 V before the MOSFET is turned on. This action ensures minimal noise is produced. However, at turn-off there is a high frequency ringing of 25 MHz which could cause issues in terms of complying with radiated emissions.

Figure 7 illustrates the effects of adding an R-C snubber (R = 30 Ω and C = 330 pF in series between the LX pin and GND). It can be seen that, through the addition of the snubber, the turn-off ringing has been considerably damped. This was achieved with almost negligible additional power loss.

Conducted Emissions To help reduce the conducted emissions, an EMI filter may be necessary as shown in the Functional Block diagram.

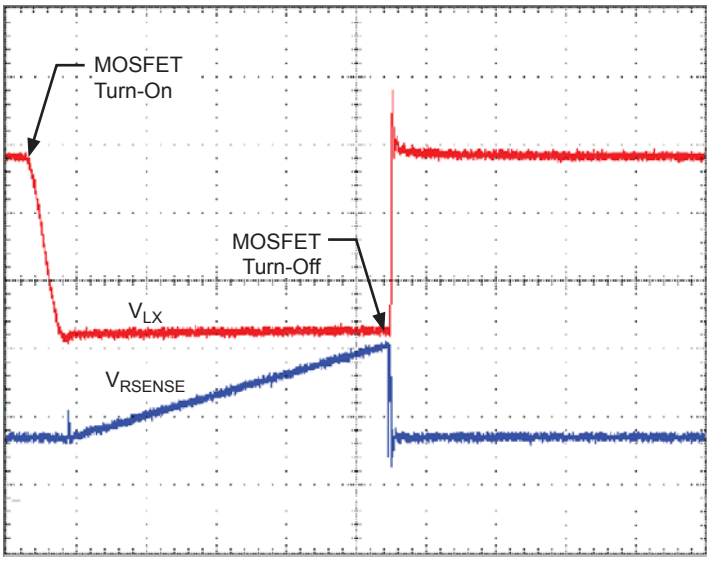
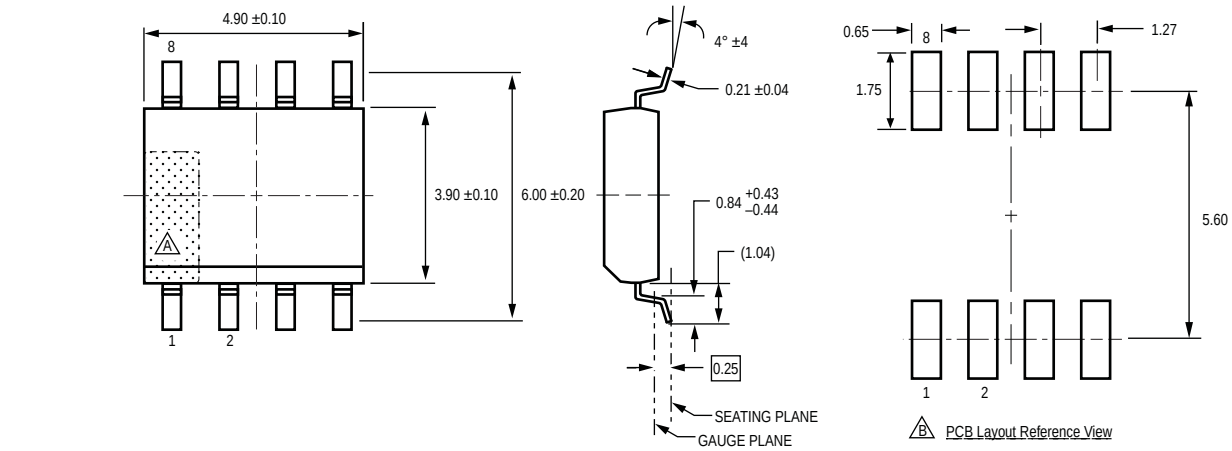


Figure 7. Voltages with 0 V switching of Q1 with an R-C snubber

The capacitance selection has been dealt with in the Input Capacitor Selection section. In terms of selecting an inductance, generally the higher the inductance the better as far as noise rejection of the differential conducted emissions is concerned. However, a large inductance usually means additional cost and increased size, therefore, it is advisable to select an inductance as large as possible within the constraints of board space and cost.

The maximum average current that flows through the inductor is similar to the maximum average current that was worked out in the Current Sense Resistor Selection section. Both the rms and saturation current ratings of the inductor selected should be higher than the maximum average current. Care should be taken when selecting inductors for operation at elevated temperatures, because some manufacturers rate their parts using only self-generated heating, giving the impression of operability at higher temperature conditions.

Package L, 8-Pin Narrow SOIC



For Reference Only
(reference JEDEC MS-012 AA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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