18Mb Pipelined DDR™II SRAM Burst of 2

IDT71P71804
IDT71P71604

Features

- 18Mb Density (1Mx18, 512kx36)
- Common Read and Write Data Port
- Dual Echo Clock Output
- 2-Word Burst on all SRAM accesses
- Multiplexed Address Bus
  - One Read or One Write request per clock cycle
- DDR (Double Data Rate) Data Bus
  - Two word bursts data per clock
- Depth expansion through Control Logic
- HSTL (1.5V) inputs that can be scaled to receive signals from 1.4V to 1.9V.
- Scalable output drivers
  - Can drive HSTL, 1.8V TTL or any voltage level from 1.4V to 1.9V.
  - Output Impedance adjustable from 35 ohms to 70 ohms
- 1.8V Core Voltage (V_{DD})
- 165-ball, 1.0mm pitch, 13mm x 15mm fBGA Package
  JTAG Interface

Description

The IDT DDRII™ Burst of two SRAMs are high-speed synchronous memories with a double-data-rate (DDR), bidirectional data port. This scheme allows maximization of the bandwidth on the data bus by passing two data items per clock cycle. The address bus operates at single data rate speeds, allowing the user to fan out addresses and ease system design while maintaining maximum performance on data transfers.

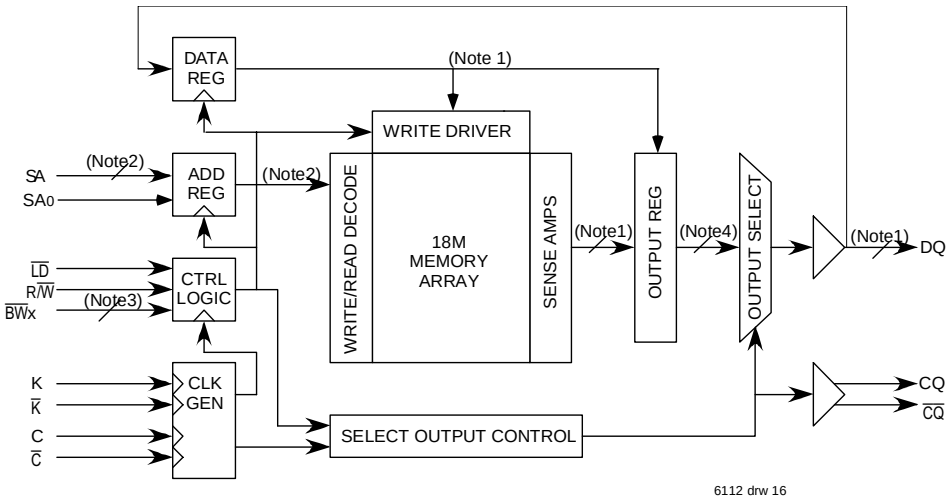
The DDRII has scalable output impedance on its data output bus and echo clocks, allowing the user to tune the bus for low noise and high performance.

All interfaces of the DDRII SRAM are HSTL, allowing speeds beyond SRAM devices that use any form of TTL interface. The interface can be scaled to higher voltages (up to 1.9V) to interface with 1.8V systems if necessary. The device has a V_{DDQ} and a separate Vref, allowing the user to designate the interface operational voltage, independent of the device core voltage of 1.8V V_{DD}. The output impedance control allows the user to adjust the drive strength to adapt to a wide range of loads and transmission lines.

Clocking

The DDRII SRAM has two sets of input clocks, namely the K, $\overline{K}$ clocks and the C, $\overline{C}$ clocks. In addition, the DDRII has an output "echo" clock, CQ, $\overline{CQ}$.

Functional Block Diagram



Notes

1) Represents 18 signal lines for x18, and 36 signal lines for x36
2) Represents 20 address signal lines for x18 and 19 address signal lines for x36.
3) Represents 2 signal lines for x18 and 4 signal lines for x36.
4) Represents 36 signal lines for x18 and 72 signal lines for x36.

APRIL 2009

The K and $\overline{K}$ clocks are the primary device input clocks. The K clock is used to clock in the control signals ($\overline{LD}$, R/$\overline{W}$ and $\overline{BW}$x), the address, and the first word of the data burst during a write operation. The $\overline{K}$ clock is used to clock in the control signals ($\overline{BW}$x), and the second word of the data burst during a write operation. The K and $\overline{K}$ clocks are also used internally by the SRAM. In the event that the user disables the C and $\overline{C}$ clocks, the K and $\overline{K}$ clocks will also be used to clock the data out of the output register and generate the echo clocks.

The C and $\overline{C}$ clocks may be used to clock the data out of the output register during read operations and to generate the echo clocks. C and $\overline{C}$ must be presented to the SRAM within the timing tolerances. The output data from the DDRII will be closely aligned to the C and $\overline{C}$ input, through the use of an internal DLL. When C is presented to the DDRII SRAM, the DLL will have already internally clocked the first data word to arrive at the device output simultaneously with the arrival of the $\overline{C}$ clock. The C and second data word of the burst will also correspond.

Single Clock Mode

The DDRII SRAM may be operated with a single clock pair. C and $\overline{C}$ may be disabled by tying both signals high, forcing the outputs and echo clocks to be controlled instead by the K and $\overline{K}$ clocks.

DLL Operation

The DLL in the output structure of the DDRII SRAM can be used to closely align the incoming clocks C and $\overline{C}$ with the output of the data, generating very tight tolerances between the two. The user may disable the DLL by holding $\overline{Doff}$ low. With the DLL off, the C and $\overline{C}$ (or K and $\overline{K}$ if C and $\overline{C}$ are not used) will directly clock the output register of the SRAM. With the DLL off, there will be a propagation delay from the time the clock enters the device until the data appears at the output.

Echo Clock

The echo clocks, CQ and $\overline{CQ}$, are generated by the C and $\overline{C}$ clocks (or K, $\overline{K}$ if C, $\overline{C}$ are disabled). The rising edge of C generates the rising edge of CQ, and the falling edge of $\overline{CQ}$. The rising edge of $\overline{C}$ generates the rising edge of $\overline{CQ}$ and the falling edge of CQ. This scheme improves the correlation of the rising and falling edges of the echo clock and will improve the duty cycle of the individual signals.

The echo clock is very closely aligned with the data, guaranteeing that the echo clock will remain closely correlated with the data, within the tolerances designated.

Read and Write Operations

Read operations are initiated by holding Read/Write control input (R/$\overline{W}$) high, the load control input ($\overline{LD}$) low and presenting the read address to the address port during the rising edge of K, which will latch the address. The data will then be read and will appear at the device output at the designated time in correspondence with the C and $\overline{C}$ clocks.

Write operations are initiated by holding the Read/Write control input (R/$\overline{W}$) low, the load control input ($\overline{LD}$) low and presenting the write address to the address port during the rising edge of K, which will latch the address. On the following rising edge of K, the first word of the two word burst must be present on the data input bus DQ[x:O], along with the appropriate byte write ($\overline{BW}$x) inputs. On the following rising edge of $\overline{K}$, the second half of the data write burst will be accepted at the device input with the designated ($\overline{BW}$x) inputs.

DDRII devices internally store two words of the burst as a single, wide word and will retain their order in the burst. The x18 and x36 DDRII devices have the ability to address to the individual word level using the SA0 address, but the burst will continue in a linear sequence and wraps around without incrementing the SA bits. Similarly when reading x18 and x36 DDRII devices, the read burst will begin at the designated address, but if the burst is started at any other position than the first word of the burst, the burst will wrap back on itself and read the first locations before completing. The x18 and x36 DDR II devices can also use the byte write signals to prevent writing any individual bytes or word of the burst.

Output Enables

The DDRII SRAM automatically enables and disables the DQ[X:0] outputs. When a valid read is in progress, and data is present at the output, the output will be enabled. If no valid data is present at the output (read not active), the output will be disabled (high impedance). The echo clocks will remain valid at all times and cannot be disabled or turned off. During power-up the DQ outputs will come up in a high impedance state.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the SRAM and Vss to allow the SRAM to adjust its output drive impedance. The value of RQ must be 5X the value of the intended drive impedance of the SRAM. The allowable range of RQ to guarantee impedance matching with a tolerance of +/- 10% is between 175 ohms and 350 ohms, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 clock cycles to correct for drifts in supply voltage and temperature. If the user wishes to drive the output impedance of the SRAM to it's lowest value, the ZQ pin may be tied to V_{DDQ}.

Pin Definitions

Symbol	Pin Function	Description
DQ[X:0]	Input/Output Synchronous	Data I/O signals. Data inputs are sampled on the rising edge of K and $\overline{K}$ during valid write operations. Data outputs are driven during a valid read operation. The outputs are aligned with the rising edge of both C and $\overline{C}$ during normal operation. When operating in a single clock mode (C and $\overline{C}$ tied high), the outputs are aligned with the rising edge of both K and $\overline{K}$. When a Read operation is not initiated or $\overline{LD}$ is high (deselected) during the rising edge of K, DQ[X:O] are automatically driven to high impedance after any previous read operation in progress completes. 1M x 18 -- DQ[17:0] 512K x 36 -- DQ[35:0]
$\overline{BW}_0$, $\overline{BW}_1$, $\overline{BW}_2$, $\overline{BW}_3$	Input Synchronous	Byte Write Select 0, 1, 2, and 3 are active LOW. Sampled on the rising edge of the K and again on the rising edge of $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. All the byte writes are sampled on the same edge as the data. Deselecting a Byte Write Select will cause the corresponding byte of data to be ignored and not written in to the device. 1M x 18 -- $\overline{BW}_0$ controls DQ[8:0] and $\overline{BW}_1$ controls DQ[17:9] 512K x 36 -- $\overline{BW}_0$ controls DQ[8:0], $\overline{BW}_1$ controls DQ[17:9], $\overline{BW}_2$ controls DQ[26:18] and $\overline{BW}_3$ controls DQ[35:27]
SA	Input Synchronous	Address Inputs. Addresses are sampled on the rising edge of K clock during active read or write operations.
SA_0	Input Synchronous	Burst count address bit on x18 and x36 DDRII devices. This bit allows changing the burst order in read or write operations, or addressing to the individual word of a burst. See page 9 for all possible burst sequences.
$\overline{LD}$	Input Synchronous	Load Control Logic: Sampled on the rising edge of K. If $\overline{LD}$ is low, a two word burst read or write operation will initiate as designated by the R/$\overline{W}$ input. If $\overline{LD}$ is high during the rising edge of K, operations in progress will complete, but new operations will not be initiated.
R/$\overline{W}$	Input Synchronous	Read or Write Control Logic. If $\overline{LD}$ is low during the rising edge of K, the R/$\overline{W}$ indicates whether a new operation should be a read or write. If R/$\overline{W}$ is high, a read operation will be initiated, if R/$\overline{W}$ is low, a write operation will be initiated. If the $\overline{LD}$ input is high during the rising edge of K, the R/$\overline{W}$ input will be ignored.
C	Input Clock	Positive Output Clock Input. C is used in conjunction with $\overline{C}$ to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
$\overline{C}$	Input Clock	Negative Output Clock Input. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
K	Input Clock	Positive Input Clock. The rising edge of K is used to capture synchronous inputs to the device and to drive out data through DQ[X:0] when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}$	Input Clock	Negative Input Clock. $\overline{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through DQ[X:0] when in single clock mode.
CQ, $\overline{CQ}$	Output Clock	Synchronous Echo clock outputs. The rising edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals are free running and do not stop when the output data is three stated.
ZQ	Input	Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. DQ[X:0] output impedance is set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

6112 tbl 02a

Pin Definitions continued

Symbol	Pin Function	Description
$\overline{Doff}$	Input	DLL Turn Off. When low this input will turn off the DLL inside the device. The AC timings with the DLL turned off will be different from those listed in this data sheet. There will be an increased propagation delay from the incidence of C and $\overline{C}$ to DQ, or K and $\overline{K}$ to DQ as configured. The propagation delay is not a tested parameter, but will be similar to the propagation delay of other SRAM devices in this speed grade.
TDO	Output	TDO pin for JTAG
TCK	Input	TCK pin for JTAG.
TDI	Input	TDI pin for JTAG. An internal resistor will pull TDI to V_{DD} when the pin is unconnected.
TMS	Input	TMS pin for JTAG. An internal resistor will pull TMS to V_{DD} when the pin is unconnected.
NC	No Connect	No connects inside the package. Can be tied to any voltage level.
V_{REF}	Input Reference	Reference Voltage input. Static input used to set the reference level for HSTL inputs and outputs as well as AC measurement points.
V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to a 1.8V power supply.
V_{SS}	Ground	Ground for the device. Should be connected to ground of the system.
V_{DDQ}	Power Supply	Power supply for the outputs of the device. Should be connected to a 1.5V power supply for HSTL or scaled to the desired output voltage.

6112 tbl 02b

Pin Configuration IDT71P71804 (1M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	Vss/ SA (2)	SA	R/$\overline{W}$	$\overline{BW_1}$	$\overline{K}$	NC	$\overline{LD}$	SA	Vss/ SA (1)	CQ
B	NC	DQ_9	NC	SA	NC	K	$\overline{BW_0}$	SA	NC	NC	DQ_8
C	NC	NC	NC	V_{SS}	SA	SA_0	SA	V_{SS}	NC	DQ_7	NC
D	NC	NC	DQ_{10}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ_{11}	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ_6
F	NC	DQ_{12}	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ_5
G	NC	NC	DQ_{13}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_4	NC
K	NC	NC	DQ_{14}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ_3
L	NC	DQ_{15}	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ_2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ_1	NC
N	NC	NC	DQ_{16}	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ_{17}	SA	SA	C	SA	SA	NC	NC	DQ_0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

6112 tbl 12b

165-ball FBGA Pinout
TOP VIEW

NOTES:
1. A10 is reserved for the 36Mb expansion address. This must be tied or driven to Vss on the 1M x 18 DDRII Burst of 2 (71P71804) devices.
2. A2 is reserved for the 72Mb expansion address. This must be tied or driven to VSS on the 1M x 18 DDRII Burst of 2 (71P71804) devices.

Pin Configuration IDT71P71604 (512K x 36)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}/ SA (3)	NC/ SA (1)	R/$\overline{W}$	$\overline{BW_2}$	$\overline{K}$	$\overline{BW_1}$	$\overline{LD}$	SA	V_{SS}/ SA (2)	CQ
B	NC	DQ_{27}	DQ_{18}	SA	$\overline{BW_3}$	K	$\overline{BW_0}$	SA	NC	NC	DQ_8
C	NC	NC	DQ_{28}	V_{SS}	SA	SA_0	SA	V_{SS}	NC	DQ_{17}	DQ_7
D	NC	DQ_{29}	DQ_{19}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ_{16}
E	NC	NC	DQ_{20}	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ_{15}	DQ_6
F	NC	DQ_{30}	DQ_{21}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	VDDQ	NC	NC	DQ_5
G	NC	DQ_{31}	DQ_{22}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ_{14}
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ_{32}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_{13}	DQ_4
K	NC	NC	DQ_{23}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ_{12}	DQ_3
L	NC	DQ_{33}	DQ_{24}	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ_2
M	NC	NC	DQ_{34}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ_{11}	DQ_1
N	NC	DQ_{35}	DQ_{25}	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ_{10}
P	NC	NC	DQ_{26}	SA	SA	C	SA	SA	NC	DQ_9	DQ_0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

6112 tbl 12c

165-ball FBGA Pinout
TOP VIEW

NOTES:
1. A3 is reserved for the 36Mb expansion address.
2. A10 is reserved for the 72Mb expansion address.
3. A2 is reserved for the 144Mb expansion address

Write Descriptions(1,2,3)

Signal	$\overline{BW}_0$	$\overline{BW}_1$	$\overline{BW}_2$	$\overline{BW}_3$
Write Byte 0	L	X	X	X
Write Byte 1	X	L	X	X
Write Byte 2	X	X	L	X
Write Byte 3	X	X	X	L

6112 tbl 09

NOTES:

1) All byte write ($\overline{BW}$x) signals are sampled on the rising edge of K and again on $\overline{K}$. The data that is present on the data bus in the designated byte will be latched into the input if the corresponding $\overline{BW}$x is held low. The rising edge of K will sample the first byte of the two word burst and the rising edge of $\overline{K}$ will sample the second byte of the two word burst.
2) The availability of the $\overline{BW}$x on designated devices is described in the pin description table.
3) The DDRII Burst of two SRAM has data forwarding. A read request that is initiated on the cycle following a write request to the same address will produce the newly written data.

Linear Burst Sequence Table (1)

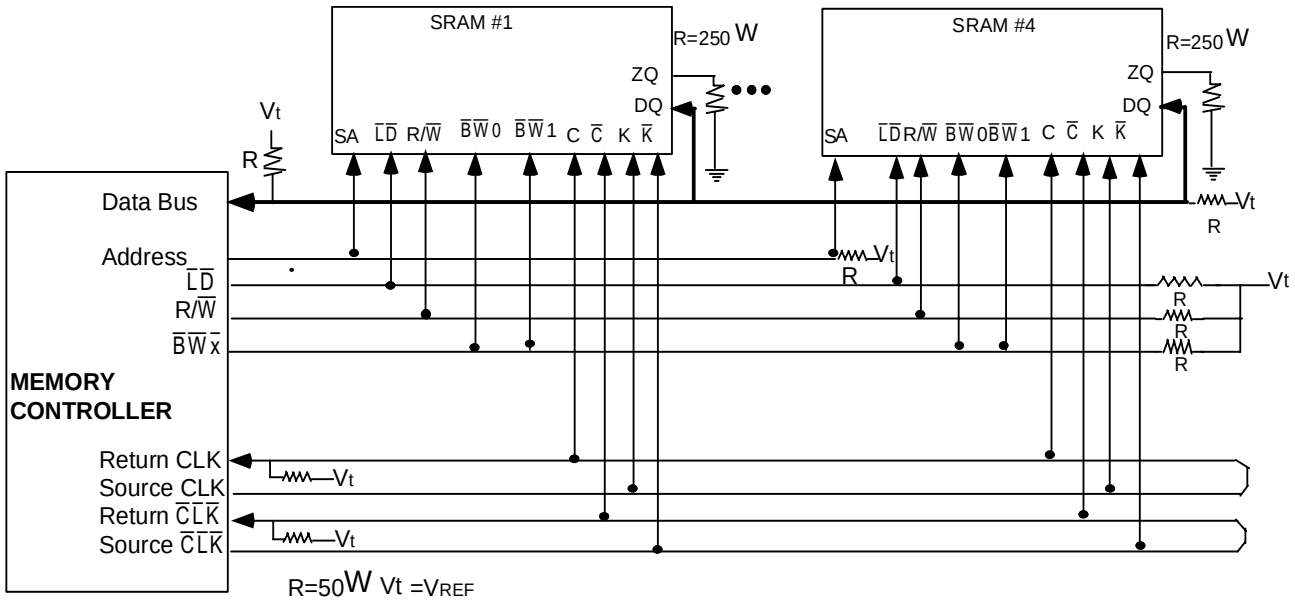
SA_0	a	b
0	0	1
1	1	0

6112 tbl 22

NOTE:

1. SA_0 is the address presented giving the burst sequence a,b.

Application Example



Absolute Maximum Ratings(1) (2)

Symbol	Rating	Value	Unit
V_{TERM}	Supply Voltage on V_{DD} with Respect to GND	–0.5 to +2.9	V
V_{TERM}	Supply Voltage on V_{DDQ} with Respect to GND	–0.5 to V_{DD}+0.3	V
V_{TERM}	Voltage on Input terminals with respect to GND	–0.5 to V_{DD} +0.3	V
V_{TERM}	Voltage on Output and I/O terminals with respect to GND.	–0.5 to V_{DDQ} +0.3	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Continuous Current into Outputs	± 20	mA

6112 tbl 05

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DDQ} must not exceed V_{DD} during normal operation.

Recommended DC Operating and Temperature Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	1.7	1.8	1.9	V
V_{DDQ}	I/O Supply Voltage	1.4	1.5	V_{DD}	V
V_{SS}	Ground	0	0	0	V
V_{REF}	Input Reference Voltage	0.68	V_{DDQ}/2	0.95	V
T_A	Ambient Temperature (1)	0	25	70	°C

6112 tbl 04

NOTE:
1. During production testing, the case temperature equals the ambient temperature.

Capacitance (T_A = +25°C, f = 1.0MHz)(1)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{DD} = 1.8V, V_{DDQ} = 1.5V	5	pF
C_{CLK}	Clock Input Capacitance		6	pF
C_O	Output Capacitance		7	pF
C_{DQ}	DQ I/O Capacitance		7	pF

6112 tbl 06

NOTE:
1. Tested at characterization and retested after any design or process change that may affect these parameters.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8 ± 100mV, V_{DDQ} = 1.4V to 1.9V)

Parameter	Symbol	Test Conditions		Min	Max	Unit	Note
Input Leakage Current	I_{IL}	V_{DD} = Max V_{IN} = V_{SS} to V_{DDQ}		-2	+2	µA	
Output Leakage Current	I_{OL}	Output Disabled		-2	+2	µA	
Operating Current (x36): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0mA (outputs open), Cycle Time ≥ t_{KHKH} Min	250MHz	-	900	mA	1
			200MHz	-	800		
			167MHz	-	700		
Operating Current (x18): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0mA (outputs open), Cycle Time ≥ t_{KHKH} Min	250MHz	-	850	mA	1
			200MHz	-	750		
			167MHz	-	650		
Standby Current: NOP	I_{SB1}	Device Deselected (in NOP state), I_{OUT} = 0mA (outputs open), f=Max, All Inputs ≤0.2V or ≥ VDD -0.2V	250MHz	-	325	mA	2
			200MHz	-	300		
			167MHz	-	275		
Output High Voltage	V_{OH1}	RQ = 250Ω, I_{OH} = -15mA		V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V	3,7
Output Low Voltage	V_{OL1}	RQ = 250Ω, I_{OH} = 15mA		V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V	4,7
Output High Voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DDQ}-0.2	V_{DDQ}	V	5
Output Low Voltage	V_{OL2}	I_{OL} = 0.1mA		V_{SS}	0.2	V	6

6112 tbl 10c

NOTES:

1. Operating Current is measured at 100% bus utilization.
2. Standby Current is only after all pending read and write burst operations are completed.
3. Outputs are impedance-controlled. I_{OH} = -(V_{DDQ}/2)/(RQ/5) and is guaranteed by device characterization for 175Ω ≤ RQ < 350Ω. This parameter is tested at RQ = 250Ω, which gives a nominal 50Ω output impedance.
4. Outputs are impedance-controlled. I_{OL} = (V_{DDQ}/2)/(RQ/5) and is guaranteed by device characterization for 175Ω ≤ RQ < 350Ω. This parameter is tested at RQ = 250Ω, which gives a nominal 50Ω output impedance.
5. This measurement is taken to ensure that the output has the capability of pulling to the V_{DDQ} rail, and is not intended to be used as an impedance measurement point.
6. This measurement is taken to ensure that the output has the capability of pulling to V_{SS}, and is not intended to be used as an impedance measurement point.
7. Programmable Impedance Mode.

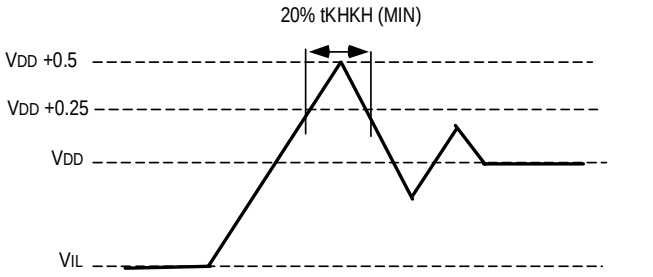
Input Electrical Characteristics Over the Operating Temperature and Supply Voltage Range (V_{DD} = 1.8 ± 100mV, V_{DDQ} = 1.4V to 1.9V)

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTES
Input High Voltage, DC	V_{IH} (DC)	V_{REF} +0.1	V_{DDQ} +0.3	V	1,2
Input Low Voltage, DC	V_{IL} (DC)	-0.3	V_{REF} -0.1	V	1,3
Input High Voltage, AC	V_{IH} (AC)	V_{REF} +0.2	-	V	4,5
Input Low Voltage, AC	V_{IL} (AC)	-	V_{REF} -0.2	V	4,5

6112 tbl 10d

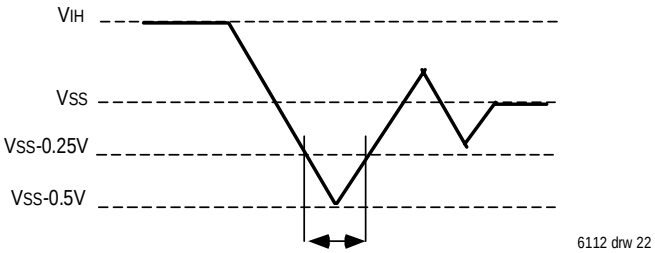
NOTES:
1. These are DC test criteria. DC design criteria is V_{REF} ± 50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IL} (Min) DC = -0.3V, V_{IL} (Min) AC = -0.5V (pulse width ≤20% tKHKH (min))
3. V_{IH} (Max) DC = V_{DDQ}+0.3, V_{IH} (Max) AC = V_{DD} +0.5V (pulse width ≤20% tKHKH (min))
4. This conditon is for AC function test only, not for AC parameter test.
5. To maintain a valid level, the transitioning edge of the input must:
   a) Sustain a constant slew rate from the current AC level through the target AC level, V_{IL}(AC) or V_{IH}(AC)
   b) Reach at leaset the target AC level.
   c) After the AC target level is reached, continue to maintain at least the target DC level, V_{IL}(DC) or V_{IH}(DC)

Overshoot Timing



6112 drw 21

Undershoot Timing



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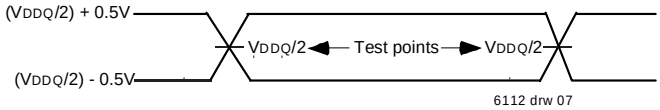
AC Test Conditions(1)

Parameter	Symbol	Value	Unit	Note
Core Power Supply Voltage	V_{DD}	1.7 to 1.9	V	2
I/O Power Supply Voltage	V_{DDQ}	1.4 to V_{DD}	V	2
Input High Level	V_{IH}	(V_{DDQ}/2)+ 0.5	V	
Input Low Level	V_{IL}	(V_{DDQ}/2)- 0.5	V	
Input Reference Level	VREF	V_{DDQ}/2	V	
Input Rise/Fall Time	TR/TF	0.3/0.3	ns	
DQ Rise/Fall Time		0.5/0.5		
Output Timing Reference Level		V_{DDQ}/2	V	

6112 tbl 11a

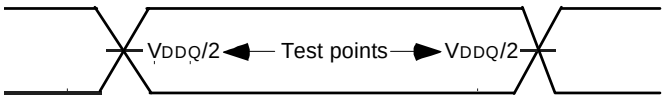
NOTE:
1. Parameters are tested with RQ=250Ω
2. VDDQ does not exceed VDD. During AC testing VDDQ is within 300mV of VDD.

Input Waveform



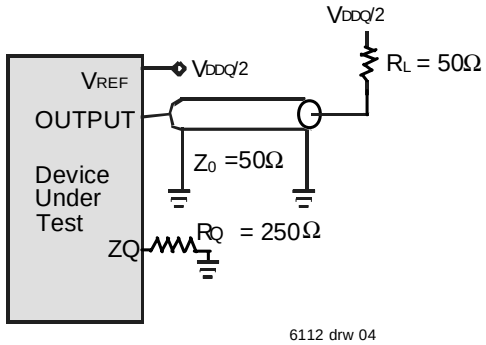
6112 drw 07

Output Waveform



6112 drw 08

AC Test Load



6112 drw 04

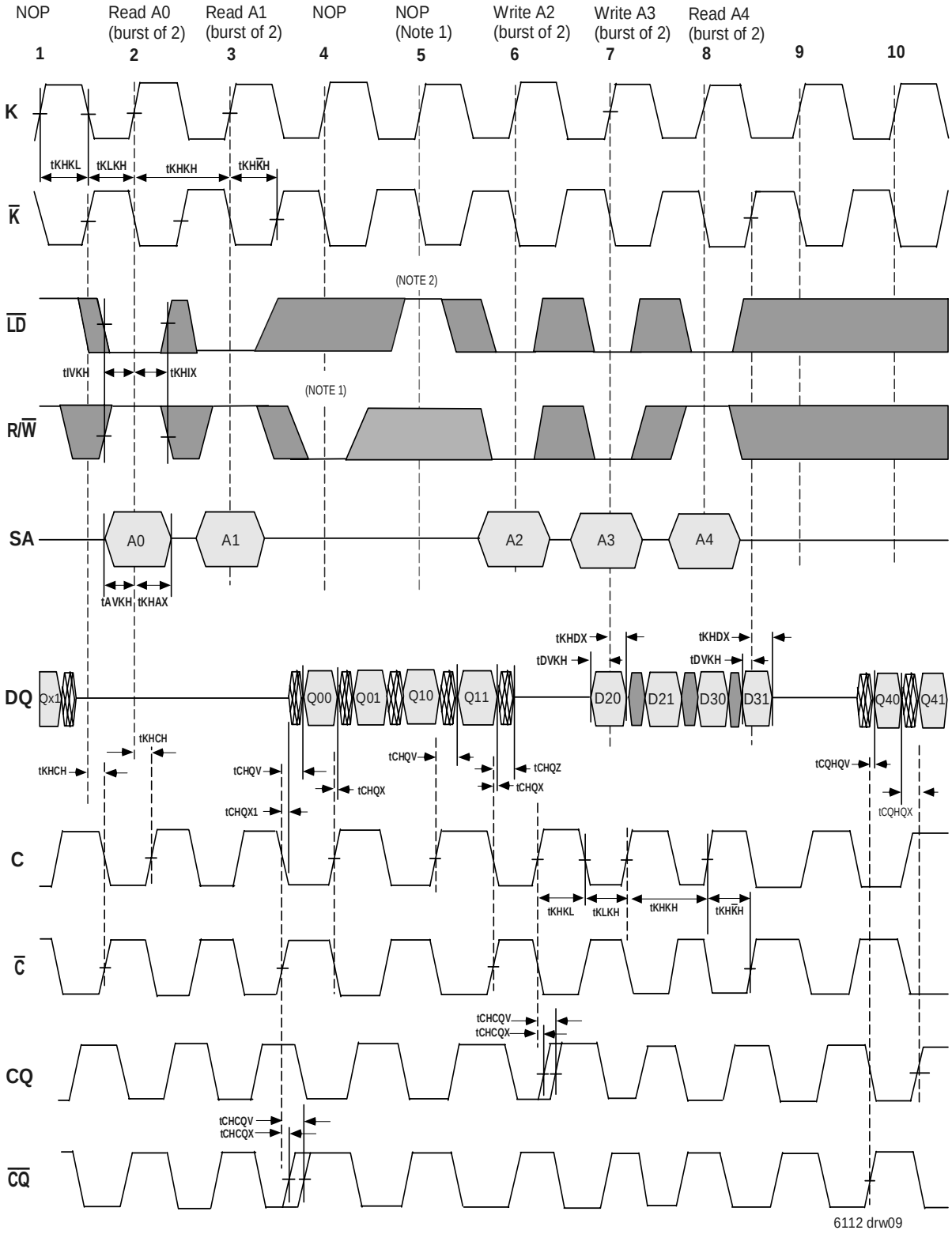
AC Electrical Characteristics (V_{DD} = 1.8 ± 100mV, V_{DDQ} = 1.4V to 1.9V, T_A =0 to 70°C) (3,7)

Symbol	Parameter	250MHz		200MHz		167MHz		Unit	Notes
		Min.	Max	Min.	Max	Min.	Max		
Clock Parameters									
tKHKH	Clock Cycle Time (K,$\overline{K}$,C,$\overline{C}$)	4.00	6.30	5.00	7.88	6.00	8.40	ns	
tKC var	Clock Phase Jitter (K,$\overline{K}$,C,$\overline{C}$)	-	0.20	-	0.20	-	0.20	ns	1,5
tKHKL	Clock High Time (K,$\overline{K}$,C,$\overline{C}$)	1.60	-	2.00	-	2.40	-	ns	8
tKLKH	Clock LOW Time (K,$\overline{K}$,C,$\overline{C}$)	1.60	-	2.00	-	2.40	-	ns	8
tKH$\overline{K}$H	Clock to $\overline{clock}$ (K→$\overline{K}$,C→$\overline{C}$)	1.80	-	2.20	-	2.70	-	ns	9
t$\overline{K}$HKH	$\overline{Clock}$ to clock ($\overline{K}$→K,$\overline{C}$→C)	1.80	-	2.20	-	2.70	-	ns	9
tKHCH	Clock to data clock (K→C,$\overline{K}$→$\overline{C}$)	0.00	1.80	0.00	2.30	0.00	2.80	ns	
tKC lock	DLL lock time (K, C)	1024	-	1024	-	1024	-	cycles	2
tKC reset	K static to DLL reset	30	-	30	-	30	-	ns	
Output Parameters									
tCHQV	C,$\overline{C}$ HIGH to output valid	-	0.50	-	0.50	-	0.50	ns	3
tCHQX	C,$\overline{C}$ HIGH to output hold	-0.45	-	-0.45	-	-0.50	-	ns	3
tCHCQV	C,$\overline{C}$ HIGH to echo clock valid	-	0.50	-	0.50	-	0.50	ns	3
tCHCQX	C,$\overline{C}$ HIGH to echo clock hold	-0.45	-	-0.45	-	-0.50	-	ns	3
tCQHQV	CQ,$\overline{CQ}$ HIGH to output valid	-	0.30	-	0.35	-	0.40	ns	
tCQHQX	CQ,$\overline{CQ}$ HIGH to output hold	-0.30	-	-0.35	-	-0.40	-	ns	
tCHQZ	C HIGH to output High-Z	-	0.45	-	0.45	-	0.50	ns	3,4,5
tCHQX1	C HIGH to output Low-Z	-0.45	-	-0.45	-	-0.50	-	ns	3,4,5
Set-Up Times									
tAVKH	Address valid to K,$\overline{K}$ rising edge	0.50	-	0.60	-	0.70	-	ns	6
tIVKH	$\overline{R}$, $\overline{W}$ inputs valid to K,$\overline{K}$ rising edge	0.50	-	0.60	-	0.70	-	ns	
tDVKH	Data-in and $\overline{BW}$x valid to K, $\overline{K}$ rising edge	0.40	-	0.40	-	0.50	-	ns	
Hold Times									
tKHAX	K,$\overline{K}$ rising edge to address hold	0.50	-	0.60	-	0.70	-	ns	6
tKHIX	K,$\overline{K}$ rising edge to $\overline{R}$, $\overline{W}$ inputs hold	0.50	-	0.60	-	0.70	-	ns	
tKHDX	K, $\overline{K}$ rising edge to data-in and $\overline{BW}$x hold	0.35	-	0.40	-	0.50	-	ns	

6112 tbl 11

NOTES:
1. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
2. V_{dd} slew rate must be less than 0.1V DC per 50 ns for DLL lock retention. DLL lock time begins once Vdd and input clock are stable.
3. If C,$\overline{C}$ are tied High, K,$\overline{K}$ become the references for C,$\overline{C}$ timing parameters.
4. To avoid bus contention, at a given voltage and temperature $tCHQX_1$ is bigger than tCHQZ.
   The specs as shown do not imply bus contention because tCHQX1 is a MIN parameter that is worse case at totally different test conditions (0°C, 1.9V) than tCHQZ, which is a MAX parameter (worst case at 70°C, 1.7V)
   It is not possible for two SRAMs on the same board to be at such different voltage and temperature.
5. This parameter is guaranteed by device characterization, but not production tested.
6. All address inputs must meet the specified setup and hold times for all latching clock edges.
7. During production testing, the case temperature equals T_A.
8. Clock High Time (tKHKL) and Clock Low Time (tKLKH) should be within 40% to 60% of the cycle time (tKHKH).
9. Clock to $\overline{clock}$ time (tKH$\overline{K}$H) and $\overline{Clock}$ to clock time (t$\overline{K}$HKH) should be within 45% to 55% of the cycle time (tKHKH).

Timing Waveform of Combined Read and Write Cycles



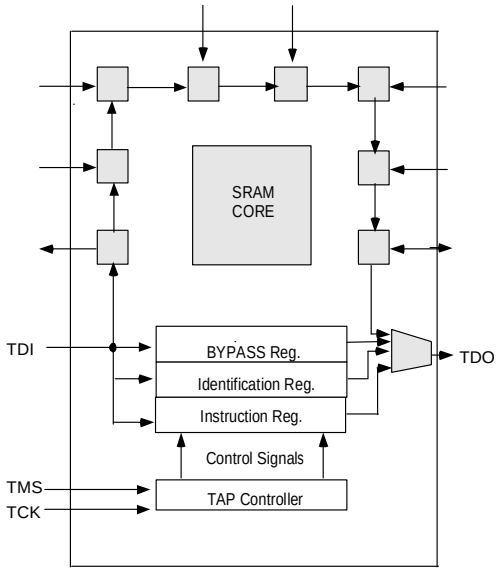
NOTE:

1. If a R/$\overline{W}$ is low on the next rising edge of K after a read request, the device automatically performs a NOP (No Operation.)
2. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies, it may be required to prevent the bus contention.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up; therefore, the TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to VSS to preclude a mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected, but they may also be tied to VDD through a resistor. TDO should be left unconnected.

JTAG Block Diagram



6112 drw 18

JTAG Instruction Coding

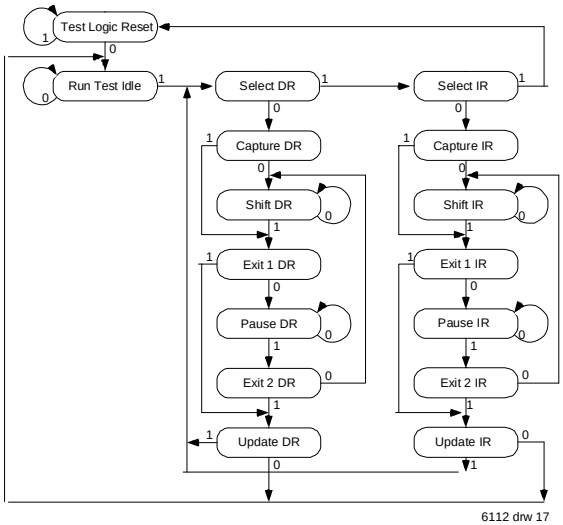
IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	
0	0	1	IDCODE	Identification register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	RESERVED	Do Not Use	5
1	0	0	SAMPLE/PRELOAD	Boundary Scan register	4
1	0	1	RESERVED	Do Not Use	5
1	1	0	RESERVED	Do Not Use	5
1	1	1	BYPASS	Bypass Register	3

6112 tbl 13

NOTE:

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initialized to Vss when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not place output pins in Hi-Z.
5. This instruction is reserved for future use.

TAP Controller State Diagram



6112 drw 17

Scan Register Definition

Part	Instrustion Register	Bypass Register	ID Register	Boundary Scan
512K x36	3 bits	1 bit	32 bits	107 bits
1Mx18	3 bits	1 bit	32 bits	107 bits

6112 tbl 14

Identification Register Definitions

INSTRUCTION FIELD	ALL DEVICES	DESCRIPTION	PART NUMBER
Revision Number (31:29)	0x0	Revision Number	
Device ID (28:12)	0x0294 0x0295	512Kx36 DDRII BURST OF 2 1Mx18	71P71604S 71P71804S
IDT JEDEC ID CODE (11:1)	0x033	Allows unique identification of SRAM vendor.	
ID Register Presence Indicator (0)	1	Indicates the presence of an ID register.	

6112 tbl 15

Boundary Scan Exit Order (1M x 18-Bit)

ORDER	PIN ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	10P
12	10N
13	9P
14	10M
15	11N
16	9M
17	9N
18	11L
19	11M
20	9L
21	10L
22	11K
23	10K
24	9J
25	9K
26	10J
27	11J
28	11H
29	10G
30	9G
31	11F
32	11G
33	9F
34	10F
35	11E
36	10E

6112 tbl 16

ORDER	PIN ID
37	10D
38	9E
39	10C
40	11D
41	9C
42	9D
43	11B
44	11C
45	9B
46	10B
47	11A
48	Internal
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	1H
65	1A
66	2B
67	3B
68	1C
69	1B
70	3D
71	3C
72	1D

6112 tbl 17

ORDER	PIN ID
73	2C
74	3E
75	2D
76	2E
77	1E
78	2F
79	3F
80	1G
81	1F
82	3G
83	2G
84	1J
85	2J
86	3K
87	3J
88	2K
89	1K
90	2L
91	3L
92	1M
93	1L
94	3N
95	3M
96	1N
97	2M
98	3P
99	2N
100	2P
101	1P
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R

6112 tbl 18

Boundary Scan Exit Order (512K x 36-Bit)

ORDER	PIN ID
1	6R
2	6P
3	6N
4	7P
5	7N
6	7R
7	8R
8	8P
9	9R
10	11P
11	9P
12	10N
13	10P
14	11M
15	9N
16	9M
17	11N
18	11L
19	10L
20	9L
21	10M
22	11K
23	9K
24	9J
25	10K
26	11J
27	9G
28	11H
29	10G
30	10J
31	11F
32	10F
33	9F
34	11G
35	11E
36	9E

6112 tbl 16b

ORDER	PIN ID
37	10D
38	10E
39	11C
40	9D
41	9C
42	11D
43	11B
44	10B
45	9B
46	10C
47	11A
48	Internal
49	9A
50	8B
51	7C
52	6C
53	8A
54	7A
55	7B
56	6B
57	6A
58	5B
59	5A
60	4A
61	5C
62	4B
63	3A
64	1H
65	1A
66	3B
67	1B
68	1C
69	2B
70	3D
71	2C
72	1D

6112 tbl 17b

ORDER	PIN ID
73	3C
74	3E
75	1E
76	2E
77	2D
78	3F
79	1F
80	1G
81	2F
82	3G
83	2J
84	1J
85	2G
86	3K
87	1K
88	2K
89	3J
90	3L
91	1L
92	1M
93	2L
94	3N
95	2M
96	1N
97	3M
98	3P
99	1P
100	2P
101	2N
102	3R
103	4R
104	4P
105	5P
106	5N
107	5R

6112 tbl 18b

JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
I/O Power Supply	V_{DDQ}	1.4	-	V_{DD}	V	
Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Input High Level	V_{IH}	1.3	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.5	V	
TCK Input Leakage Current	I_{IL}	-5	-	+5	µA	
TMS, TDI Input Leakage Current	I_{IL}	-15	-	+15	µA	
TDO Output Leakage Current	I_{OL}	-5	-	+5	µA	
Output High Voltage (I_{OH} = -1mA)	V_{OH}	V_{DDQ} - 0.2	-	V_{DDQ}	V	1
Output Low Voltage (I_{OL} = 1mA)	V_{OL}	V_{SS}	-	0.2	V	1

6112 tbl 19

NOTE:
1. The output impedance of TDO is set to 50 ohms (nominal process) and does not vary with the external resistor connected to ZQ.

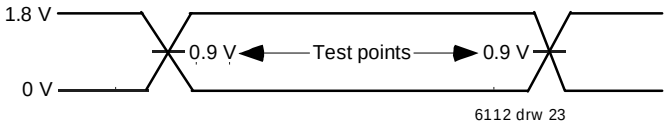
JTAG AC Test Conditions

Parameter	Symbol	Min	Unit	Note
Input High Level	V_{IH}	1.8	V	
Input Low Level	V_{IL}	0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	1

6112 tbl 20

NOTE:
1. For SRAM outputs see AC test load on page 12.

JTAG Input Test Waveform



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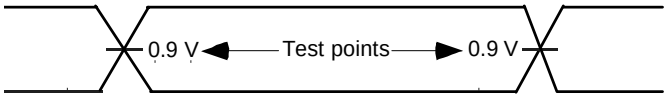
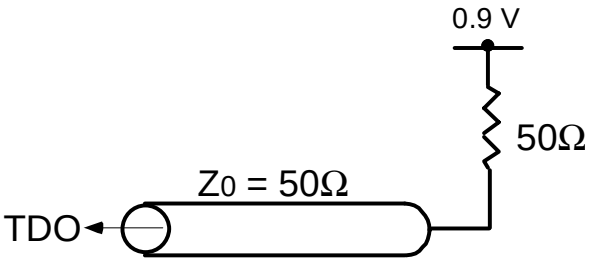
JTAG Output Test Waveform



6112 drw 24

JTAG AC Test Load



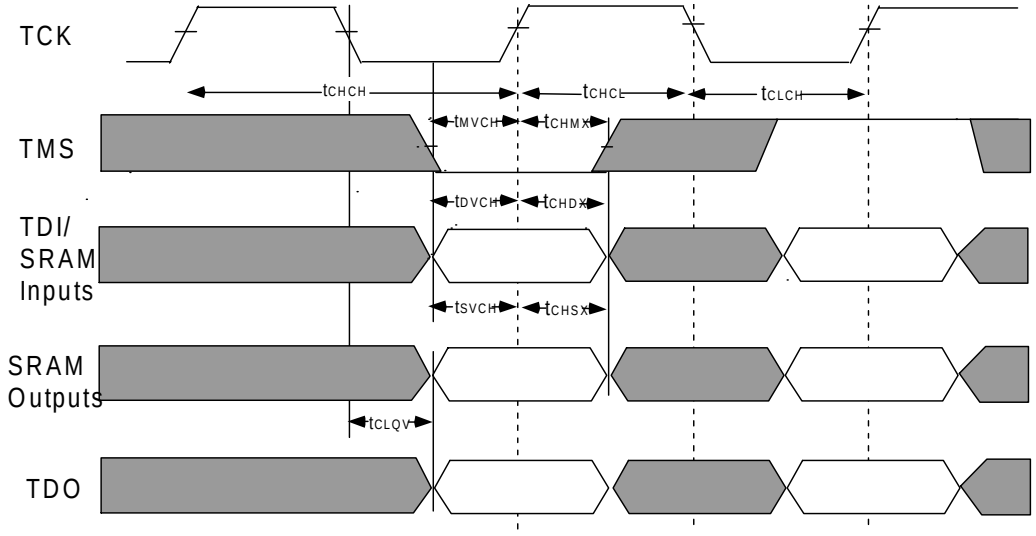
6112 drw 25

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
SRAM Input Setup Time	t_{SVCH}	5	-	ns	
SRAM Input Hold Time	t_{CHSX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

6112 tbl.21

JTAG Timing Diagram



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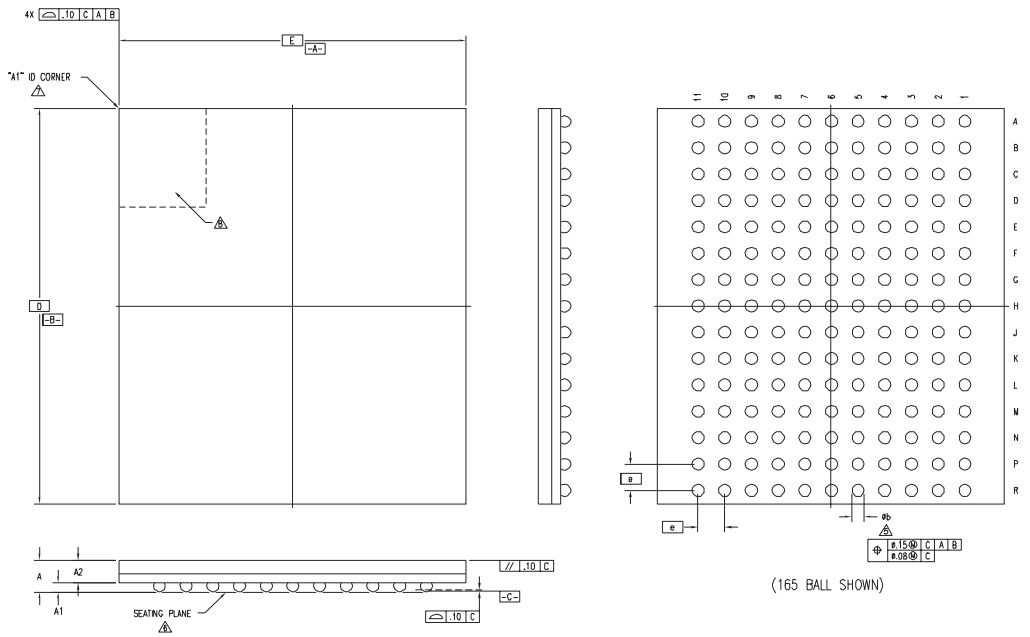
Package Diagram Outline for 165-Ball Fine Pitch Grid Array

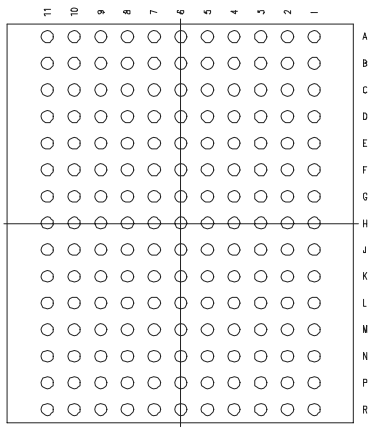
REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	



(165 BALL SHOWN)

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070		
DECIMAL ANGULAR				
APPROVALS	DATE	TITLE	BQ PACKAGE OUTLINE 13.0 X 15.0 mm BODY FPBGA	
DRAWN JTF	05/01/00			
CHECKED		SIZE C	DRAWING No. PSC-4086	REV 00
		DO NOT SCALE DRAWING		SHEET 1 OF 2

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	05/01/00	



(165 BALL)

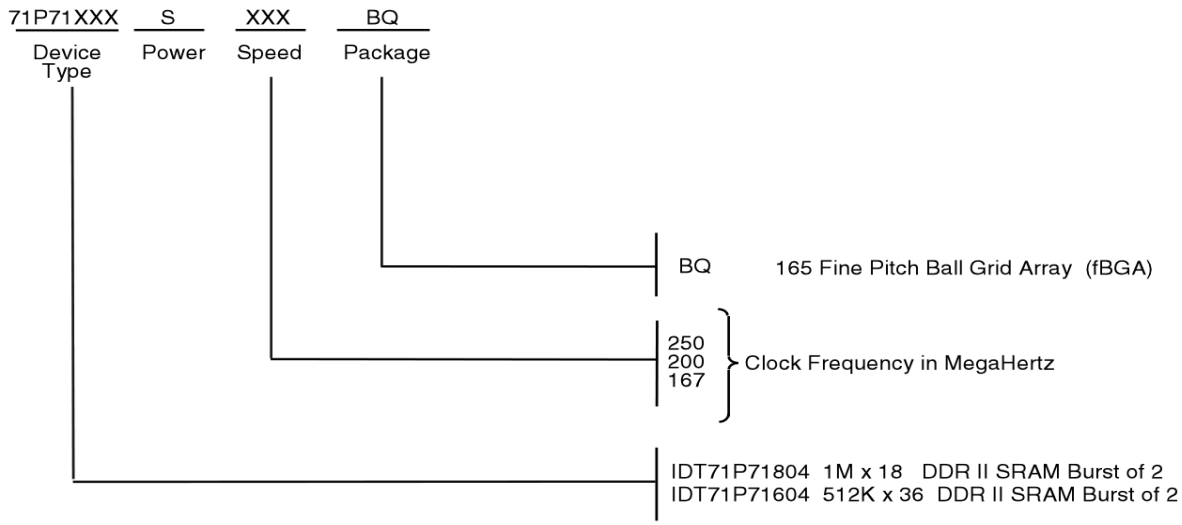
SYMBOL	JEDEC VARIATION NOT YET REGISTERED MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	.30	.35	.40	
A2	.78	.85	.92	
D	15.00 BSC			
E	13.00 BSC			
M	11 X 15			3
N	165			4
e	1.00 BSC			
b	.35	.45	.50	5
CENTER BALL MATRIX	N/A			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M-1994
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH
3. "M" REPRESENTS THE MAXIMUM SOLDER BALL MATRIX SIZE
4. "N" REPRESENTS THE BALLCOUNT NUMBER
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM -C-
6. SEATING PLANE AND PRIMARY DATUM -C- ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
7. "A1" ID CORNER MUST BE IDENTIFIED BY CHAMFER, INK MARK, METALLIZED MARKING, INDENTATION OR OTHER FEATURE ON PACKAGE BODY
8. IF "A1" ID CORNER IS ON PACKAGE BODY, IT MUST BE LOCATED WITHIN THE ZONE INDICATED
9. ALL DIMENSIONS ARE IN MILLIMETERS

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way Santa Clara CA 95054 PHONE (408) 727-6116 FAX: (408) 492-8674 TWX. 910-338-2070		
DECIMAL ANGULAR				
APPROVALS	DATE	TITLE	BQ PACKAGE OUTLINE 13.0 X 15.0 mm BODY FPBGA	
DRAWN JTF	05/01/00			
CHECKED		SIZE C	DRAWING No. PSC-4086	REV 00
		DO NOT SCALE DRAWING		SHEET 2 OF 2

Ordering Information



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Revision History

REVISION	DATE	PAGES	DESCRIPTION
0	07/29/05	1-24	Released Final datasheet
A	04/21/06	1-3,7,8,10,13, 16,17,22	Removed 2Mx8 (71P71204) and 2Mx9 (71P71104) device options.
		9,12,19	Clarified VDDQ maximum value equals VDD.
		10	Updated IDD operating current for x36 and x18 options.
		12	Added clarification for VDDQ and VDD values for AC test condition.
B	10/13/08	22	Removed “IDT” from orderable part number
C	04/01/09	13	Revised t_{CHQV}, t_{CHCQV}, and t_{DVKH} speeds