# Converting from CY14E256L/STK14C88 to CY14E256LA

## AN55663

**Author**: Ravi Prakash
**Associated Part Family**: CY14E256L/STK14C88
CY14E256LA
**Associated Application Notes**: None

## Application Note Abstract

This application note provides information for converting from CY14E256L/STK14C88 parts to the CY14E256LA. It lists the parameter differences between the parts and the design considerations when converting existing applications from CY14E256L/STK14C88 to CY14E256LA.

## Introduction

Cypress CY14E256LA is a 5V, 32Kb x 8, 256 Kbit nvSRAM in 0.13u technology. This part is functionally equivalent to CY14E256L/STK14C88 (0.8u) and is intended as a drop in replacement. (STK14C88 is the Simtek part number for CY14E256L.) This application note highlights the differences between the CY14E256L/STK14C88 and the CY14E256LA and the parameters of significance that must be considered while migrating.

## Overview

The following tables compare the features and parameters of the two parts. As shown in Table 1, the 256 Kbit nvSRAM is available in x8 configuration.

Table 1. Part Number Description

| Description | Original Part Number | Replacement Part Number |
|---|---|---|
| 32Kb x 8 | CY14E256L/STK14C88 | CY14E256LA |

## Feature Set

Both parts share the same overall feature set and are available in the operation speed bins as follows.

Table 2. Feature Set Comparison

| Feature Set | CY14E256L/STK14C88 | CY14E256LA |
|---|---|---|
| AutoStore | Available | Available |
| Software STORE | Available | Available |
| Hardware STORE | Available | Available |
| Software RECALL | Available | Available |
| AutoStore Inhibit | Available | Not Available |
| AutoStore Enable/Disable | Not Available | Available |

| Feature Set | CY14E256L/STK14C88 | CY14E256LA |
|---|---|---|
| Speed | 25 ns<br>35 ns<br>45 ns | 25 ns<br>-<br>45 ns |
| STORE Cycles | 1,000,000 | 200,000 |
| Data Retention | 100 years at 55°C | 20 years at 85°C |

## Operating Temperature Range

While CY14E256L/STK14C88 is available in both Commercial and Industrial temperature ranges, CY14E256LA is offered only in the Industrial temperature range.

Table 3. Operating Temperature Range Comparison

| Operating Temperature Range | CY14E256L/STK14C88 | CY14E256LA |
|---|---|---|
| Commercial (0 to 70°C) | Available | Not Available |
| Industrial (-40 to 85°C) | Available | Available |

## Packages

CY14E256LA is pin compatible with CY14E256L/STK14C88 and is available in the same packages and pin configurations, as well as in additional packages

Table 4. Packages Comparison

| Package | CY14E256L/STK14C88 | CY14E256LA |
|---|---|---|
| 32 SOIC | Available | Available |
| 32 CDIP | Available | Not Available |
| 44 TSOPII | Not Available | Available |

[+] Feedback

## Parameters

The CY14E256LA is a drop in replacement for CY14E256L/STK14C88 and will require minimum changes in the application board. However, the differences in parameters should be considered before replacing one part with the other. Table 5 lists the differences in parameters between CY14E256L/STK14C88 and CY14E256LA.

Table 5. Parameter Comparison

| Parameter | Description | Speed | CY14E256L/ STK14C88 | | CY14E256LA | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| **DC Parameters** | | | | | | | |
| $I_{CC1}$ | Average $V_{CC}$ Current | 25 ns | | 100 | | 70 | mA |
| | | 35 ns | | 85 | | - | |
| | | 45 ns | | 70 | | 52 | |
| $I_{CC2}$ | Average $V_{CC}$ Current during STORE | | | 3 | | 10 | mA |
| $I_{CC3}$ | Average $V_{CC}$ Current at $t_{RC} = 200$ ns, 5V, 25°C | | 10 (typ) | | 35 (typ) | | |
| $I_{CC4}$ | Average $V_{CAP}$ Current during AutoStore Cycle | | | 2 | | 5 | mA |
| $I_{SB1}$ | Average $V_{CC}$ Standby Current (Standby, Cycling Input) | 25 ns | | 31 | Not specified | | mA |
| | | 35 ns | | 26 | | | |
| | | 45 ns | | 23 | | | |
| $I_{SB}$ | $V_{CC}$ Standby Current | | | 1.5 | | 5 | mA |
| $I_{IX}$ | Input Leakage Current | | -5 | +5 | -1 | +1 | uA |
| $V_{IH}$ | Input High Voltage | | 2.2 | | 2 | | V |
| $V_{OH}$ | Output HIGH Voltage | | | 2.4 ($I_{OUT} = -4$ mA) | | 2.4 ($I_{OUT} = -2$ mA) | V |
| $V_{OL}$ | Output LOW Voltage | | | 0.4 ($I_{OUT} = 8$ mA) | | 0.4 ($I_{OUT} = 4$ mA) | V |
| $V_{CAP}$ | Storage Capacitor | | 54 to 260 | | 61 to 180 | | uF |
| **AC Switching Parameters** | | | | | | | |
| $t_{DOE}$ | Output Enable to Data Valid | 25 ns | | 10 | | 12 | mA |
| | | 35 ns | | 15 | | - | |
| | | 45 ns | | 20 | | 20 | |
| $t_{OHA}$ | Output Hold After Address Change | | 5 | | 3 | | ns |
| $t_{LZCE}$ | Chip Enable to Output Active | | 5 | | 3 | | ns |
| $t_{LZWE}$ | Output Active After End of Write | | 5 | | 3 | | ns |
| **AutoStore / Power Up RECALL Parameters** | | | | | | | |
| $t_{HRECALL}$ | Power Up RECALL Duration | | | 0.55 | | 20 | ms |
| $t_{STORE}$ | STORE Cycle Duration | | | 10 | | 8 | ms |
| $t_{VSBL}$ | Low Voltage Trigger ($V_{SWITCH}$) to $\overline{HSB}$ low | | | 300 | | 25 | ns |
| $V_{RESET}$ | Low Voltage Reset Level | | | 3.6 | Not Applicable | | V |
| $V_{SWITCH}$ | Low Voltage Trigger Level | | 4.0 | 4.5 | | 4.4 | V |
| $t_{DELAY}$ | Time Allowed to Complete SRAM Write Cycle | | 1,000 | | | 25 | ns |
| $V_{HDIS}$ | $\overline{HSB}$ Output Disable Voltage | | Not specified | | | 1.9 | V |
| $t_{LZHSB}$ | $\overline{HSB}$ To Output Active Time | | Not specified | | | 5 | us |
| $t_{HHHD}$ | $\overline{HSB}$ High Active Time | | Not specified | | | 500 | ns |

[+] Feedback

| Parameter | Description | Speed | CY14E256L/ STK14C88 | | CY14E256LA | | Unit |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| **Software Controlled STORE/RECALL cycle Parameters** | | | | | | | |
| $t_{HA}$ | Address Hold Time | | 20 | | 0 | | ns |
| $t_{RECALL}$ | STORE Cycle Duration | | | 20 | | 200 | us |
| **Hardware STORE cycle Parameters** | | | | | | | |
| $t_{HLBL}$ | $\overline{HSB}$ LOW to STORE Busy | | | 300 | | 25 ($t_{DELAY}$) | ns |
| $t_{DHSB}$ | $\overline{HSB}$ To Output Active Time when write latch not set | | Not specified | | | 25 | ns |

# Critical Considerations

The impact of the differences in CY14E256LA with respect to the CY14E256/STK14C88 in existing applications are discussed below. Board designers are recommended to review the detailed datasheets when converting to the new part.

### DC Parameters

$I_{CC1}$ (Average current at full speed) is lower in CY14E256LA and hence power supply design in applications with CY14E256L/STK14C88 would require no changes when replacing the nvSRAM with the CY14E256LA in spite of the higher values in the lower speed / higher standby current. The critical parameter to consider is the $V_{CAP}$.

### $V_{CAP}$

While most of the differences do not impact the application, the difference in $V_{CAP}$ is a critical consideration while converting from the older rev parts. $V_{CAP}$ is the capacitor which provides the required charge for AutoStore to complete NV store of the SRAM data during power down. The required capacitor range is different in the two parts.

Table 6. $V_{CAP}$ Comparison

| Description | CY14E256L/ STK14C88 | CY14E256LA |
|---|---|---|
| $V_{CAP}$ | 54uF to 260 uF | 61uF to 180 uF |

Therefore, any existing application using a capacitor value outside the overlapping range for the capacitor values needs to consider the impact of capacitor dimensions while changing to the new capacitor. Note: The capacitor range is the absolute value of the capacitor, net of tolerence.

### AC Switching Parameters

There are a few minor differences in switching parameters between the CY14E256LA and the CY14B256L/STK14C88 as listed in the Table 5. However, these differences do not impact most applications. For replacing 35ns speed parts, choose the 25ns speed parts as replacement (since 35ns speed grade is not available in the CY14E256LA).

### AutoStore / Power Up RECALL Parameters

$t_{HRECALL}$

The power up RECALL is much different in the CY14E256LA compared to the STK14C88 because of architecture differences.

Table 7. $t_{HRECALL}$ Comparison

| Description | CY14E256L/ STK14C88 | CY14E256LA |
|---|---|---|
| $t_{HRECALL}$ | 550 us | 20 ms |

This difference is not likely to affect applications since the initialization of the controller on the board happens at the same time. However, this should be taken into consideration when replacing the STK14C88 with CY14E256LA.

### Software Controlled STORE/RECALL Cycle Parameters

The Software cycle parameter $t_{RECALL}$ is different in CY14E256LA as described below. The software address sequences are identical to that in the old rev part.

### $t_{RECALL}$

Software RECALL time ($t_{RECALL}$) is higher in CY14E256LA.

Table 8. $t_{RECALL}$ Comparison

| Description | CY14E256L/ STK14C88 | CY14E256LA |
|---|---|---|
| $t_{RECALL}$ | 20 us | 200 us |

This difference could require firmware change in the application to increase the wait state when software RECALL is initiated.

### Software Sequence

The CY14E256LA has been designed to be compatible with the CY14E256L/STK14C88 in the software sequence modes. Hence, the same Software STORE and RECALL address sequences in CY14E256L/STK14C88 works in CY14E256LA, requiring no firmware change.

### Hardware STORE cycle Parameters

The Hardware STORE parameters are much improved in the CY14E256LA. The improvements are listed under the following section on Details of Improvement. No changes will be required in applications.

**AutoStore Inhibit**

The CY14E256L/STK14C88 has the AutoStore Inhibit feature and the CY14E256LA has AutoStore Disable mode. These two provide the same result of AutoStore disable but are done by different means – hardware in CY14E256L/STK14C88 and software in CY14E256LA.

To disable AutoStore in CY14E256L/STK14C88, the power is to be connected to the $V_{CAP}$ pin and the $V_{CC}$ pin is grounded (or left open). This cannot be done in CY14E256LA. For proper operation of the device, in CY14E256LA, power is to be connected to the $V_{CC}$ pin only. However, AutoStore disable is more easily done through simple software sequence. Therefore, if the CY14E256L/STK14C88 is to be replaced in an applicaiton where AutoStore has been disabled, then the layout has to be modified to connect the power to the $V_{CC}$ pin and a software sequence has to be used to disable AutoStore function followed by a Software STORE, the first time the board is powerd up.

**STORE Cycles**

The NV STORE cycles endurance in CY14E256LA is lower than the endurance in the older 0.8u technology. However, this would not affect in most applications since all nvSRAMs have infinite read/write endurance and the NV STORE would happen only during power down or during Software STORE. For example, if a system is powered down 10 times a day, then the NV STORE endurance is reached in 54 years in CY14E256LA.

**Data Retention**

The Data Retention in 0.13u part is vastly improved from the older technology part. The CY14E256LA has a data retention of 20 years at 85°C against the CY14E256L/STK14C88 data retention of 100 years at 55°C. This would translate to over 4 times improvement in data retention at the same temperatures.

[+] Feedback

# Details of Improvement

## Hardware STORE Related Improvements

$\overline{HSB}$ pin *(Hardware STORE Busy Indication/Hardware STORE Initiation)*

The $\overline{HSB}$ pin of the nvSRAM is an open drain I/O pin used to indicate or initiate a STORE operation. When a STORE operation is in progress, nvSRAM pulls the $\overline{HSB}$ pin low to indicate that the device is busy and cannot be accessed for read/write operation. During normal operation, the $\overline{HSB}$ pin can be pulled low to initiate a Hardware STORE operation.

As shown in Table 5, several timing parameters related to the $\overline{HSB}$ pin input and output have changed from CY14E256L/STK14C88 to CY14E256LA. All of these changes are improvements from the original part specification and should be considered as added benefits in your system while converting to the new part number.

Write Latch: When a write operation is done, a 'write latch' is set internally. When $\overline{HSB}$ is pulled low, nvSRAM checks this write latch before initiating a STORE. This is done to prevent any unnecessary loss of endurance cycles.

$t_{DELAY}$

If a write latch is set and the $\overline{HSB}$ pin is pulled low, CY14E256L/STK14C88 enables 1 us time for write operations to complete before STORE operation begins and reads and writes are inhibited. This potentially enables inadvertent data to be written to the nvSRAM during the $t_{DELAY}$ duration.

In CY14E256LA, the $t_{DELAY}$ parameter enables only one write cycle time for any ongoing write to complete after $\overline{HSB}$ pin is pulled low. This improvement provides better security from inadvertent write operations.

Also, if $\overline{HSB}$ pin is pulled low externally for a minimum of $t_{PHSB}$ time on CY14E256LA, the output driver of $\overline{HSB}$ pin pulls the pin low only indicating a STORE operation within 25 ns ($t_{DELAY}$). This parameter for $\overline{HSB}$ low to STORE busy is not specified in the CY14E256L/STK14C88. (See Figure 1 and Figure 2)

$\overline{HSB}$ LOW when write latch not set:

If no writes are performed since the last STORE/RECALL operation, STORE operation does not start when $\overline{HSB}$ is pulled low. However, the $\overline{HSB}$ pin is still internally pulled low for 1 us ($t_{DELAY}$) time in the CY14E256L/ STK14C88 device.

CY14E256LA device does not pull the $\overline{HSB}$ pin low internally if write latch is not set.

Figure 1. CY14E256L/STK14C88: AC Parameters Related to $\overline{HSB}$
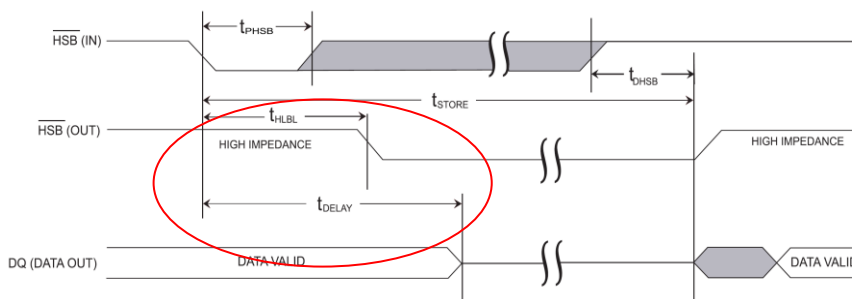


Figure 2. CY14E256LA: AC Parameters Related to $\overline{HSB}$

     [+] Feedback
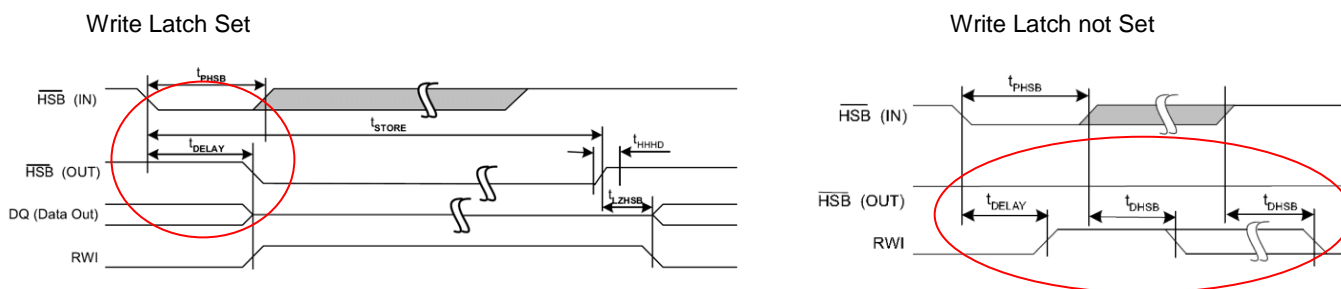
## Power up Recall Related Improvements

Additional parameters are specified in CY14E256LA such as $\overline{\text{HSB}}$ Output Disable Voltage ($V_{HDIS}$), $\overline{\text{HSB}}$ To Output Active Time ($t_{LZHSB}$), and $\overline{\text{HSB}}$ High Active Time ($t_{HHHD}$) which helps in system design. Refer to Figure 3 and Figure 4 for the definition of the additional specs in power up. Also, note that $\overline{\text{HSB}}$ remains low until the end of the power up in the new part. This would guard against the system inadvertently thinking the part has completed the boot up prior to real completion.

Figure 3. CY14E256L/STK14C88: Power Up Recall
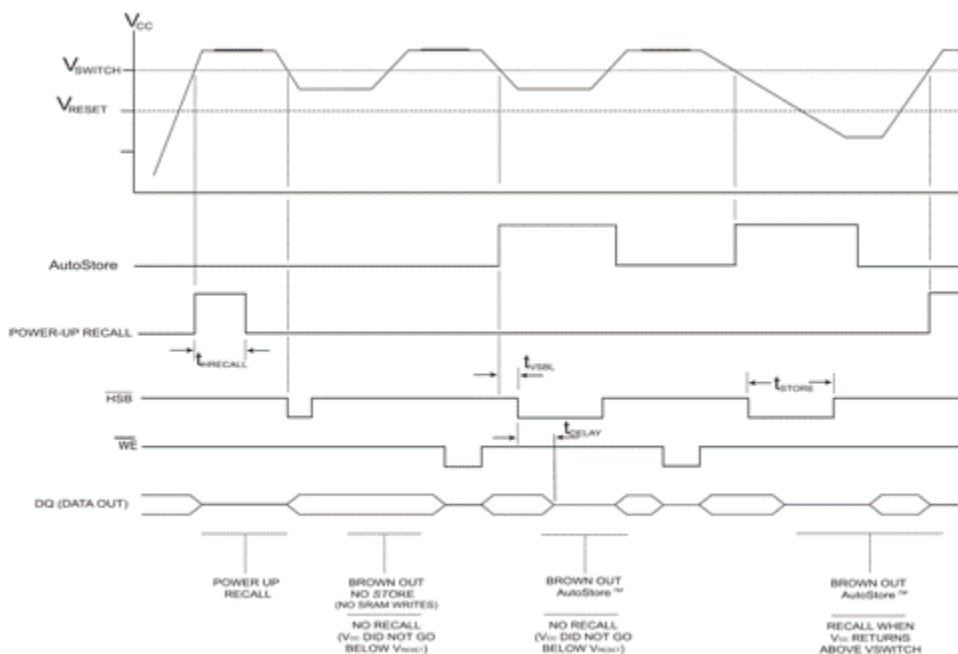


Figure 4. CY14E256LA: Power Up Recall
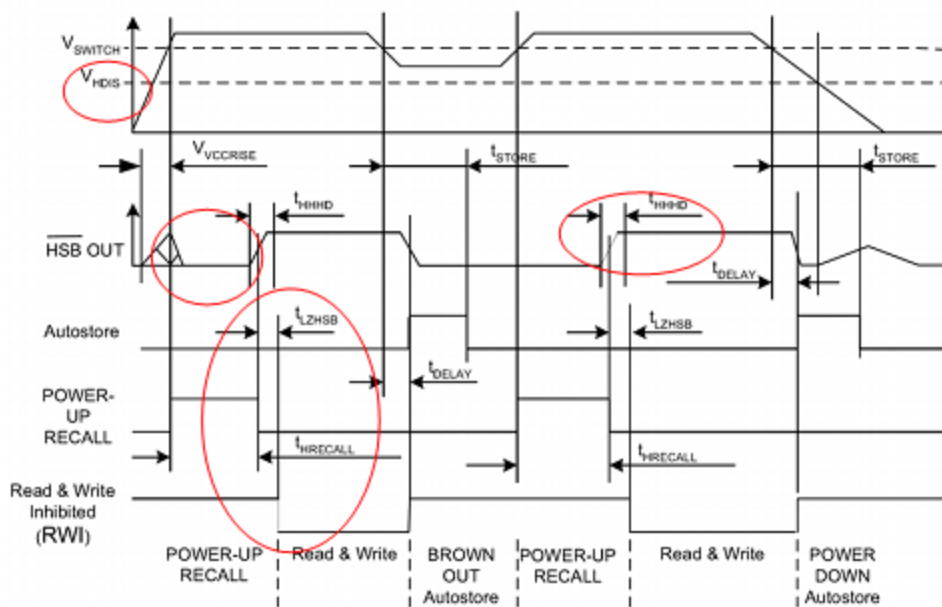
## Summary

The application note discusses the differences between CY14E256LA in the latest 0.13u technology and CY14E256L/STK14C88 in the 0.8u technology. Several parameters related to $\overline{\text{HSB}}$ and power up have improved / specified in the new device enabling faster device response, greater data security and ease of design.

CY14E256LA is pin compatible and can replace the CY14E256L/STK14C88 device with no changes or minimum changes to the firmware. The value of $V_{CAP}$ in the existing design needs to be considered while replacing the part.

# Document History

**Document Title: Converting from CY14E256L/STK14C88 to CY14E256LA**

**Document Number: 001-55663**

| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
|---|---|---|---|---|
| ** | 2773126 | PSR | 10/01/09 | New Spec. |

All trademarks and registered trademarks referenced herein are the property of their respective owners.

Cypress Semiconductor

198 Champion Court

San Jose, CA 95134-1709

Phone: 408-943-2600

Fax: 408-943-4730

http://www.cypress.com/