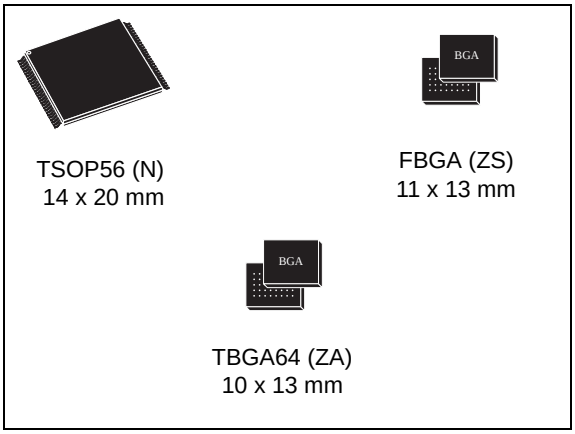
M29W256GH
M29W256GL

256-Mbit (32 Mbit x8 or 16 Mbit x16, page, uniform block) 3 V supply flash memory

Features

- Supply voltage
  - V_{CC} = 2.7 to 3.6 V for program, erase, read
  - V_{CCQ} = 1.65 to 3.6 V for I/O buffers
  - V_{PPH} = 12 V for fast program (optional)
- Asynchronous random/page read
  - Page size: 8 words or 16 bytes
  - Page access: 25, 30 ns
  - Random access: 60 (only available upon customer request) or 70, 80 ns
- Fast program commands
  - 32 words (64-byte write buffer)
- Enhanced buffered program commands
  - 256 words
- Programming time
  - 16 µs per byte/word typical
  - Chip program time: 10 s with V_{PPH} and 16 s without V_{PPH}
- Memory organization
  - M29W256G: 256 main blocks, 128 Kbytes/64 Kwords each
- Program/erase controller
  - Embedded byte/word program algorithms
- Program/ erase suspend and resume
  - Read from any block during program suspend
  - Read and program another block during erase suspend
- Unlock Bypass/Block Erase/Chip Erase/Write to Buffer/Enhanced Buffer Program commands
  - Faster production/batch programming



TSOP56 (N)
14 x 20 mm

FBGA (ZS)
11 x 13 mm

TBGA64 (ZA)
10 x 13 mm

  - Faster block and chip erase
- $V_{PP}/\overline{WP}$ pin for fast program and write: protects first or last block regardless of block protection settings
- Software protection:
  - Volatile protection
  - Non-volatile protection
  - Password protection
- Common flash interface
  - 64-bit security code
- 128-word extended memory block
  - Extra block used as security block or to store additional information
- Low power consumption
  - Standby and automatic standby
- Minimum 100,000 program/erase cycles per block
- RoHS compliant packages
- Automotive device grade: Temperature -40 °C to 85 °C (Automotive grade certified)

Table 1. Device summary

Root part number	Device code
M29W256GH / M29W256GL	227Eh + 2222h + 2201

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1 Description

The M29W256GH and M29W256GL are 256-Mbit (16 Mbit x16 or 32 Mbit x8) non-volatile flash memories that can be read, erased and reprogrammed. These operations can be performed using a single low voltage (2.7 to 3.6 V) supply. On power-up the memory defaults to its read mode.

The memory array is divided into 64-Kword/128-Kbyte uniform blocks that can be erased independently so it is possible to preserve valid data while old data is erased. Program and Erase commands are written to the command interface of the memory. An on-chip program/erase controller simplifies the process of programming or erasing the memory by taking care of all of the special operations that are required to update the memory contents. The end of a program or erase operation can be detected and any error conditions identified. The command set required to control the memory is consistent with JEDEC standards.

Chip Enable, Output Enable and Write Enable signals control the bus operation of the memory. They allow simple connection to most microprocessors, often without additional logic.

The M29W256GH and M29W256GL support asynchronous random read and page read from all blocks of the memory array. The devices also feature a write to buffer program capability that improves the programming throughput by programming in one shot a buffer of 32 words/64 bytes. The enhanced buffered program feature is also available to speed up the programming throughput, allowing to program 256 words in one shot (only in x16 mode). The $V_{PP}/\overline{WP}$ signal can be used to enable faster programming of the device.

The M29W256GH and M29W256GL have an extra block, the extended block, of 128 words in x16 mode or of 256 bytes in x8 mode that can be accessed using a dedicated command. The extended block can be protected and so is useful for storing security information. However the protection is not reversible, once protected the protection cannot be undone.

The device features different levels of hardware and software block protection to avoid unwanted program or erase (modify):

- Hardware protection:
  - The $V_{PP}/\overline{WP}$ provides a hardware protection of the highest and lowest block on the M29W256GH, M29W256GL, respectively.
- Software protection:
  - Volatile protection
  - Non-volatile protection
  - Password protection

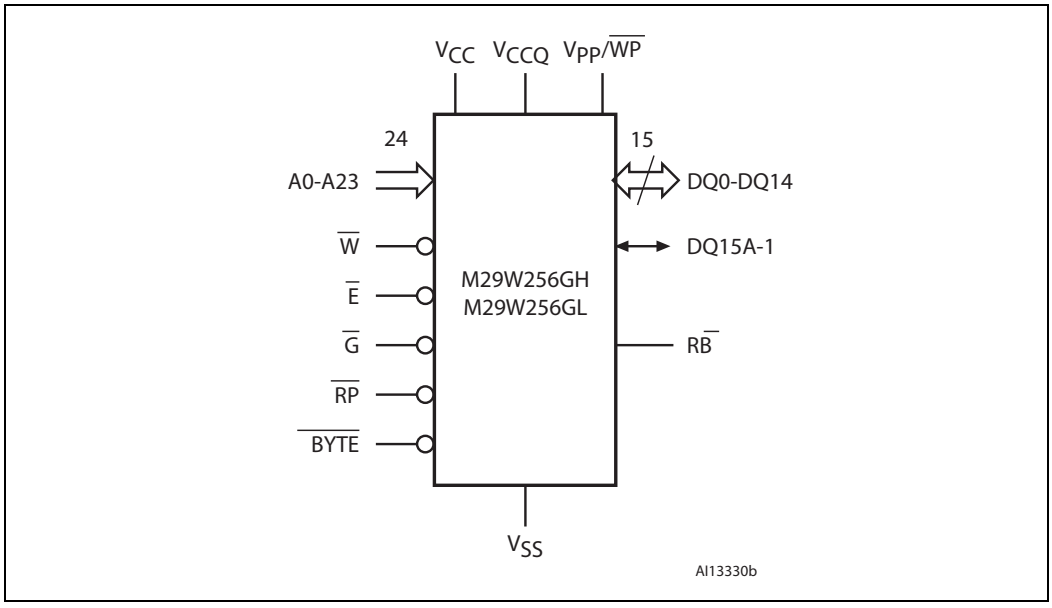
The M29W256GH and M29W256GL are offered in TSOP56 (14 x 20 mm), and TBGA64 (10 x 13 mm, 1 mm pitch), packages. The memories are delivered with all the bits erased (set to ‘1’).

Table 2. Signal names

Name	Description	Direction
A0-A23	Address inputs	Inputs
DQ0-DQ7	Data inputs/outputs	I/O
DQ8-DQ14	Data inputs/outputs	I/O
DQ15A–1	Data input/output or address input	I/O
$\overline{E}$	Chip enable	Input
$\overline{G}$	Output enable	Input
$\overline{W}$	Write enable	Input
$\overline{RP}$	Reset	Input
$R\overline{B}$	Ready/busy output	Output
$\overline{BYTE}$	Byte/word organization select	Input
V_{CCQ}	Input/output buffer supply voltage	Supply
V_{CC}	Supply voltage	Supply
$V_{PP}/\overline{WP}$(1)	V_{PP}/write protect	Supply/Input
V_{SS}	Ground	–
NC	Not connected	–

1. $V_{PP}/\overline{WP}$ may be left floating as it is internally connected to a pull-up resistor which enables program/erase operations.

Figure 1. Logic diagram



1. Also see *Appendix A* and *Table 37* for a full listing of the block addresses.

Figure 2. TSOP connections

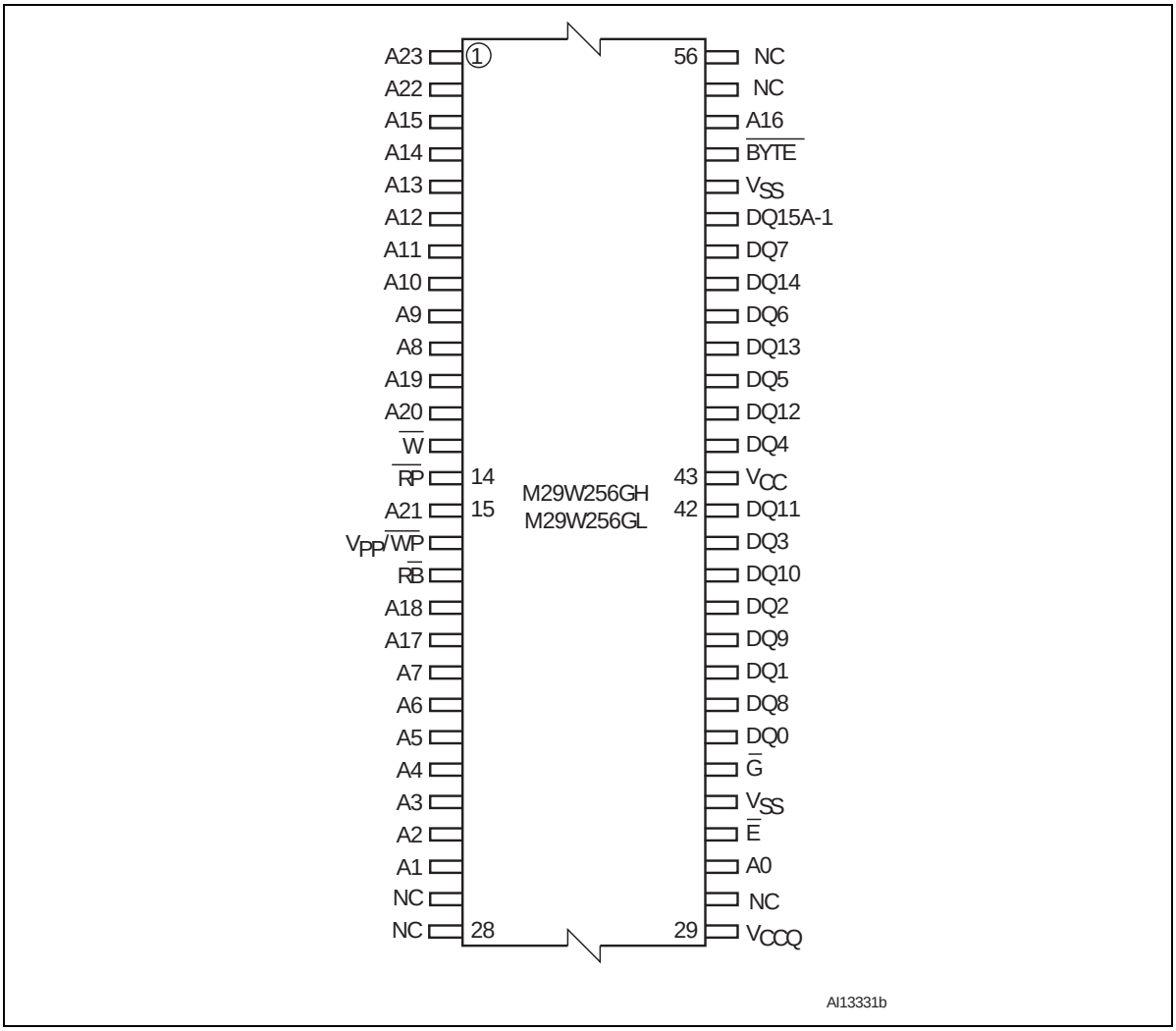


Figure 3. TBGA and FBGA connections (top view through package)

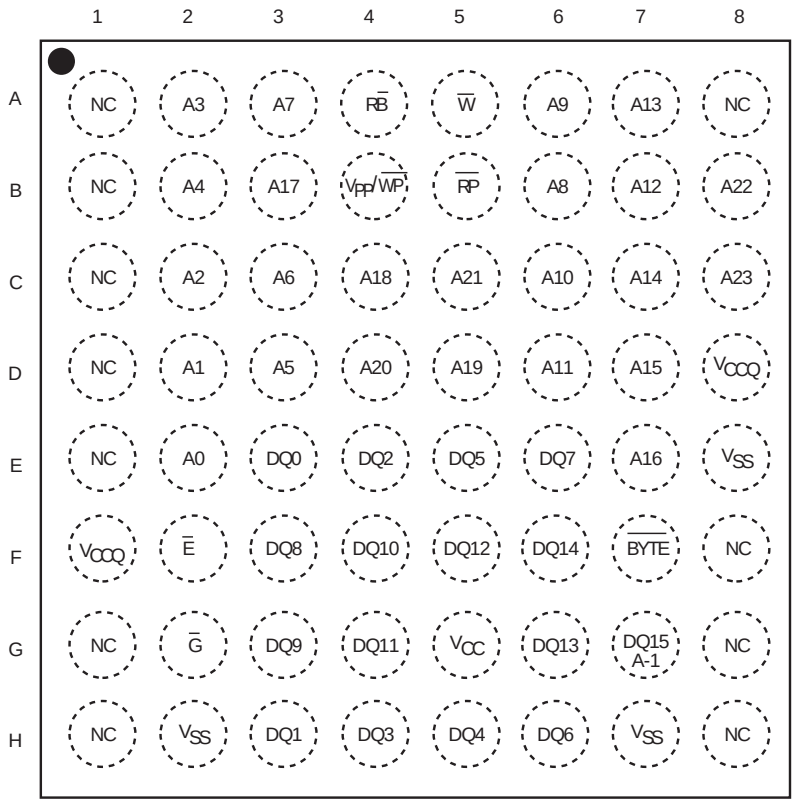
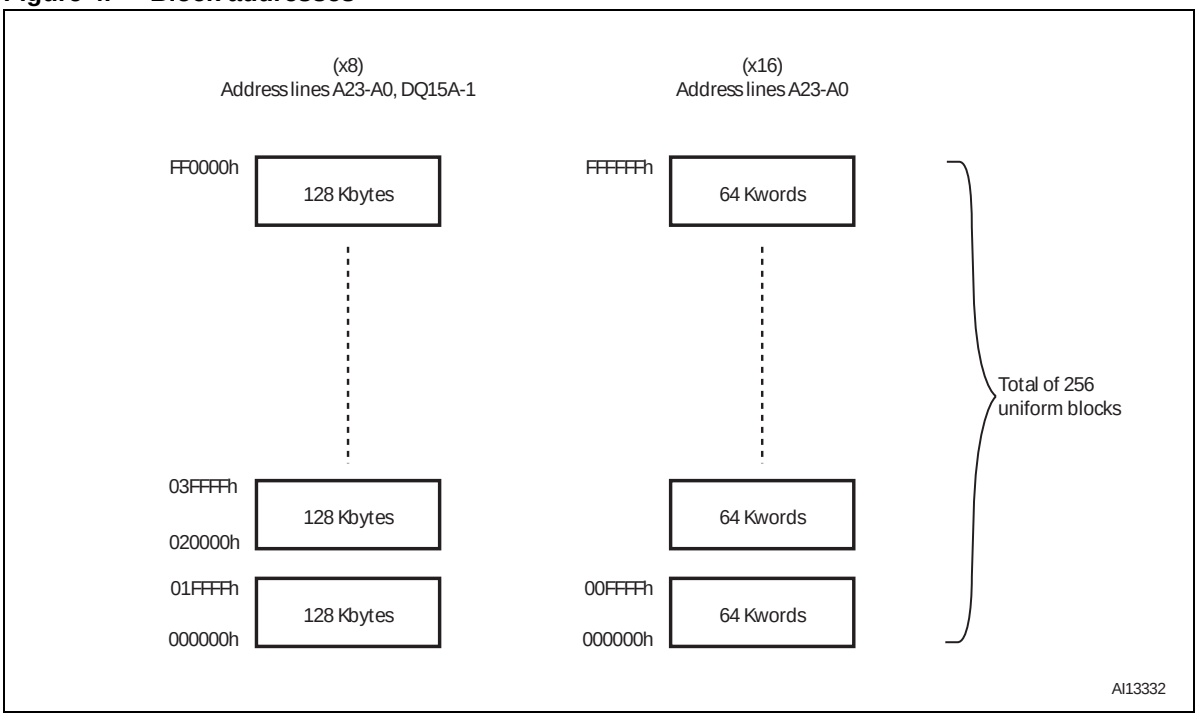


Figure 4. Block addresses



2 Signal descriptions

See *Figure 1: Logic diagram*, and *Table 2: Signal names*, for a brief overview of the signals connected to this device.

2.1 Address inputs (A0-A23)

The address inputs select the cells in the memory array to access during bus read operations. During bus write operations they control the commands sent to the command interface of the program/erase controller.

2.2 Data inputs/outputs (DQ0-DQ7)

The data I/O outputs the data stored at the selected address during a bus read operation. During bus write operations they represent the commands sent to the command interface of the internal state machine.

2.3 Data inputs/outputs (DQ8-DQ14)

The data I/O outputs the data stored at the selected address during a bus read operation when $\overline{BYTE}$ is High, V_{IH}. When $\overline{BYTE}$ is Low, V_{IL}, these pins are not used and are high impedance. During bus write operations the command register does not use these bits. When reading the status register these bits should be ignored.

2.4 Data inputs/outputs or address inputs (DQ15A–1)

When the device is in x 16 bus mode, this pin behaves as a data input/output pin (as DQ8-DQ14). When the device operates in x 8 bus mode, this pin behaves as the least significant bit of the address. Throughout the text consider references to the data input/output to include this pin when the device operates in x 16 bus mode and references to the address inputs to include this pin when the device operates in x 8 bus mode except when stated explicitly otherwise.

2.5 Chip enable ($\overline{E}$)

The chip enable pin, $\overline{E}$, activates the memory, allowing bus read and bus write operations to be performed. When chip enable is High, V_{IH}, all other pins are ignored.

2.6 Output enable ($\overline{G}$)

The output enable pin, $\overline{G}$, controls the bus read operation of the memory.

2.7 Write enable ($\overline{W}$)

The write enable pin, $\overline{W}$, controls the bus write operation of the memory's command interface.

2.8 V_{PP}/write protect ($V_{PP}/\overline{WP}$)

The V_{PP}/write protect pin provides two functions. The V_{PPH} function allows the memory to use an external high voltage power supply to reduce the time required for program operations. This is achieved by bypassing the unlock cycles.

The write protect function provides a hardware method of protecting the highest or lowest block (see *Section 1: Description*). When V_{PP}/write protect is Low, V_{IL}, the highest or lowest block is protected. Program and erase operations on this block are ignored while V_{PP}/write protect is Low.

When V_{PP}/write protect is High, V_{IH}, the memory reverts to the previous protection status of the highest or lowest block. Program and erase operations can now modify the data in this block unless the block is protected using block protection.

When V_{PP}/write protect is raised to V_{PPH} the memory automatically enters the unlock bypass mode (see *Section 6.2*).

When V_{PP}/write protect is raised to V_{PPH}, the execution time of the command is lower (see *Table 21: Program/erase times and program/erase endurance cycles*).

When V_{PP}/write protect returns to V_{IH} or V_{IL} normal operation resumes. During unlock bypass program operations the memory draws I_{PP} from the pin to supply the programming circuits. See the description of the Unlock Bypass command in the command interface section. The transitions from V_{IH} to V_{PPH} and from V_{PPH} to V_{IH} must be slower than t_{VHVPP} (see *Figure 23: Accelerated program timing waveforms*).

Never raise V_{PP}/write protect to V_{PPH} from any mode except read mode, otherwise the memory may be left in an indeterminate state. A 0.1 µF capacitor should be connected between the VPP/write protect pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during unlock bypass program (see I_{PP1}, I_{PP2}, I_{PP3}, I_{PP4} in *Table 27: DC characteristics*).

The V_{PP}/write protect pin may be left floating or unconnected because it features an internal pull-up.

Refer to *Table 3* for a summary of $V_{PP}/\overline{WP}$ functions.

Table 3. $V_{PP}/\overline{WP}$ functions

$V_{PP}/\overline{WP}$	Function
V_{IL}	Highest block protected on M29W256GH. Lowest block protected on M29W256GL.
V_{IH}	Highest and lowest block unprotected unless a software protection is activated (see *Section 4: Hardware protection*).
V_{PPH}	Unlock bypass mode. It supplies the current needed to speed up programming.

2.9 Reset ($\overline{RP}$)

The reset pin can be used to apply a hardware reset to the memory.

A hardware reset is achieved by holding reset Low, V_{IL}, for at least t_{PLPX}. After reset goes High, V_{IH}, the memory will be ready for bus read and bus write operations after t_{PHEL} or t_{RHEL}, whichever occurs last. See *Section 2.10: Ready/busy output (RB)*, *Table 31: Reset AC characteristics*, *Figure 21* and *Figure 22* for more details.

2.10 Ready/busy output ($\overline{RB}$)

The ready/busy pin is an open-drain output that can be used to identify when the device is performing a program or erase operation. During program or erase operations ready/busy is Low, V_{OL} (see *Table 22: Status register bits*). Ready/busy is high-impedance during read mode, auto select mode and erase suspend mode.

After a hardware reset, bus read and bus write operations cannot begin until ready/busy becomes high-impedance. See *Table 31: Reset AC characteristics*, *Figure 21* and *Figure 22*.

The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

2.11 Byte/word organization select ($\overline{BYTE}$)

It is used to switch between the x8 and x16 bus modes of the memory. When byte/word organization select is Low, V_{IL}, the memory is in x8 mode, when it is High, V_{IH}, the memory is in x16 mode.

2.12 V_{CC} supply voltage

V_{CC} provides the power supply for all operations (read, program and erase).

The command interface is disabled when the V_{CC} supply voltage is less than the lockout voltage, V_{LKO}. This prevents bus write operations from accidentally damaging the data during power-up, power-down and power surges. If the program/erase controller is programming or erasing during this time then the operation aborts and the memory contents being altered will be invalid.

A 0.1 µF capacitor should be connected between the V_{CC} supply voltage pin and the V_{SS} ground pin to decouple the current surges from the power supply. The PCB track widths must be sufficient to carry the currents required during program and erase operations (see I_{CC1}, I_{CC2}, I_{CC3} in *Table 27: DC characteristics*).

2.13 V_{CCQ} input/output supply voltage

V_{CCQ} provides the power supply to the I/O pins and enables all outputs to be powered independently from V_{CC}.

2.14 V_{SS} ground

V_{SS} is the reference for all voltage measurements. The device features two V_{SS} pins both of which must be connected to the system ground.

3 Bus operations

There are five standard bus operations that control the device. These are bus read (random and page modes), bus write, output disable, standby and automatic standby.

See *Table 4: Bus operations, 8-bit mode* and *Table 5: Bus operations, 16-bit mode* for a summary. Typical glitches of less than 5 ns on chip enable, write enable, and reset pins are ignored by the memory and do not affect bus operations.

3.1 Bus read

Bus read operations read from the memory cells, or specific registers in the command interface. To speed up the read operation the memory array can be read in page mode where data is internally read and stored in a page buffer. The page has a size of 8 words (or 16 bytes) and each word in the page is addressed by the address inputs A2-A0 in x 16 mode and A2-A0 plus DQ15A–1 in byte mode.

A valid bus read operation involves setting the desired address on the address inputs, applying a Low signal, V_{IL}, to chip enable and output enable and keeping write enable High, V_{IH}. The data inputs/outputs will output the value, see *Figure 13: Random read AC waveforms (8-bit mode)*, *Figure 15: Page read AC waveforms (16-bit mode)*, and *Table 28: Read AC characteristics*, for details of when the output becomes valid.

3.2 Bus write

Bus write operations write to the command interface. A valid bus write operation begins by setting the desired address on the address inputs. The address inputs are latched by the command interface on the falling edge of chip enable or write enable, whichever occurs last. The Data inputs/outputs are latched by the command interface on the rising edge of chip enable or write enable, whichever occurs first. Output enable must remain High, V_{IH}, during the whole bus write operation. See *Figure 16*, and *Figure 17*, Write AC waveforms, and *Table 29* and *Table 30*, Write AC characteristics, for details of the timing requirements.

3.3 Output disable

The data inputs/outputs are in the high impedance state when output enable is High, V_{IH}.

3.4 Standby

Driving chip enable High in read mode, causes the memory to enter standby mode and the data inputs/outputs pins are placed in the high-impedance state. To reduce the supply current to the standby supply current, I_{CC2}, chip enable should be held within $V_{CC} \pm 0.3$ V. For the standby current level see *Table 27: DC characteristics*.

During program or erase operations the memory will continue to use the program/erase supply current, I_{CC3}, for program or erase operations until the operation completes.

3.5 Reset

During reset mode the memory is deselected and the outputs are high impedance. The memory is in reset mode when $\overline{RP}$ is at V_{IL}. The power consumption is reduced to the standby level, independently from the chip enable, output enable or write enable inputs.

3.6 Automatic standby

Automatic standby allows the memory to achieve low power consumption during read mode.

After a read operation, if CMOS levels (V_{CC} ± 0.3 V) are used to drive the bus and the bus is inactive for t_{AVQV} + 30 ns or more, the memory enters automatic standby where the internal supply current is reduced to the standby supply current, I_{CC2} (see *Table 27: DC characteristics*). The data inputs/outputs will still output data if a bus read operation is in progress.

The power supplier of data bus, V_{CCQ}, can have a null consumption (depending on load circuits connected with data bus) when the memory enters automatic standby.

3.7 Auto select mode

The auto select mode allows the system or the programming equipment to read the electronic signature, verify the protection status of the extended memory block, and apply/remove block protection. For example, this mode can be used by a programming equipment to automatically match a device and the application code to be programmed.

There are two methods to enter auto select mode:

- programmer method:

  Additional bus operations are used. They require V_{ID} to be applied to address pin A9. Refer to *Table 6*, *Table 7*, *Table 8*, and *Table 9* for a description of the bus operations required to read the electronic signature using the programmer method

- in-system method:

  The auto select mode is entered by issuing the Auto Select command (see *Section 6.1.2*). It is not necessary to apply V_{ID} to A9.

At power-up, the device is in read mode, and can then be put in auto select mode by using one of the methods described above.

The device cannot enter auto select mode when a program or erase operation is ongoing ($\overline{RB}$ Low). However, auto select mode can be entered if the erase operation has been suspended by issuing an Erase Suspend command (see *Section 6.1.6*).

The auto select mode is exited by performing a reset. The device is returned to read mode, except if the auto select mode was entered after an Erase Suspend or a Program Suspend command. In this case, it returns to the erase or program suspend mode.

3.7.1 Read electronic signature

The memory has two codes, the manufacturer code and the device code used to identify the memory. These codes can be accessed by performing read operations with control signals and addresses set as shown in *Table 6: Read electronic signature - auto select mode - programmer method (8-bit mode)* and *Table 7: Read electronic signature - auto select mode - programmer method (16-bit mode)*.

These codes can also be accessed by issuing an Auto Select command (see *Section 6.1.2: Auto Select command*).

3.7.2 Verify extended memory block protection indicator

The extended memory block is either factory locked or customer lockable.

The protection status of the extended memory block (factory locked or customer lockable) can be accessed by reading the extended memory block protection indicator. It can be read in auto select mode using either the programmer (see *Table 8* and *Table 9*) or the in-system method (see *Table 12* and *Table 13*).

The protection status of the extended memory block is then output on bit DQ7 of the data input/outputs (see *Table 4* and *Table 5*, Bus operations in 8-bit and 16-bit mode).

3.7.3 Verify block protection status

The protection status of a block can be directly accessed by performing a read operation with control signals and addresses set as shown in *Table 8* and *Table 9*.

If the block is protected, then 0001h (in x 16 mode) is output on data input/outputs DQ0-DQ15, otherwise 0000h is output.

3.7.4 Hardware block protect

The $V_{PP}/\overline{WP}$ pin can be used to protect the highest or lowest block. When $V_{PP}/\overline{WP}$ is at V_{IL} the highest (M29W256GH) or lowest block (M29W256GL) is protected and remains protected regardless of the block protection status or the reset pin state.

Table 4. Bus operations, 8-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address Inputs	Data inputs/outputs	
						A23, A0, DQ15A-1	DQ14-DQ8	DQ7-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Hi-Z	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Hi-Z	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If $\overline{WP}$ is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 5. Bus operations, 16-bit mode

Operation[1]	$\overline{E}$	$\overline{G}$	$\overline{W}$	$\overline{RP}$	$V_{PP}/\overline{WP}$	Address inputs	Data inputs/outputs
						A23, A0	DQ15A-1, DQ14-DQ0
Bus read	V_{IL}	V_{IL}	V_{IH}	V_{IH}	X	Cell address	Data output
Bus write	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X[2]	Command address	Data input[3]
Standby	V_{IH}	X	X	V_{IH}	X	X	Hi-Z
Output disable	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z
Reset	X	X	X	V_{IL}	X	X	Hi-Z

1. X = V_{IL} or V_{IH}.
2. If $\overline{WP}$ is Low, V_{IL}, the outermost block remains protected.
3. Data input as required when issuing a command sequence, performing data polling or block protection.

Table 6. Read electronic signature - auto select mode - programmer method (8-bit mode)

Read cycle(1)	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs										Data inputs/outputs	
				A23-A10	A9	A8-A7	A6	A5-A4	A3	A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	X	X	20h
Device code (cycle 1)									V_{IL}	V_{IL}	V_{IL}	V_{IH}	X	X	7Eh (both devices)
Device code (cycle 2)									V_{IH}	V_{IH}	V_{IH}	V_{IL}	X	X	22h (both devices)
Device code (cycle 3)									V_{IH}	V_{IH}	V_{IH}	V_{IH}	X	X	01h (both devices)

1. X = V_{IL} or V_{IH}.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

Table 7. Read electronic signature - auto select mode - programmer method (16-bit mode)

Read cycle(1)	$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs
				A23-A10	A9	A8-A7	A6	A5-A4	A3	A2	A1	A0	DQ15A-1, DQ14-DQ0
Manufacturer code	V_{IL}	V_{IL}	V_{IH}	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	0020h
Device code (cycle 1)									V_{IL}	V_{IL}	V_{IL}	V_{IH}	227Eh (both devices)
Device code (cycle 2)									V_{IH}	V_{IH}	V_{IH}	V_{IL}	2222h (both devices)
Device code (cycle 3)									V_{IH}	V_{IH}	V_{IH}	V_{IH}	2201h (both devices)

1. X = V_{IL} or V_{IH}.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

Table 8. Block protection - auto select mode - programmer method (8-bit mode)

Operation[1]		$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs	
					A23-A16	A14-A10	A9	A8-A7	A6	A5-A4	A3-A2	A1	A0	DQ15A-1	DQ14-DQ8	DQ7-DQ0
Verify extended memory block protection indicator (bit DQ7)	M29W256GL	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	X	X	89h (factory locked) 09h (customer lockable)
	M29W256GH															99h (factory locked) 19h (customer lockable)
Verify block protection status					BAd								V_{IL}			01h (protected) 00h (unprotected)

1. X = V_{IL} or V_{IH}. BAd any address in the block.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

Table 9. Block protection - auto select mode - programmer method (16-bit mode)

Operation[1]		$\overline{E}$	$\overline{G}$	$\overline{W}$	Address inputs									Data inputs/outputs
					A23-A16	A14-A10	A9	A8-A7	A6	A5-A4	A3-A2	A1	A0	DQ15A-1, DQ14-DQ0
Verify extended memory block indicator (bit DQ7)	M29W256GL	V_{IL}	V_{IL}	V_{IH}	X	X	V_{ID} (2)	X	V_{IL}	X	V_{IL}	V_{IH}	V_{IH}	0089h (factory locked) 0009h (customer lockable)
	M29W256GH													0099h (factory locked) 0019h (customer lockable)
Verify block protection status					BAd								V_{IL}	0001h (protected) 0000h (unprotected)

1. X = V_{IL} or V_{IH}. BAd any address in the block.
2. When using the in-system method, applying V_{ID} to A9 is not required. A9 can be either V_{IL} or V_{IH}.

4 Hardware protection

The M29W256GH and M29W256GL feature a $V_{PP}/\overline{WP}$ pin that protects the highest or lowest block. Refer to *Section 2: Signal descriptions* for a detailed description of the signal.

5 Software protection

The M29W256GH and M29W256GL have three different software protection modes:

- Volatile protection
- Non-volatile protection
- Password protection

On first use all parts default to operate in non-volatile protection mode and the customer is free to activate the non-volatile or the password protection mode.

The desired protection mode is activated by setting either the one-time programmable non-volatile protection mode lock bit, or the password protection mode lock bit of the lock register (see *Section 5.4: Lock register*). Programming the non-volatile protection mode lock bit or the password protection mode lock bit, to '0' will permanently activate the non-volatile or the password protection mode, respectively. These two bits are one-time programmable and non-volatile: once the protection mode has been programmed, it cannot be changed and the device will permanently operate in the selected protection mode. It is recommended to activate the desired software protection mode when first programming the device.

The non-volatile and password protection modes both provide non-volatile protection. Volatilely protected blocks and non-volatilely protected blocks can co-exist within the memory array. However, the volatile protection only control the protection scheme for blocks that are not protected using the non-volatile or password protection.

If the user attempts to program or erase a protected block, the device ignores the command and returns to read mode.

The device is shipped with all blocks unprotected. The block protection status can be read either by performing a read electronic signature (see *Table 6* and *Table 7*) or by issuing an Auto Select command (see *Table 11: Block protection status*).

For the lowest and highest blocks, an even higher level of block protection can be achieved by locking the blocks using the non-volatile protection and then by holding the $V_{PP}/\overline{WP}$ pin Low.

5.1 Volatile protection mode

The volatile protection allows the software application to easily protect blocks against inadvertent change. However, the protection can be easily disabled when changes are needed. Volatile protection bits, VPBs, are volatile and unique for each block and can be individually modified. VPBs only control the protection scheme for unprotected blocks that have their non-volatile protection bits, NVPBs, cleared (erased to '1') (see *Section 5.2: Non-volatile protection mode* and *Section 6.4.4: Non-volatile protection mode command set*).

By issuing the VPB Program or VPB Clear commands, the VPBs are set (programmed to '0') or cleared (erased to '1'), thus placing each block in the protected or unprotected state respectively. The VPBs can be set (programmed to '0') or cleared (erased to '1') as often as needed.

When the parts are first shipped, or after a power-up or hardware reset, the VPBs can be set or cleared depending upon the ordering option chosen:

- If the option to clear the VPBs after power-up is selected, then the blocks can be programmed or erased depending on the NVPBs state (see *Table 11: Block protection status*)
- If the option to set the VPBs after power-up is selected, the blocks default to be protected.

Refer to *Section 6.4.3* for a description of the volatile protection mode command set.

5.2 Non-volatile protection mode

5.2.1 Non-volatile protection bits

A non-volatile protection bit (NVPB) is assigned to each block.

When a NVPB is set to '0', the associated block is protected, preventing any program or erase operations in this block.

The NVPB bits are set individually by issuing a NVPB Program command. They are non-volatile and will remain set through a hardware reset or a power-down/power-up sequence.

The NVPBs cannot be cleared individually, they can only be cleared all at the same time by issuing a Clear all Non-volatile Protection bits command.

The NVPBs can be protected all at a time by setting a volatile bit, the NVPB lock bit (see *Section 5.2.2: Non-volatile protection bit lock bit*).

If one of the non-volatile protected blocks needs to be unprotected (corresponding NVPB set to '1'), a few more steps are required:

1. First, the NVPB lock bit must be cleared by either putting the device through a power cycle, or hardware reset
2. The NVPBs can then be changed to reflect the desired settings
3. The NVPB lock bit must be set once again to lock the NVPBs. The device operates normally again.

Note: 1 To achieve the best protection, it is recommended to execute the NVPB Lock Bit Program command early in the boot code and to protect the boot code by holding V_{PP}/$\overline{WP}$ Low, V_{IL}.

2 The NVPBs and VPBs have the same function when V_{PP}/$\overline{WP}$ pin is High, V_{IH}, as they do when V_{PP} /$\overline{WP}$ pin is at the voltage for program acceleration (V_{PPH}).

Refer to *Table 11: Block protection status* and *Figure 5: Software protection scheme* for details on the block protection mechanism, and to *Section 6.4.4* for a description of the non-volatile protection mode command set.

5.2.2 Non-volatile protection bit lock bit

The non-volatile protection bit lock bit (NVPB lock bit) is a global volatile bit for all blocks.

When set (programmed to '0'), it prevents changing the state of the NVPBs. When cleared (programmed to '1'), the NVPBs can be set and reset using the NVPB Program command and Clear all NVPBs command, respectively.

There is only one NVPB lock bit per device.

Refer to *Section 6.4.5* for a description of the NVPB lock bit command set.

Note: 1 No software command unlocks this bit unless the device is in password protection mode; it can be cleared only by taking the device through a hardware reset or a power-up.

2 The NVPB lock bit must be set (programmed to '0') only after all NVPBs are configured to the desired settings.

5.3 Password protection mode

The password protection mode provides an even higher level of security than the non-volatile protection mode by requiring a 64-bit password for unlocking the device NVPB lock bit.

In addition to this password requirement, the NVPB lock bit is set '0' after power-up and reset to maintain the device in password protection mode. Successful execution of the Password Unlock command by entering the correct password clears the NVPB lock bit, allowing for block NVPBs to be modified.

If the password provided is not correct, the NVPL lock bit remains locked and the state of the NVPBs cannot be modified.

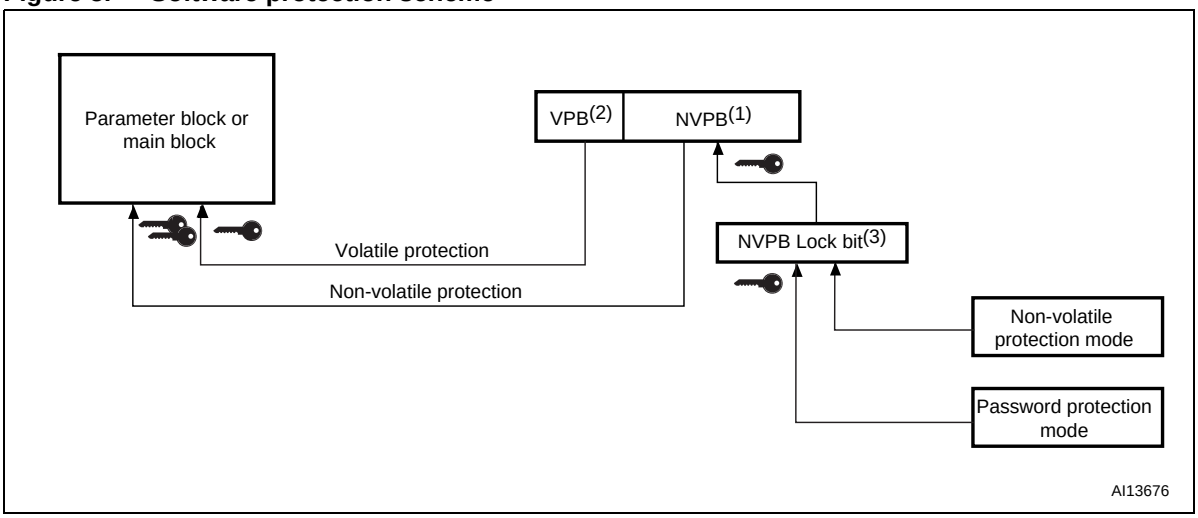
To place the device in password protection mode, the following steps are required:

1. Prior to entering the password protection mode, it is necessary to set a 64-bit password and to verify it (see *Password protection mode command set on page 47*). Password verification is only allowed during the password programming operation
2. The password protection mode is then activated by programming the password protection mode lock bit to '0'. This operation is not reversible and once the bit is programmed it cannot be erased, the device permanently remains in password protection mode, and the 64-bit password can neither be retrieved nor reprogrammed. Moreover, all commands to the address where the password is stored, are disabled. Refer to *Table 11: Block protection status* and *Figure 5: Software protection scheme* for details on the block protection scheme.

Refer to *Section 6.4.6* for a description of the password protection mode command set.

Note: There is no means to verify the password after it is set. If the password is lost after setting the password mode lock bit, there is no way to clear the NVPB lock bit.

Figure 5. Software protection scheme



1. NVPBs default to ‘1’ (block unprotected) after power-up and hardware reset. A block is protected or unprotected when its NVPB is set to ‘0’ and ‘1’, respectively. NVPBs are programmed individually and cleared collectively.
2. VPB default status depends on ordering option. A block is protected or unprotected when its VPB is set to ‘0’ and ‘1’, respectively. VPBs are programmed and cleared individually. For the volatile protection to be effective, the NVPB lock bit must be set to ‘0’ (NVPB bits unlocked) and the block NVPB must be set to ‘1’ (block unprotected).
3. The NVPB lock bit is volatile and default to ‘1’ (NVPB bits unlocked) after power-up and hardware reset. NVPB bits are locked by setting the NVPB lock bit to ‘0’. Once programmed to ‘0’, the NVPB lock bit can be reset to ‘1’ only be taking the device through a power-up or hardware reset.

5.4 Lock register

The lock register is a 16-bit one-time programmable register. The bits in the lock register are summarized in *Table 10: Lock register bits*.
The lock register allows configuration of memory blocks and extended memory block protection (see *Table 11: Block protection status*).
See *Section 6.4.1: Lock Register Command Set* for a description of the commands allowing to read and program the lock register.

5.4.1 Extended block protection bit (DQ0)

If the device has not been shipped with the extended memory block factory locked, the block can be protected by setting the extended memory block protection bit, DQ0, to ‘0’. However, this bit is one-time programmable and once protected the extended memory block cannot be unprotected.

The extended memory block protection status can be read in auto select mode either by applying V_{ID} to A9 (see *Table 8* and *Table 9*) or by issuing an Auto Select command (see *Table 12* and *Table 13*).

5.4.2 Non-volatile protection mode lock bit (DQ1)

The non-volatile protection mode lock bit, DQ1, is one-time programmable. Programming (change the first apex to ‘0’) this bit permanently places the device in non-volatile protection mode.

By default the memory operates in non-volatile protection mode independently whether the non-volatile protection mode lock bit, DQ1, is programmed. From Factory the memory blocks can be either unprotected (change the first apex to ‘1’) or protected (change the first apex to ‘0’), according to the ordering option that has been chosen.

Any attempt to program the non-volatile protection mode lock bit when the password protection mode bit is programmed causes the operation to abort and the device to return to read mode.

5.4.3 Password protection mode lock bit (DQ2)

The password protection mode lock bit, DQ2, is one-time programmable. Programming (setting to ‘0’) this bit permanently places the device in password protection mode.

Any attempt to program the password protection mode lock bit when the non-volatile protection mode bit is programmed causes the operation to abort and the device to return to read mode.

5.4.4 DQ15 to DQ3 reserved

DQ15 to DQ3 are reserved and during programming they must be held at '1'.

Table 10. Lock register bits(1)

DQ15-3	DQ2	DQ1	DQ0
Reserved	Password protection mode lock bit	Non-volatile protection mode lock bit	Extended block protection bit

1. DQ0, DQ1 and DQ2 lock register bits are set to ‘1’ when shipped from the factory.

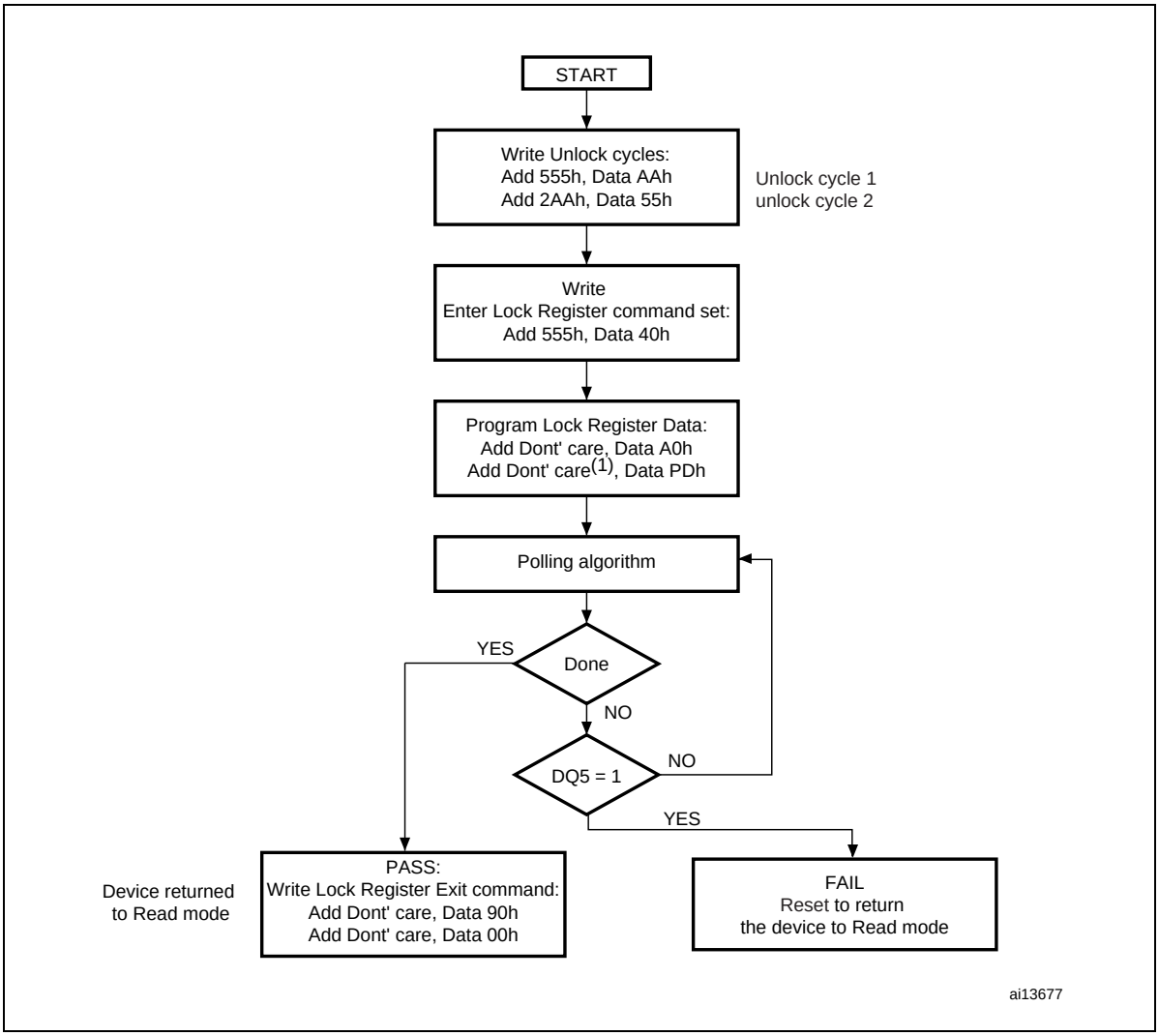
Table 11. Block protection status

NVPB lock bit(1)	Block NVPB(2)	Block VPB(3)	Block protection status	Block protection status
0	0	x	01h	Block protected (non-volatile protection through NVPB)
0	1	1	00h	Block unprotected
0	1	0	00h	Block protected (volatile protection through VPB)
1	0	x	01h	Block protected (non-volatile protection through NVPB)
1	1	0	01h	Block protected (volatile protection through VPB)
1	1	1	00h	Block unprotected

1. If the NVPB lock bit is set to ‘0’, all NVPBs are locked. If the NVPB lock bit is set to ‘1’, all NVPBs are unlocked.

2. If the block NVPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.
3. If the block VPB is set to ‘0’, the block is protected, if set to ‘1’, it is unprotected.

Figure 6. Lock register program flowchart



1. PD is the programmed data (see *Table 10: Lock register bits*).
2. The lock register can only be programmed once.

6 Command interface

All bus write operations to the memory are interpreted by the command interface. Commands consist of one or more sequential bus write operations. Failure to observe a valid sequence of bus write operations will result in the memory returning to read mode. The long command sequences are imposed to maximize data security.

The address used for the commands changes depending on whether the memory is in 16-bit or 8-bit mode.

6.1 Standard commands

See either *Table 12*, or *Table 13*, depending on the configuration that is being used, for a summary of the standard commands.

6.1.1 Read/Reset command

The device is in read mode after reset or after power-up.

The Read/Reset command returns the memory to read mode. It also resets the errors in the status register. Either one or three bus write operations can be used to issue the Read/Reset command.

The Read/Reset command can be issued, between bus write cycles before the start of a program or erase operation, to return the device to read mode. If the Read/Reset command is issued during the timeout of a block erase operation, the memory will take up to 10 µs to abort. During the abort period no valid data can be read from the memory.

The Read/Reset command will not abort an erase operation when issued while in erase suspend.

6.1.2 Auto Select command

The Auto Select command puts the device in auto select mode, when using the in-system method (see *Section 3.7: Auto select mode*). When in auto select mode, the system can read the manufacturer code, the device code, the protection status of each block (block protection status) and the extended memory block protection indicator.

Three consecutive bus write operations are required to issue the Auto Select command. Once the Auto Select command is issued bus read operations to specific addresses output the manufacturer code, the device code, the extended memory block protection indicator and a block protection status (see *Table 12* and *Table 13* in conjunction with *Table 6*, *Table 7*, *Table 8*, and *Table 9*). The memory remains in auto select mode until a Read/Reset or CFI Query command is issued.

6.1.3 Read CFI Query command

The memory contains an information area, named CFI data structure, which contains a description of various electrical and timing parameters, density information and functions supported by the memory. See *Appendix B*, *Table 39*, *Table 40*, *Table 41, Table 42, Table 43* and *Table 44* for details on the information contained in the common flash interface (CFI) memory area.

The Read CFI Query command is used to put the memory in read CFI query mode. Once in read CFI query mode, bus read operations to the memory will output data from the common flash interface (CFI) memory area. One bus write cycle is required to issue the Read CFI Query command. This command is valid only when the device is in the read array or auto select mode.

The Read/Reset command must be issued to return the device to the previous mode (the read array mode or auto select mode). A second Read/Reset command is required to put the device in read array mode from auto select mode.

6.1.4 Chip Erase command

The Chip Erase command can be used to erase the entire chip. Six bus write operations are required to issue the Chip Erase command and start the program/erase controller.

If some block are protected, then these are ignored and all the other blocks are erased. If all of the blocks are protected the Chip Erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the erase operation the memory will ignore all commands, including the Erase Suspend command. It is not possible to issue any command to abort the operation. Typical chip erase times are given in *Table 21*. All bus read operations during the chip erase operation will output the status register on the data inputs/outputs. See *Section 7: Status register* for more details.

After the chip erase operation has completed the memory will return to the read mode, unless an error has occurred. When an error occurs the memory will continue to output the status register. A Read/Reset command must be issued to reset the error condition and return to read mode.

The Chip Erase command sets all of the bits in unprotected blocks of the memory to ’1’. All previous data is lost.

The chip erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the entire chip.

6.1.5 Block Erase command

The Block Erase command can be used to erase a list of one or more blocks. It sets all of the bits in the unprotected selected blocks to ’1’. All previous data in the selected blocks is lost.

Six bus write operations are required to select the first block in the list. Each additional block in the list can be selected by repeating the sixth bus write operation using the address of the additional block. After the command sequence is written, a block erase timeout occurs. During the timeout period, additional sector addresses and sector erase commands may be written. Once the program/erase controller has started, it is not possible to select any more blocks. Each additional block must therefore be selected within the timeout period of the last block. The timeout timer restarts when an additional block is selected. After the sixth bus write operation, a bus read operation outputs the status register. See *Figure 16: Write enable controlled program waveforms (8-bit mode)* and *Figure 17: Write enable controlled program waveforms (16-bit mode)* for details on how to identify if the program/erase controller has started the block erase operation.

After the block erase operation has completed, the memory returns to the read mode, unless an error has occurred. When an error occurs, bus read operations will continue to output the status register. A Read/Reset command must be issued to reset the error condition and return to read mode.

If any selected blocks are protected then these are ignored and all the other selected blocks are erased. If all of the selected blocks are protected the block erase operation appears to start but will terminate within about 100 µs, leaving the data unchanged. No error condition is given when protected blocks are ignored.

During the block erase operation the memory ignores all commands except the Erase Suspend command and the Read/Reset command which is only accepted during the timeout period. Typical block erase time and block erase timeout are given in *Table 21*.

The block erase operation is aborted by performing a reset or powering down the device. In this case, data integrity cannot be ensured, and it is recommended to erase again the blocks aborted.

6.1.6 Erase Suspend command

The Erase Suspend command can be used to temporarily suspend a block erase operation. One bus write operation is required to issue the command together with the block address.

The program/erase controller suspends the erase operation within the erase suspend latency time of the Erase Suspend command being issued. However, when the Erase Suspend command is written during the block erase timeout, the device immediately terminates the timeout period and suspends the erase operation.

Once the program/erase controller has stopped, the memory operates in read mode and the erase is suspended.

During erase suspend it is possible to read and execute program or write to buffer program operations in blocks that are not suspended; both read and program operations behave as normal on these blocks. Reading from blocks that are suspended will output the status register. If any attempt is made to program in a protected block or in the suspended block then the Program command is ignored and the data remains unchanged. In this case the status register is not read and no error condition is given.

It is also possible to issue the Auto Select (after entering Autoselect mode), Read CFI Query and Unlock Bypass commands during an erase suspend. The Read/Reset command must be issued to return the device to read array mode before the Resume command will be accepted.

During erase suspend a bus read operation to the extended memory block will output the extended memory block data. Once in the extended block mode, the Exit Extended Block command must be issued before the erase operation can be resumed.

The Erase Suspend command is ignored if written during chip erase operations.

Refer to *Table 21: Program/erase times and program/erase endurance cycles* for the values of block erase timeout and block erase suspend latency time.

If the erase suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to erase again the blocks suspended.

6.1.7 Erase Resume command

The Erase Resume command is used to restart the program/erase controller after an erase suspend.

The device must be in read array mode before the Resume command will be accepted. An erase can be suspended and resumed more than once.

6.1.8 Program command

The Program command can be used to program a value to one address in the memory array at a time. The command requires four bus write operations, the final write operation latches the address and data in the internal state machine and starts the program/erase controller.

Programming can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.9: Program Suspend command* and *Section 6.1.10: Program Resume command*).

If the address falls in a protected block then the program command is ignored, the data remains unchanged. The status register is never read and no error condition is given.

After programming has started, bus read operations output the status register content. See *Figure 16: Write enable controlled program waveforms (8-bit mode)* and *Figure 17: Write enable controlled program waveforms (16-bit mode)* for more details. Typical program times are given in *Table 21: Program/erase times and program/erase endurance cycles*.

After the program operation has completed the memory will return to the read mode, unless an error has occurred. When an error occurs, bus read operations to the memory continue to output the status register. A Read/Reset command must be issued to reset the error condition and return to read mode.

One of the erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

The program operation is aborted by performing a reset or powering-down the device. In this case data integrity cannot be ensured, and it is recommended to reprogram the word or byte aborted.

6.1.9 Program Suspend command

The Program Suspend command allows the system to interrupt a program operation so that data can be read from any block. When the Program Suspend command is issued during a program operation, the device suspends the program operation within the program suspend latency time (see *Table 21: Program/erase times and program/erase endurance cycles*) and updates the status register bits.

After the program operation has been suspended, the system can read array data from any address. However, data read from program-suspended addresses is not valid.

The Program Suspend command may also be issued during a program operation while an erase is suspended. In this case, data may be read from any addresses not in erase suspend or program suspend. If a read is needed from the extended memory block area (one-time program area), the user must use the proper command sequences to enter and exit this region.

The system may also issue the Auto Select command sequence when the device is in the program suspend mode. The system can read as many auto select codes as required. When the device exits the auto select mode, the device reverts to the program suspend mode, and is ready for another valid operation. See Auto Select command sequence for more information.

If the program suspend operation is aborted by performing a reset or powering down the device, data integrity cannot be ensured, and it is recommended to program again the words or bytes aborted.

6.1.10 Program Resume command

After the Program Resume command is issued, the device reverts to programming. The controller can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. Refer to *Figure 16: Write enable controlled program waveforms (8-bit mode)* and *Figure 17: Write enable controlled program waveforms (16-bit mode)* for details.

The system must issue a Program Resume command, to exit the program suspend mode and to continue the programming operation.

Further issuing of the Resume command is ignored. Another Program Suspend command can be written after the device has resumed programming.

Table 12. Standard commands, 8-bit mode

Command		Length	Bus operations(1)											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0										
		3	AAA	AA	555	55	X	F0						
Auto Select	Manufacturer code	3	AAA	AA	555	55	AAA	90	(2)(3)	(2)(3)				
	Device code													
	Extended memory block protection indicator													
	Block protection status													
Program(4)		4	AAA	AA	555	55	AAA	A0	PA	PD				
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Block Erase		6+	AAA	AA	555	55	AAA	80	AAA	AA	555	55	BAd	30
Erase/Program Suspend		1	X	B0										
Erase/Program Resume		1	X	30										
Read CFI Query		1	AA	98										

1. X don't care, PA program address, PD program data, BAd any address in the block. All values in the table are in hexadecimal.
2. These cells represent read cycles. The other cells are write cycles.
3. The auto select addresses and data are given in *Table 6: Read electronic signature - auto select mode - programmer method (8-bit mode)*, and *Table 8: Block protection - auto select mode - programmer method (8-bit mode)*, except for A9 that is 'don't care'.
4. In unlock bypass, the first two unlock cycles are no more needed (see *Table 16: Write to buffer commands, 8-bit mode* and *Table 17: Write to buffer commands, 16-bit mode*).

Table 13. Standard commands, 16-bit mode

Command		Length	Bus operations(1)											
			1st		2nd		3rd		4th		5th		6th	
			Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Read/Reset		1	X	F0										
		3	555	AA	2AA	55	X	F0						
Auto Select	Manufacturer code	3	555	AA	2AA	55	555	90	(2)(3)	(2)(3)				
	Device code													
	Extended memory block protection indicator													
	Block protection status													
Program(4)		4	555	AA	2AA	55	555	A0	PA	PD				
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Block Erase		6+	555	AA	2AA	55	555	80	555	AA	2AA	55	BAd	30
Erase/Program Suspend		1	X	B0										
Erase/Program Resume		1	X	30										
Read CFI Query		1	55	98										

1. X don't care, PA program address, PD program data, BAd any address in the block. All values in the table are in hexadecimal.
2. These cells represent read cycles. The other cells are write cycles.
3. The auto select addresses and data are given in *Table 7: Read electronic signature - auto select mode - programmer method (16-bit mode)*, and *Table 9: Block protection - auto select mode - programmer method (16-bit mode)*, except for A9 that is 'don't care'.
4. In unlock bypass, the first two unlock cycles are no more needed (see *Table 16* and *Table 17*).

6.2 Unlock Bypass command

The Unlock Bypass command is used to place the device in unlock bypass mode. When the device enters the unlock bypass mode, the two initial unlock cycles required in the standard program command sequence are no more needed, and only two write cycles are required to program data, instead of the normal four cycles (see Note *4.* below *Table 12* and *Table 13*). This results in a faster total programming time.

Unlock Bypass command is consequently used in conjunction with the Unlock Bypass Program command to program the memory faster than with the standard program commands. When the cycle time to the device is long, considerable time saving can be made by using these commands. Three bus write operations are required to issue the Unlock Bypass command. When in unlock bypass mode, only the Unlock Bypass Program, Unlock Bypass Block Erase, Unlock Bypass Chip Erase, and Unlock Bypass Reset commands are valid:

- The Unlock Bypass Program command can be issued to program addresses within the memory.
- The Unlock Bypass Block Erase command can then be issued to erase one or more memory blocks.
- The Unlock Bypass Chip Erase command can be issued to erase the whole memory array.
- The Unlock Bypass Write to Buffer Program command can be issued to speed up programming operation.
- The Unlock Bypass Reset command can be issued to return the memory to read mode. In unlock bypass mode the memory can be read as if in read mode.

6.2.1 Unlock Bypass Program command

The Unlock Bypass Program command can be used to program one address in the memory array at a time. The command requires two bus write operations, the final write operation latches the address and data and starts the program/erase controller.

The program operation using the Unlock Bypass Program command behaves identically to the program operation using the Program command. The operation cannot be aborted, a bus read operation to the memory outputs the status register (see *Section 6.1.8: Program command* for details on the behavior).

6.2.2 Unlock Bypass Block Erase command

The Unlock Bypass Block Erase command can be used to erase one or more memory blocks at a time. The command requires two bus write operations instead of six using the standard Block Erase command. The final bus write operation latches the address of the block and starts the program/erase controller.

To erase multiple block (after the first two bus write operations have selected the first block in the list), each additional block in the list can be selected by repeating the second bus write operation using the address of the additional block.

The Unlock Bypass Block Erase command behaves in the same way as the Block Erase command: the operation cannot be aborted, and a bus read operation to the memory outputs the status register (see *Section 6.1.5: Block Erase command* command for details).

6.2.3 Unlock Bypass Chip Erase command

The Unlock Bypass Chip Erase command can be used to erase all memory blocks at a time. The command requires two bus write operations only instead of six using the standard Chip Erase command. The final bus write operation starts the program/erase controller. The Unlock Bypass Chip Erase command behaves in the same way as the Chip Erase command: the operation cannot be aborted, and a bus read operation to the memory outputs the status register (see *Section 6.1.4: Chip Erase command* command for details).

6.2.4 Unlock Bypass Write to Buffer Program command

The Unlock Bypass Write to Buffer command can be used to program the memory in fast program mode (see *Section 6.3.1: Write to Buffer Program command set* set for details). The command requires two bus write operations less than the standard Write to Buffer Program command.

The Unlock Bypass Write to Buffer Program command behaves in the same way as the Write to Buffer Program command: the operation cannot be aborted and a bus read operation to the memory outputs the status register.

The Write to Buffer Program Confirm command is used to confirm an Unlock Bypass Write to Buffer Program command and to program the N+1 words/bytes loaded in the write buffer by this command.

6.2.5 Unlock Bypass Reset command

The Unlock Bypass Reset command can be used to return to read/reset mode from unlock bypass mode. Two bus write operations are required to issue the Unlock Bypass Reset command. Read/Reset command does not exit from unlock bypass mode.

Table 14. Unlock Bypass commands, 8-bit mode

Command	Length	Bus write operations(1)					
		1st		2nd		3rd	
		Add	Data	Add	Data	Add	Data
Unlock Bypass	3	AAA	AA	555	55	AAA	20
Unlock Bypass Program	2	X	A0	PA	PD		
Unlock Bypass Block Erase	2+	X	80	BAd	30		
Unlock Bypass Chip Erase	2	X	80	X	10		
Unlock Bypass Reset	2	X	90	X	0		

1. X don't care PA program address, PD program data, BAd any address in the block, WBL write buffer location. All values in the table are in hexadecimal.

Table 15. Unlock Bypass commands, 16-bit mode

Command	Length	Bus write operations[1]					
		1st		2nd		3rd	
		Add	Data	Add	Data	Add	Data
Unlock Bypass	3	555	AA	2AA	55	555	20
Unlock Bypass Program	2	X	A0	PA	PD		
Unlock Bypass Block Erase	2+	X	80	BAd	30		
Unlock Bypass Chip Erase	2	X	80	X	10		
Unlock Bypass Reset	2	X	90	X	0		

1. X don't care, PA program address, PD program data, BAd any address in the block, WBL write buffer location. All values in the table are in hexadecimal.

6.3 Fast program commands

The M29W256GH/L offers a set of fast program commands to improve the programming throughput:

- Write to Buffer Program
- Enhanced Buffered Program (valid in x 16 mode only)

See either *Table 16*, *Table 17* or *Table 18* depending on the configuration that is being used, for a summary of the fast program commands.

After programming has started, bus read operations in the memory output the status register content. Write to Buffer Program command can be suspended and then resumed by issuing a Program Suspend command and a Program Resume command, respectively (see *Section 6.1.9: Program Suspend command* and *Section 6.1.10: Program Resume command*).

6.3.1 Write to Buffer Program command set

The Write to Buffer Program command set makes use of the device's 32-word/64-byte write buffer to speed up programming. 32 words/64 bytes can be loaded into the write buffer.

Each write buffer has the same A23-A5 addresses. The Write to Buffer Program command dramatically reduces system programming time compared to the standard non-buffered Program command. When issuing a Write to Buffer Program command, the VPP/WP pin can be either held High, VIH, or raised to VPPH.

See *Table 16*, *Table 17* or *Table 18* for details on typical write to buffer program times in both cases.

Write to Buffer Program command

Five successive steps are required to issue the Write to Buffer Program command:

1. The Write to Buffer Program command starts with two unlock cycles
2. The third bus write cycle sets up the Write to Buffer Program command. The setup code can be addressed to any location within the targeted block.
3. The fourth bus write cycle sets up the number of words/bytes to be programmed. Value N is written to the same block address, where N+1 is the number of words/bytes to be programmed. N+1 must not exceed the size of the write buffer or the operation will abort.
4. The fifth cycle loads the first address and data to be programmed.
5. Use N bus write cycles to load the address and data for each word/byte into the write buffer. Addresses must lie within the range from the start address+1 to the start address +N-1. Optimum performance is obtained when the start address corresponds to a 32-word/ 64-byte boundary. If the start address is not aligned to a 32-word/64-byte boundary, the total programming time is doubled.

All the addresses used in the write to buffer program operation must lie within the same page.

To program the content of the write buffer, this command must be followed by a Write to Buffer Program Confirm command.

If an address is written several times during a write to buffer program operation, the address/data counter will be decremented at each data load operation and the data will be programmed to the last word loaded into the buffer.

Invalid address combinations or failing to follow the correct sequence of bus write cycles will abort the write to buffer program.

The status register bits DQ1, DQ5, DQ6, DQ7 can be used to monitor the device status during a write to buffer program operation.

It is possible to detect program operation fails when changing programmed data from '0' to '1', that is when reprogramming data in a portion of memory already programmed. The resulting data will be the logical OR between the previous value and the current value.

After the write to buffer program operation has completed, the memory will return to read mode, unless an error has occurred. When an error occurring bus read operations to the memory will continue to output the status register.

Table 16. Write to buffer commands, 8-bit mode

Command	Length	Bus write operations(1)											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	AAA	AA	555	55	BAd	25	BAd	N(2)	PA (3)	PD	WBL (4)	PD
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N(2)	PA (3)	PD	WBL (6)	PD				
Write to Buffer Program Confirm	1	BAd (5)	29										
Buffered Program Abort Reset	3	AAA	AA	555	55	AAA	F0						

1. X don't care, PA program address, PD program data, BAd any address in the block, WBL write buffer location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 68. N+1 is the number of bytes to be programmed during the write to buffer program operation.
3. Each buffer has the same A23-A5 addresses. A0-A4 and A-1 are used to select a byte within the N+1 byte page.
4. The 6th cycle has to be issued N time. WBL scans the word inside the page.
5. BAd must be identical to the address loaded during the write to buffer program 3rd and 4th cycles.
6. The 4th cycle has to be issued N time. WBL scans the word inside the page.

Table 17. Write to buffer commands, 16-bit mode

Command	Length	Bus write operations(1)											
		1st		2nd		3rd		4th		5th		6th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Write to Buffer Program	N+5	555	AA	2AA	55	BAd	25	BAd	N(2)	PA (3)	PD	WBL (4)	PD
Unlock Bypass Write to Buffer Program	N+3	BAd	25	BAd	N(2)	PA (3)	PD	WBL (6)	PD				
Write to Buffer Program Confirm	1	BAd (5)	29										
Buffered Program Abort Reset	3	555	AA	2AA	55	555	F0						

1. X don't care, PA program address, PD program data, BAd any address in the block, WBL write buffer location. All values in the table are in hexadecimal.
2. The maximum number of cycles in the command sequence is 36. N+1 is the number of words to be programmed during the write to buffer program operation.
3. Each buffer has the same A23-A5 addresses. A0-A4 are used to select a word within the N+1 word page.
4. The 6th cycle has to be issued N time. WBL scans the word inside the page.
5. BAd must be identical to the address loaded during the write to buffer program 3rd and 4th cycles.
6. The 4th cycle has to be issued N time. WBL scans the word inside the page.

Buffered Program Abort Reset command

A Buffered Program Abort Reset command must be issued to reset the error condition and return to read mode. One of the erase commands must be used to set all the bits in a block or in the whole memory from '0' to '1'.

The write to buffer programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the number of locations to program step in the Write to Buffer Program command.
- Write to an address in a block different than the one specified during the write-buffer load command.
- Write an address/data pair to a different write-buffer-page than the one selected by the starting address during the write buffer data loading stage of the operation.
- Write data other than the Confirm command after the specified number of data load cycles.
- Load address/data pairs in an incorrect sequence during the enhanced buffered program.

The abort condition is indicated by DQ1 = 1, DQ6 = toggle, and DQ5 = 0 (all of which are status register bits). A Buffered Program Abort and Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Buffered Program Abort and Reset command sequence is required when using write to buffer and enhanced buffered programming features in unlock bypass mode.

See *Appendix D*, *Figure 29: Write to buffer program flowchart and pseudocode*, for a suggested flowchart on using the Write to Buffer Program command.

6.3.2 Enhanced Buffered Program command set

The Enhanced Buffered Program command set is available only in x 16 mode.

Enhanced Buffered Entry command

Enhanced Buffered Entry command is used in order to allow the execution of the Enhanced Buffered Program. Once issued the Enhanced Buffered Entry Command, it is possible to execute Enhanced Buffered Program Command more then one time; there is no need to repeat it again.

After an Enhanced Buffered Entry Command only the commands belonging to the Enhanced Buffered Program command set are accepted. Enhanced Buffered Program command set is listed below:

- Enhanced Buffered Program command
- Enhanced Buffered Program Abort Reset
- Enhanced Buffered Program Exit

After these commands any other command is ignored.

In order to be sure that the Entry procedure has successfully completed and the device is ready to receive one of the commands listed above it is recommended to monitor toggle bit (DQ6), see *Figure 9: Data toggle flowchart*.

Enhanced Buffered Exit command

The Enhanced Buffered Exit command is used to return the device to read mode; before this command any other command, except the Enhanced Buffered Program command set, is ignored. Two bus write operations are required to issue the command.

Enhanced Buffered Program command

The Enhanced Buffered Program command, available only in x 16 mode, makes use of the device's 256-word write buffer to speed up programming. 256 words can be loaded into the write buffer. Each write buffer has the same A23-A8 addresses. The Enhanced Buffered Program command dramatically reduces system programming time compared to both the standard non-buffered Program command and the Write to Buffer command.

When issuing an Enhanced Buffered Program command, the VPP/WP pin can be either held High, VIH, or raised to VPPH (see *Table 21: Program/erase times and program/erase endurance cycles* for details on typical enhanced buffered program times in both cases).

- Enhanced Buffered Program command is accepted only after Enhanced Buffered Entry command.
- Only one bus write cycle is needed to set up the Enhanced Buffered Program command. The setup code can be addressed to any location within the targeted block.
- The second bus write cycle loads the first address and data to be programmed. There a total of 256 address and data loading cycles.
- Once the 256 words are loaded to the buffer a further bus write is needed to program the content of the write buffer.
- Once Enhanced Buffered Program is completed Enhanced Buffered Exit command is required to return to read mode.

(See *Table 18: Enhanced buffered program commands, 16-bit mode* for more details);

Note that address/data cycles must be loaded in an increasing address order (from ADD[7:0]=00000000 to ADD[7:0]=11111111) and completely (all 256 words). Invalid address combinations or failing to follow the correct sequence of bus write cycles will abort the enhanced buffered program.

The status register bits DQ1, DQ5, DQ6, and DQ7 can be used to monitor the device status during an enhanced buffered program operation.

An external supply (12 V) can be used to improve programming efficiency.

It is possible to detect program operation fails when changing programmed data from '0' to '1', that is when reprogramming data in a portion of memory already programmed. The resulting data will be the logical OR between the previous and the current value.

See *Appendix D* and *Figure 30: Enhanced buffered program flowchart and pseudocode*, for a suggested flowchart on using the Enhanced Buffered Program command.

Enhanced Buffered Program Abort Reset command

After an enhanced buffered program abort the memory does not accept any other command; in order to reset the device from the abort must be issued an Enhanced Buffered Program Abort Reset. After the Enhanced Buffered Program Abort Reset command the memory waits for one of the Enhanced Buffered Program command set.

The enhanced buffered programming sequence can be aborted in the following ways:

- Write to an address in a block different than the one specified during the buffer load.
- Write an address/data pair to a different buffer-page than the one selected by the starting address during the buffer data loading stage of the operation
- Write data other than the Confirm command after the 256 data load cycles.
- Load address/data pairs in an incorrect sequence during the enhanced buffered program.
- Load a number of data that is less or greater than 256 during the program step.

Table 18. Enhanced buffered program commands, 16-bit mode

Command	Length	Bus write operations													
		1st		2nd		3rd		...		256th		257th		258th	
		Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data	Add	Data
Enter Enhanced Buffered Program Command Set	3	555	AA	2AA	55	555	38								
Enhanced Buffered Program	258	BAd	33	BAd (00)	Data	BAd (01)	Data	...	...	BAd (FE)	Data	BAd (FF)	Data	BAd (00)	29
Exit Enhanced Buffered Program Command Set	2	X	90	X	00										
Enhanced Buffered Program Abort Reset	3	555	AA	2AA	55	555	F0								

The abort condition is indicated by DQ1 = 1, DQ6 = toggle, and DQ5 = 0 (all of which are status register bits).

Note: Enhanced Buffered Program commands are available for x 16 mode only.

6.4 Protection commands

Blocks can be protected individually against accidental program, erase or read operations. The device block protection scheme is shown in *Figure 5: Software protection scheme*. See either *Table 19*, or *Table 20*, depending on the configuration that is being used, for a summary of the block protection commands.

Block protection commands are available both in 8-bit and 16-bit configuration.

The memory block and extended memory block protection is configured through the lock register (see *Section 5.4: Lock register*).

The program commands referred to in the following sections must be used according to all the Program command timings listed here:

- *Figure 16.: Write enable controlled program waveforms (8-bit mode)*,
- *Figure 17.: Write enable controlled program waveforms (16-bit mode)*,
- *Figure 18.: Chip enable controlled program waveforms (8-bit mode)*,
- *Figure 19.: Chip enable controlled program waveforms (16-bit mode)*.

6.4.1 Lock Register Command Set

The M29W256GL and M29W256GH offer a set of commands to access the lock register and to configure and verify its content. See the following sections in conjunction with *Section 5.4: Lock register*, *Table 19* and *Table 20*.

Enter Lock Register Command Set command

Three bus write cycles are required to issue the Enter Lock Register Command Set command. Once the command has been issued, all bus read or program operations are issued to the lock register.

An Exit Protection Command Set command must then be issued to return the device to read mode (see *Section 6.4.7: Exit Protection Command Set command*).

Lock Register Program and Lock Register Read command

The Lock Register Program command allows to configure the lock register. The programmed data can then be checked by issuing a Lock Register Read command.

6.4.2 Extended Memory Block

The M29W256GH/L has one extra 128-word block (extended memory block). that can only be accessed using the Enter Extended Memory Block command.

The extended memory block cannot be erased, and is one-time programmable (OTP) memory.

In extended block mode, Erase, Chip Erase, Erase Suspend and Erase Resume commands are not allowed.

To exit from the extended memory block mode the Exit Extended Memory Block command must be issued.

The device remains in extended memory block mode until the Exit Extended Memory Block command is issued or power is removed from the device. After power-up or an hardware reset, the device reverts to read mode, and the commands issued to block 0 addresses will properly address block 0.

The extended memory block can be protected by setting the extended memory block protection bit to '0' (see *Section 5.4: Lock register*); however once protected the protection cannot be undone.

Note: When the device is in the extended memory block mode, the VPP/WP pin cannot be used for fast programming and the unlock bypass mode is not available (see Section 2.8: VPP/write protect (VPP/WP)).

Enter Extended Memory Block command

The M29W256GH/L has one extra 128-word block (extended memory block) that can only be accessed using the Enter Extended Memory Block command.

Three bus write cycles are required to issue the Extended Memory Block command. Once the command has been issued the device enters the extended memory block mode where all bus read or program operations are conducted on the extended memory block. Once the device is in the extended block mode, the extended memory block is addressed by using the addresses occupied by block 0 in the other operating modes (see *Table 37: Block addresses 0 - 127*).

The device remains in extended memory block mode until the Exit Extended Memory Block command is issued or power is removed from the device. After power-up or a hardware reset, the device reverts to read mode, and the commands issued to block 0 addresses will properly address block 0.

The extended memory block cannot be erased, and can be treated as one-time programmable (OTP) memory.

In extended block mode, Erase, Chip Erase, Erase Suspend and Erase Resume commands are not allowed.

To exit from the extended memory block mode the Exit Extended Memory Block command must be issued.

The extended memory block can be protected by setting the extended memory block protection bit to ‘1’ (see *Section 5.4: Lock register*); however once protected the protection cannot be undone.

Note: When the device is in the extended memory block mode, the $V_{PP}/\overline{WP}$ pin cannot be used for fast programming and the unlock bypass mode is not available (see Section 2.8: VPP/write protect (VPP/WP)).

Exit Extended Memory Block command

The Exit Extended Memory Block command is used to exit from the extended memory block mode and return the device to read mode. Four bus write operations are required to issue the command.

6.4.3 Volatile protection mode command set

Enter Volatile Protection Command Set command

Three bus write cycles are required to issue the Enter Volatile Protection Command Set command. Once the command has been issued, only the commands related to the volatile protection mode and the Exit Protection Command Set can be issued to the device.

Volatile Protection Bit Program command (VPB Program)

The VPB Program command individually sets a VPB to ‘0’ for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit. (see *Table 11: Block protection status*).

Read VPB Status command

The status of a VPB for a given block can be read by issuing a Read VPB Status command along with the block address.

VPB Clear command

The VPB Clear command individually clears (sets to ‘1’) the VPB for a given block.

If the NVPB for the same block is set, the block is locked regardless of the value of the VPB bit (see *Table 11: Block protection status*).

6.4.4 Non-volatile protection mode command set

Enter Non-volatile Protection Command Set command

Three bus write cycles are required to issue the Enter Non-volatile Protection Command Set command. Once the command has been issued, only the commands related to the non-volatile protection mode and the Exit Protection Command Set can be issued to the device.

Non-volatile Protection Bit Program command (NVPB Program)

A block can be protected from program or erase by issuing a Non-volatile Protection Bit command along with the block address. This command sets the NVPB to ‘0’ for a given block.

The Non-volatile Bit Program command is a special kind of Program command and must be used according to all the Program command timings. The result from this command can be verified by checking the status register.

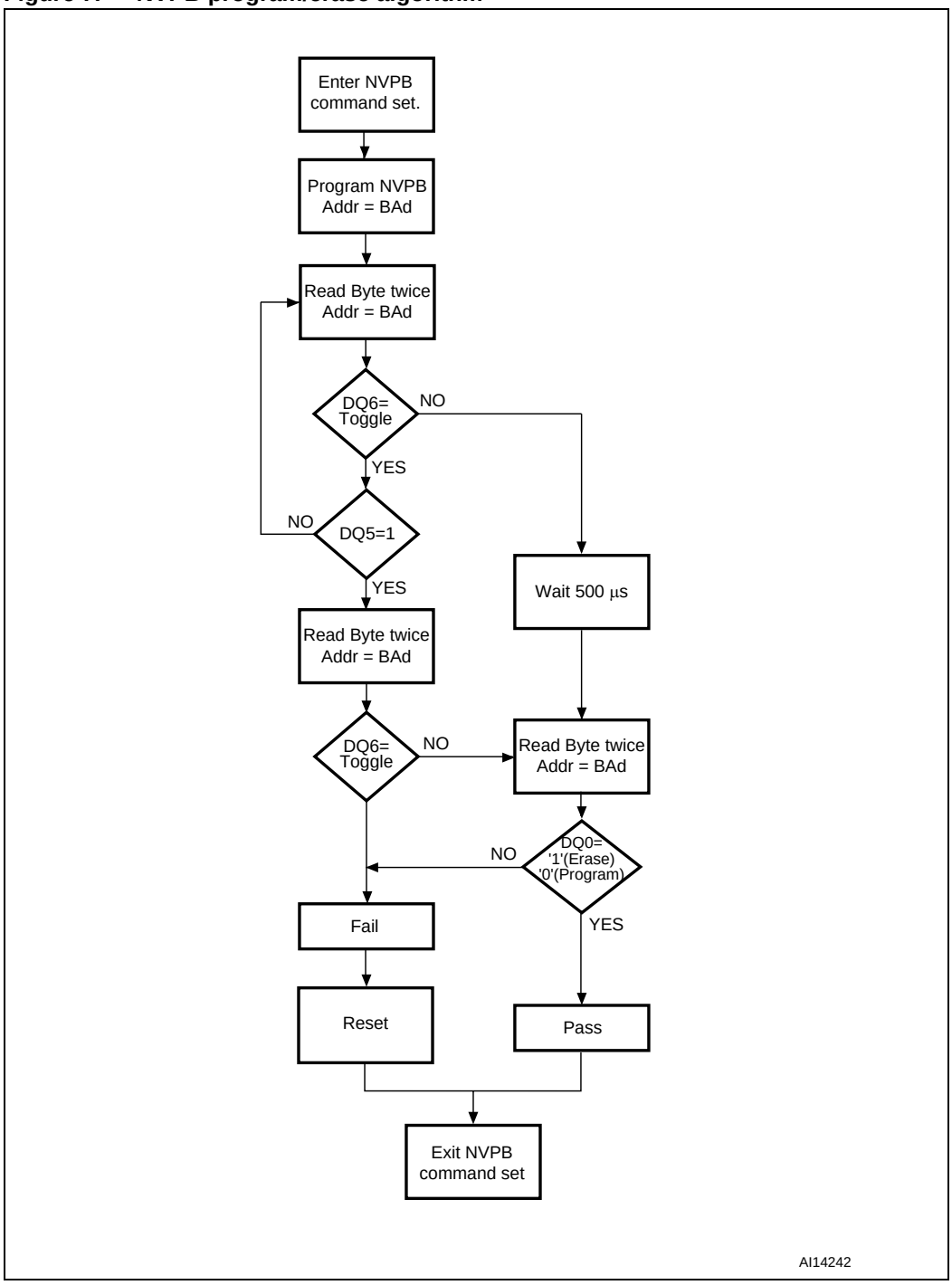
Read Non-volatile Protection Bit Status command (Read NVPB Status)

The status of a NVPB for a given block or group of blocks can be read by issuing a Read Non-Volatile Modify Protection Bit command along with the block address.

Clear all Non-volatile Protection Bits command (Clear all NVPBs)

The NVPBs are erased simultaneously by issuing a Clear all Non-volatile Protection Bits command. No specific block address is required. If the NVPB lock bit is set to ‘0’, the command fails.

Figure 7. NVPB program/erase algorithm



6.4.5 NVPB lock bit command set

Enter NVPB Lock Bit Command Set command

Three bus write cycles are required to issue the Enter NVPB Lock Bit Command Set command. Once the command has been issued, the only commands allowing to set the NVPB lock bit and the Exit Protection Command Set can be issued to the device. Any other command is ignored. See *Section 5.2.2: Non-volatile protection bit lock bit*.

NVPB Lock Bit Program command

This command is used to set the NVPB lock bit to ‘0’ thus locking the NVPBs, and preventing them from being modified.

Read NVPB Lock Bit Status command

This command is used to read the status of the NVPB lock bit.

6.4.6 Password protection mode command set

The device accepts the commands belonging to the Password protection mode commands set if and only if the Password protection mode lock bit (DQ2) has been set to '0', (see section *Section 5.4.3: Password protection mode lock bit (DQ2)*) otherwise the password commands are ignored.

Enter Password Protection Command Set command

Three bus write cycles are required to issue the Enter Password Protection Command Set command. Once the command has been issued, only the commands related to the password protection mode and the Exit Protection Command Set can be issued to the device. Any other command is ignored.

Password Program command

The Password Program command is used to program the 64-bit password used in the password protection mode.

To program the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A1-A0 plus DQ15A-1 in 8-bit mode, or four times at four consecutive addresses selected by A1-A0 in 16-bit mode. The Password Program command is a special kind of Program command and must be used according to all the Program command timings. The result from this command can be verified by checking the status register.

The password can be checked by issuing a Password Read command.

Once password program operation has completed, an Exit Protection Command Set command must be issued to return the device to read mode. The password protection mode can then be selected.

By default, all password bits are set to ‘1’.

Password Read command

The Password Read command is used to verify the password used in password protection mode.

To verify the 64-bit password, the complete command sequence must be entered eight times at eight consecutive addresses selected by A1-A0 plus DQ15A-1 in 8-bit mode, or four times at four consecutive addresses selected by A1-A0 in 16-bit mode.

If the password mode lock bit is programmed and the user attempts to read the password, the device will output FFh onto the I/O data bus.

An Exit Protection Command Set command must be issued to return the device to read mode.

Password Unlock command

The Password Unlock command is used to clear the NVPB lock bit allowing to modify the NVPBs.

The Password Unlock command must be issued along with the correct password.

There must be a 1 µs delay between successive password unlock commands in order to prevent hackers from cracking the password by trying all possible 64-bit combinations. If this delay is not respected, the latest command will be ignored.

Approximately 1 µs is required for unlocking the device after the valid 64-bit password has been provided.

6.4.7 Exit Protection Command Set command

The Exit Protection Command Set command is used to exit from the lock register, password protection, non-volatile protection, volatile protection, and NVPB lock bit command set mode. It returns the device to read mode.

Table 19. Block protection commands, 8-bit mode(1)(2)(3)

	Command	Length	Bus operations																					
			1st		2nd		3rd		4th		5th		6th		7th		8th		9th		10th		11th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock Register	Enter Lock Register Command Set(4)	3	AAA	AA	555	55	AAA	40																
	Lock Register Program	2	X	A0	X	DATA (5)																		
	Lock Register Read	1	X	DATA (5)																				
Volatile Protection	Enter Volatile Protection Command Set	3	AAA	AA	555	55	AAA	E0																
	VPB Program(8)	2	X	A0	BAd	00																		
	Read VPB Status	1	X	RD(0)																				
	VPB Clear(8)	2	X	A0	BAd	01																		
Non-volatile Protection	Enter Non-Volatile Protection Command Set(4)	3	AAA	AA	555	55	AAA	C0																
	NVPB Program(6)	2	X	A0	BAd	00																		
	Clear all NVPBs(7)	2	X	80	00	30																		
	Read NVPB Status (8)	1	BAd	RD(0)																				
NVPB Lock bit	Enter NVPB Lock Bit Command Set	3	AAA	AA	555	55	AAA	50																
	NVPB Lock Bit Program(8)	2	X	A0	X	00																		
	Read NVPB Lock Bit Status (8)	1	X	RD(0)																				
Password Protection	Enter Password Protection Command Set(4)	3	AAA	AA	555	55	AAA	60																
	Password Program (8)(9)	2	X	A0	PWAn	PWDn																		
	Password Read	8	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6	07	PWD7						
	Password Unlock(7)	11	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6	07	PWD7	00	29
	Exit Protection Command Set (10)	2	X	90	X	00																		
	Enter Extended Block(4)	3	AAA	AA	555	55	AAA	88																
	Exit Extended Block	4	AAA	AA	555	55	AAA	90	X	00														

1. Ad address, Dat data, BAd any address in the block, RD read data, PWDn password byte 0 to 7, PWAn password address (n = 0 to 7), X don't care. All values in the table are in hexadecimal.
2. Grey cells represent read cycles. The other cells are Write cycles.
3. DQ15 to DQ8 are 'don't care' during unlock and command cycles. A23 to A16 are 'don't care' during unlock and command cycles unless an address is required.
4. An Enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = lock register content.
6. Protected and unprotected states correspond to 00 and 01, respectively.
7. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared non volatile modify protection bits.
8. Only one portion of password can be programmed or read by each Password Program command.
9. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to read mode.

Table 20. Block protection commands, 16-bit mode(1)(2)(3)

Command		Length	Bus operations													
			1st		2nd		3rd		4th		5th		6th		7th	
			Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data	Ad	Data
Lock register	Enter Lock Register Command Set(4)	3	555	AA	2AA	55	555	40								
	Lock Register Program	2	X	A0	X	DATA (5)										
	Lock Register Read	1	X	DATA (5)												
Volatile Protection	Enter Volatile Protection Command Set	3	555	AA	2AA	55	555	E0								
	VPB Program	2	X	A0	BAd	00										
	Read VPB Status	1	X	RD(0)												
	VPB Clear	2	X	A0	BAd	01										
Non-Volatile Protection	Enter Non-volatile Protection Command Set(4)	3	555	AA	2AA	55	555	C0								
	NVPB Program(6)	2	X	A0	BAd	00										
	Clear all NVPBs(7)	2	X	80	00	30										
	Read NVPB Status	1	BAd	RD(0)												
NVPB Lock bit	Enter NVPB Lock Bit Command Set	3	555	AA	2AA	55	555	50								
	NVPB Lock Bit Program	2	X	A0	X	00										
	Read NVPB Lock Bit Status	1	X	RD(0)												
Password Protection	Enter Password Protection Command Set(4)	3	555	AA	2AA	55	555	60								
	Password Program (8)(9)	2	X	A0	PWAn	PWDn										
	Password Read	4	00	PWD0	01	PWD1	02	PWD2	03	PWD3						
	Password Unlock(7)	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
Exit Protection Command Set(10)		2	X	90	X	00										
Enter Extended Block(4)		3	555	AA	2AA	55	555	88								
Exit Extended Block		4	555	AA	2AA	55	555	90	X	00						

1. Ad address, Dat data, BAd any address in the block, RD read data, PWDn password word 0 to 3, PWAn password address (n = 0 to 3), X don't care. All values in the table are in hexadecimal.
2. Grey cells represent read cycles. The other cells are write cycles.
3. DQ15 to DQ8 are 'don't care' during unlock and command cycles. A23 to A16 are 'don't care' during unlock and command cycles unless an address is required.
4. An Enter command sequence must be issued prior to any operation. It disables read and write operations from and to block 0. Read and write operations from any other block are allowed.
5. DATA = lock register content.
6. Protected and unprotected states correspond to 00 and 01, respectively.
7. The Clear all NVPBs command programs all NVPBs before erasure in order to prevent the over-erasure of previously cleared non-volatile modify protection bits.
8. Only one portion of password can be programmed or read by each Password Program command.
9. The password portion can be entered or read in any order as long as the entire 64-bit password is entered or read.
10. If an Entry Command Set command is issued, an Exit Protection Command Set command must be issued to return the device to read mode.

Table 21. Program/erase times and program/erase endurance cycles

Parameter			Min	Typ (1) (2)	Max (2)	Unit
Chip Erase				145 (3)	400 (4)	s
Chip Erase		$V_{PP}/\overline{WP} = V_{PPH}$		125	400 (4)	s
Block Erase (128 kbytes) (4) (5)				0.5	2	s
Erase Suspend latency time				25	45	µs
Block Erase timeout			50			µs
Byte Program	Single Byte Program			16	200 (4)	µs
	Write to Buffer Program (64 bytes at-a-time)	$V_{PP}/\overline{WP} = V_{PPH}$		50		µs
		$V_{PP}/\overline{WP} = V_{IH}$		70		
Word Program	Single Word Program			16	200 (4)	µs
	Write to Buffer Program (32 words at-a-time)	$V_{PP}/\overline{WP} = V_{PPH}$		50		µs
		$V_{PP}/\overline{WP} = V_{IH}$		70		
Chip Program (byte by byte)				540	800 (4)	s
Chip Program (word by word)				270	400 (4)	s
Chip Program (Write to Buffer Program) (6)				25	200 (4)	s
Chip Program (Write to Buffer Program with $V_{PP}/\overline{WP} = V_{PPH}$) (6)				13	50 (4)	s
Chip Program (Enhanced Buffered Program) (6)				15	60	s
Chip Program (Enhanced Buffered Program with $V_{PP}/\overline{WP} = V_{PP}$) (6)				10	40	s
Program Suspend latency time				5	15	µs
Program/Erase cycles (per block)			100,000			Cycles
Data retention			20			Years

1. Typical values measured at room temperature and nominal voltages and for not cycled devices.
2. Sampled, but not 100% tested.
3. Time needed to program the whole array at 0 is included.
4. Maximum value measured at worst case conditions for both temperature and V_{CC} after 100,000 program/erase cycles.
5. Block erase polling cycle time (see *Figure 24: Data polling AC waveforms*).
6. Intrinsic program timing, that means without the time required to execute the bus cycles to load the program commands.

7 Status register

The M29W256GH/L has one status register. The various bits convey information and errors on the current and previous program/erase operation. Bus read operations from any address within the memory, always read the status register during program and erase operations. It is also read during erase suspend when an address within a block being erased is accessed.

The bits in the status register are summarized in *Table 22: Status register bits*.

7.1 Data polling bit (DQ7)

The data polling bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an erase suspend. The data polling bit is output on DQ7 when the status register is read.

During program operations the data polling bit outputs the complement of the bit being programmed to DQ7. After successful completion of the program operation the memory returns to read mode and bus read operations, from the address just programmed, output DQ7, not its complement.

During erase operations the data polling bit outputs ’0’, the complement of the erased state of DQ7. After successful completion of the erase operation the memory returns to read mode.

In erase suspend mode the data polling bit will output a ’1’ during a bus read operation within a block being erased. The data polling bit will change from ’0’ to ’1’ when the program/erase controller has suspended the erase operation.

Figure 8: Data polling flowchart, gives an example of how to use the data polling bit. A valid address is the address being programmed or an address within the block being erased.

7.2 Toggle bit (DQ6)

The toggle bit can be used to identify whether the program/erase controller has successfully completed its operation or if it has responded to an erase suspend. The toggle bit is output on DQ6 when the status register is read.

During a program/erase operation the toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive bus read operations at any address. After successful completion of the operation the memory returns to read mode.

During erase suspend mode the toggle bit will output when addressing a cell within a block being erased. The toggle bit will stop toggling when the program/erase controller has suspended the erase operation.

Figure 9: Data toggle flowchart, gives an example of how to use the toggle bit.

7.3 Error bit (DQ5)

The error bit can be used to identify errors detected by the program/erase controller. The error bit is set to ’1’ when a program, block erase or chip erase operation fails to write the correct data to the memory. If the error bit is set a Read/Reset command must be issued before other commands are issued. The error bit is output on DQ5 when the status register is read.

Note that the Program command cannot change a bit set to ’0’ back to ’1’ and attempting to do so will set DQ5 to ‘1’. A bus read operation to that address will show the bit is still ‘0’. One of the erase commands must be used to set all the bits in a block or in the whole memory from ’0’ to ’1’.

7.4 Erase timer bit (DQ3)

The erase timer bit can be used to identify the start of program/erase controller operation during a Block Erase command. Once the program/erase controller starts erasing the erase timer bit is set to ’1’. Before the program/erase controller starts the erase timer bit is set to ’0’ and additional blocks to be erased may be written to the command interface. The erase timer bit is output on DQ3 when the status register is read.

7.5 Alternative toggle bit (DQ2)

The alternative toggle bit can be used to monitor the program/erase controller during erase operations. The alternative toggle bit is output on DQ2 when the status register is read.

During chip erase and block erase operations the toggle bit changes from ’0’ to ’1’ to ’0’, etc., with successive bus read operations from addresses within the blocks being erased. A protected block is treated the same as a block not being erased. Once the operation completes the memory returns to read mode.

During erase suspend the alternative toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive bus read operations from addresses within the blocks being erased. Bus read operations to addresses within blocks not being erased will output the memory array data as if in read mode.

After an erase operation that causes the error bit to be set, the alternative toggle bit can be used to identify which block or blocks have caused the error. The alternative toggle bit changes from ’0’ to ’1’ to ’0’, etc. with successive bus read operations from addresses within blocks that have not erased correctly. The alternative toggle bit does not change if the addressed block has erased correctly.

7.6 Buffered program abort bit (DQ1)

The buffered program abort bit, DQ1, is set to ‘1’ when a write to buffer program or enhanced buffered program operation aborts. The Buffered Program Abort Reset command must be issued to return the device to read mode (see *Buffered Program Abort Reset command* and *Enhanced Buffered Program Abort Reset command* in *Section 6.3: Fast program commands*).

Table 22. Status register bits(1)

Operation	Address	DQ7	DQ6	DQ5	DQ3	DQ2	DQ1	RB
Program	Any address	$\overline{DQ7}$	Toggle	0	–	–	0	0
Program during erase suspend	Any address	$\overline{DQ7}$	Toggle	0	–	–	–	0
Enhanced Buffered Program Entry	Any address	-	Toggle	0	-	-	-	0
Buffered program abort	Any address	$\overline{DQ7}$	Toggle	0	–	–	1	0
Program error	Any address	$\overline{DQ7}$	Toggle	1	–	–	–	Hi-Z
Chip erase	Any address	0	Toggle	0	1	Toggle	–	0
Block erase before timeout	Erasing block	0	Toggle	0	0	Toggle	–	0
	Non-erasing block	0	Toggle	0	0	No toggle	–	0
Block erase	Erasing block	0	Toggle	0	1	Toggle	–	0
	Non-erasing block	0	Toggle	0	1	No toggle	–	0
Erase suspend	Erasing block	1	No Toggle	0	–	Toggle	–	Hi-Z
	Non-erasing block	Data read as normal					–	Hi-Z
Erase error	Good block address	0	Toggle	1	1	No toggle	–	Hi-Z
	Faulty block address	0	Toggle	1	1	Toggle	–	Hi-Z

1. Unspecified data bits should be ignored.

Figure 8. Data polling flowchart

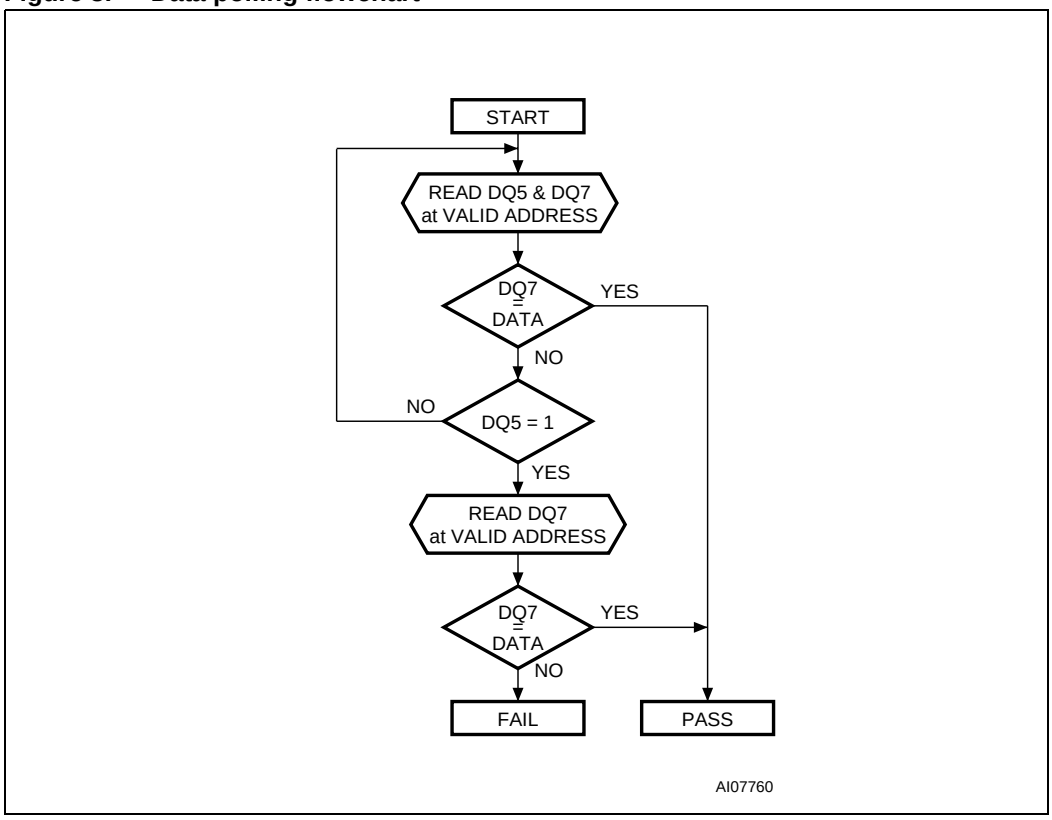
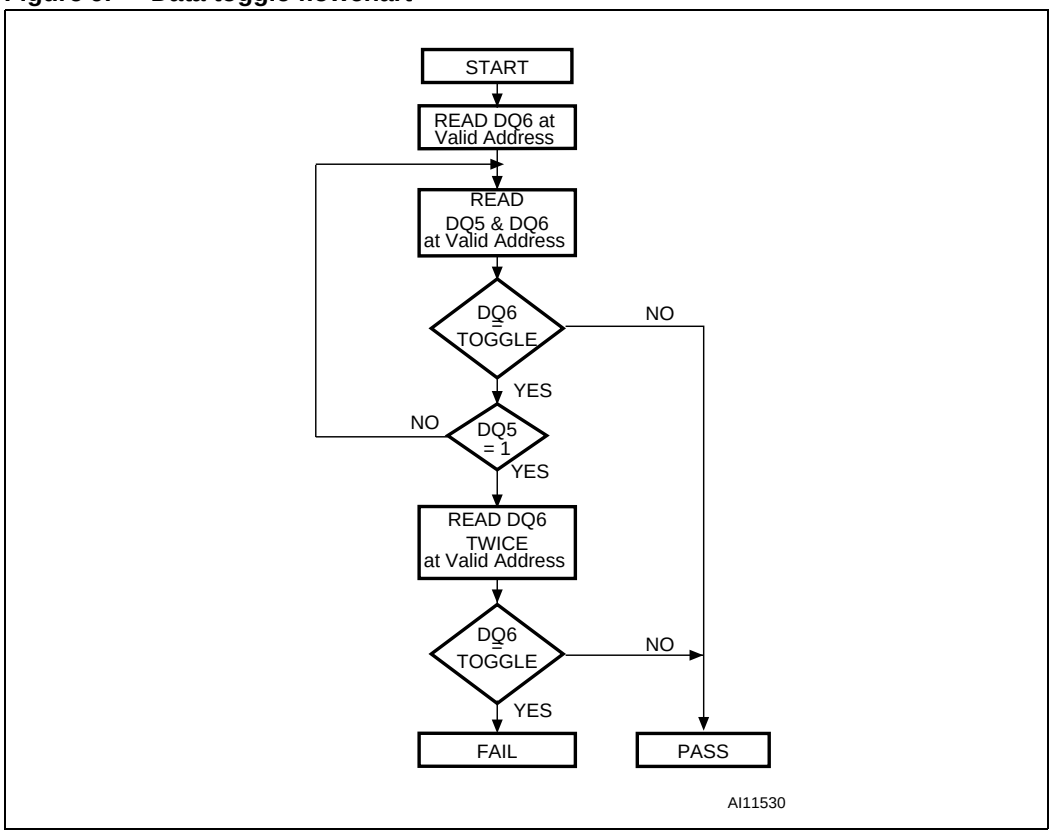


Figure 9. Data toggle flowchart



8 Maximum ratings

Stressing the device above the rating listed in *Table 23: Absolute maximum ratings* may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Table 23. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
T_{BIAS}	Temperature under bias	–50	125	°C
T_{STG}	Storage temperature	–65	150	°C
V_{IO}	Input or output voltage(1)(2)	–0.6	V_{CC} + 0.6	V
V_{CC}	Supply voltage	–0.6	4	V
V_{CCQ}	Input/output supply voltage	–0.6	4	V
V_{ID}	Identification voltage	–0.6	13.5	V
V_{PPH}(3)	Program voltage	–0.6	13.5	V

1. Minimum voltage may undershoot to –2 V during transition and for less than 20 ns during transitions.
2. Maximum voltage may overshoot to V_{CC} + 2 V during transition and for less than 20 ns during transitions.
3. V_{PPH} must not remain at 12 V for more than a total of 80 hrs.

9 DC and AC parameters

This section summarizes the operating measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 24: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the operating conditions when relying on the quoted parameters.

Table 24. Operating and AC measurement conditions

Parameter	M29W256GH, M29W256GL				Unit
	70 or 60[1] ns		80 ns		
	Min	Max	Min	Max	
V_{CC} supply voltage	2.7	3.6	2.7	3.6	V
V_{CCQ} supply voltage ($V_{CCQ} \leq V_{CC}$)	2.7	3.6	1.65	3.6	V
Ambient operating temperature (temperature range 1)	0	70	0	70	°C
Ambient operating temperature (temperature range 6)	– 40	85	– 40	85	°C
Load capacitance (C_L)	30		30		pF
Input rise and fall times		10		10	ns
Input pulse voltages	0 to V_{CCQ}		0 to V_{CCQ}		V
Input and output timing ref. voltages	$V_{CCQ}/2$		$V_{CCQ}/2$		V

1. Only available upon customer request.

Figure 10. AC measurement load circuit

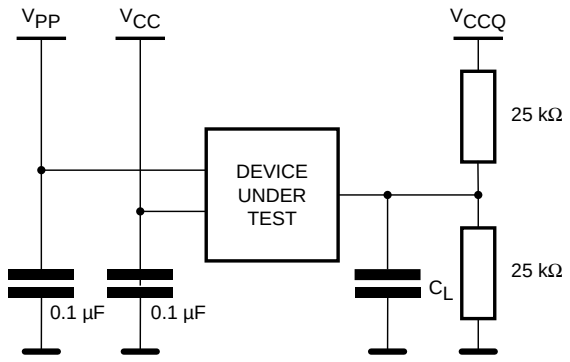


Figure 11. AC measurement I/O waveform

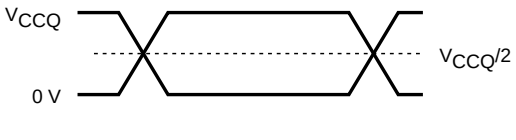


Table 25. Power-up waiting timings

Symbol	Parameter		M29W256GH, M29W256GL		Unit
			70 or 60(1) ns	80 ns	
t_{VCHEL}	V_{CC}(2) High to Chip Enable Low	Min	55		µs
t_{VCQHEL}	V_{CCQ}(2) High to Chip Enable Low	Min	55		µs
t_{VCHWL}	V_{CC} High to Write Enable Low	Min	500		µs
t_{VCQHWL}	V_{CCQ} High to Write Enable Low	Min	500		µs

1. Only available upon customer request.
2. V_{CC} and V_{CCQ} ramps must be synchronized during power-up.

Figure 12. Power-up waiting timings

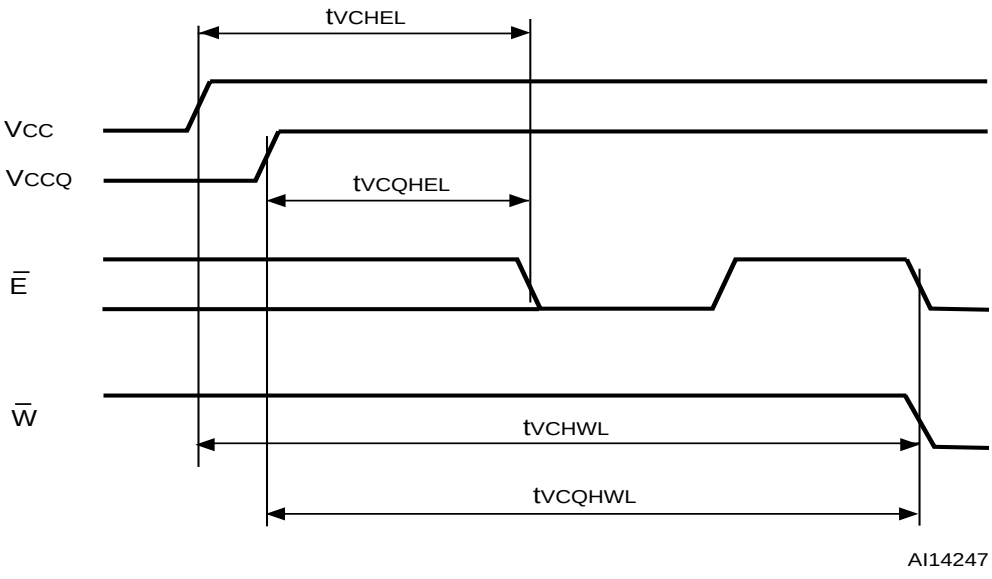


Table 26. Device capacitance(1)

Symbol	Parameter	Test condition	Min	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		6	pF
C_{OUT}	Output capacitance	V_{OUT} = 0 V		12	pF

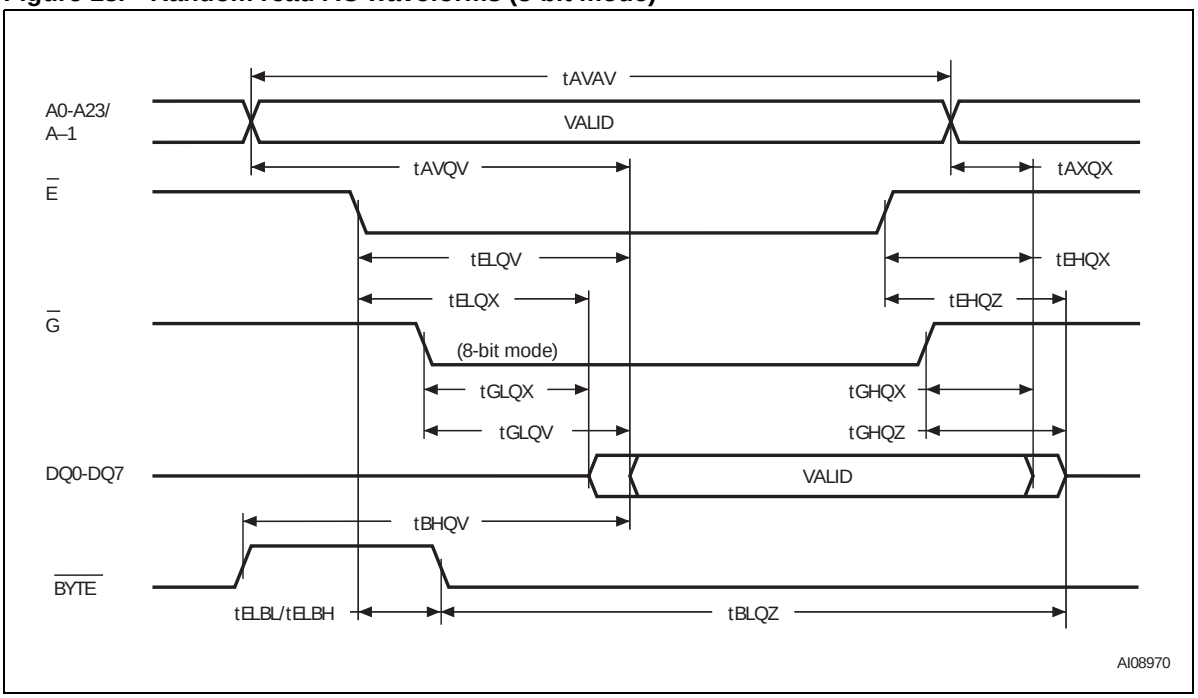
1. Sampled only, not 100% tested.

Table 27. DC characteristics

Symbol	Parameter		Test condition		Min	Typ	Max	Unit
I_{LI}(1)	Input leakage current		0 V ≤ V_{IN} ≤ V_{CC}				±1	µA
I_{LO}	Output leakage current		0 V ≤ V_{OUT} ≤ V_{CC}				±1	µA
I_{CC1}	Read current	Random read	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 6 MHz				10	mA
		Page read	$\overline{E}$ = V_{IL}, $\overline{G}$ = V_{IH}, f = 10 MHz				1	mA
I_{CC2}	Supply current (standby)		$\overline{E}$ = V_{CCQ} ± 0.2 V, $\overline{RP}$ = V_{CCQ} ± 0.2 V				100	µA
I_{CC3}(2)	Supply current (program/erase)		Program/erase controller active	$V_{PP}/\overline{WP}$ = V_{IL} or V_{IH}			20	mA
				$V_{PP}/\overline{WP}$ = V_{PPH}			15	mA
I_{PP1}	Program current (program)	Read or standby	$V_{PP}/\overline{WP}$ ≤ V_{CC}			1	5	µA
I_{PP2}		Reset	$\overline{RP}$ = V_{SS} ± 0.2 V			1	5	µA
I_{PP3}		Program operation ongoing	$V_{PP}/\overline{WP}$ = VppH ± 5%			1	10	mA
			$V_{PP}/\overline{WP}$ = V_{CC}			1	5	mA
I_{PP4}	Program current (erase)	Erase operation ongoing	$V_{PP}/\overline{WP}$ = VppH ± 5%			3	10	mA
			$V_{PP}/\overline{WP}$ = V_{CC}			1	5	mA
V_{IL}	Input Low voltage		V_{CC} ≥ 2.7 V		–0.5		0.3V_{CCQ}	V
V_{IH}	Input High voltage		V_{CC} ≥ 2.7 V		0.7V_{CCQ}		V_{CCQ}+0.4	V
V_{OL}	Output Low voltage		I_{OL} = 100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$				0.15V_{CCQ}	V
V_{OH}	Output High voltage		I_{OH} = 100 µA, V_{CC} = $V_{CC(min)}$, V_{CCQ} = $V_{CCQ(min)}$		0.85V_{CCQ}			V
V_{ID}	Identification voltage				11.5		12.5	V
V_{PPH}	Voltage for $V_{PP}/\overline{WP}$ program acceleration				11.5		12.5	V
V_{LKO}(2)	Program/erase lockout supply voltage				1.8		2.5	V

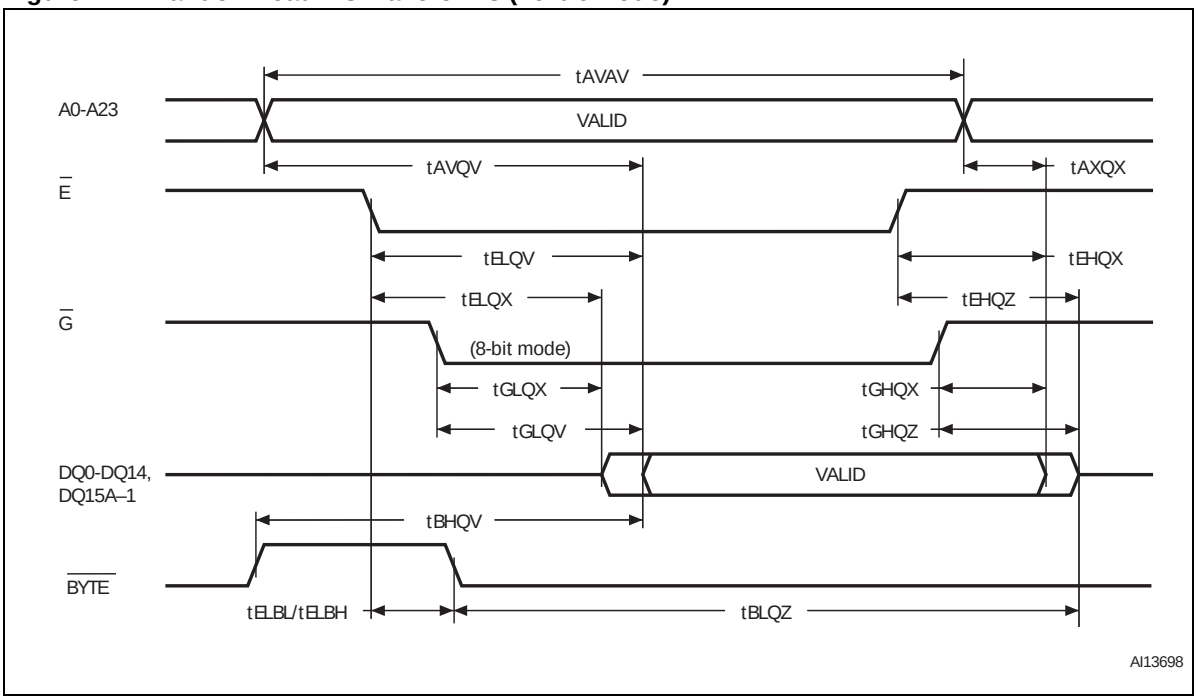
1. The maximum input leakage current is ±5 µA on the $V_{PP}/\overline{WP}$ pin.
2. Sampled only, not 100% tested.

Figure 13. Random read AC waveforms (8-bit mode)



Note: $\overline{BYTE} = V_{IL}$

Figure 14. Random read AC waveforms (16-bit mode)



Note: $\overline{BYTE} = V_{IH}$

Figure 15. Page read AC waveforms (16-bit mode)

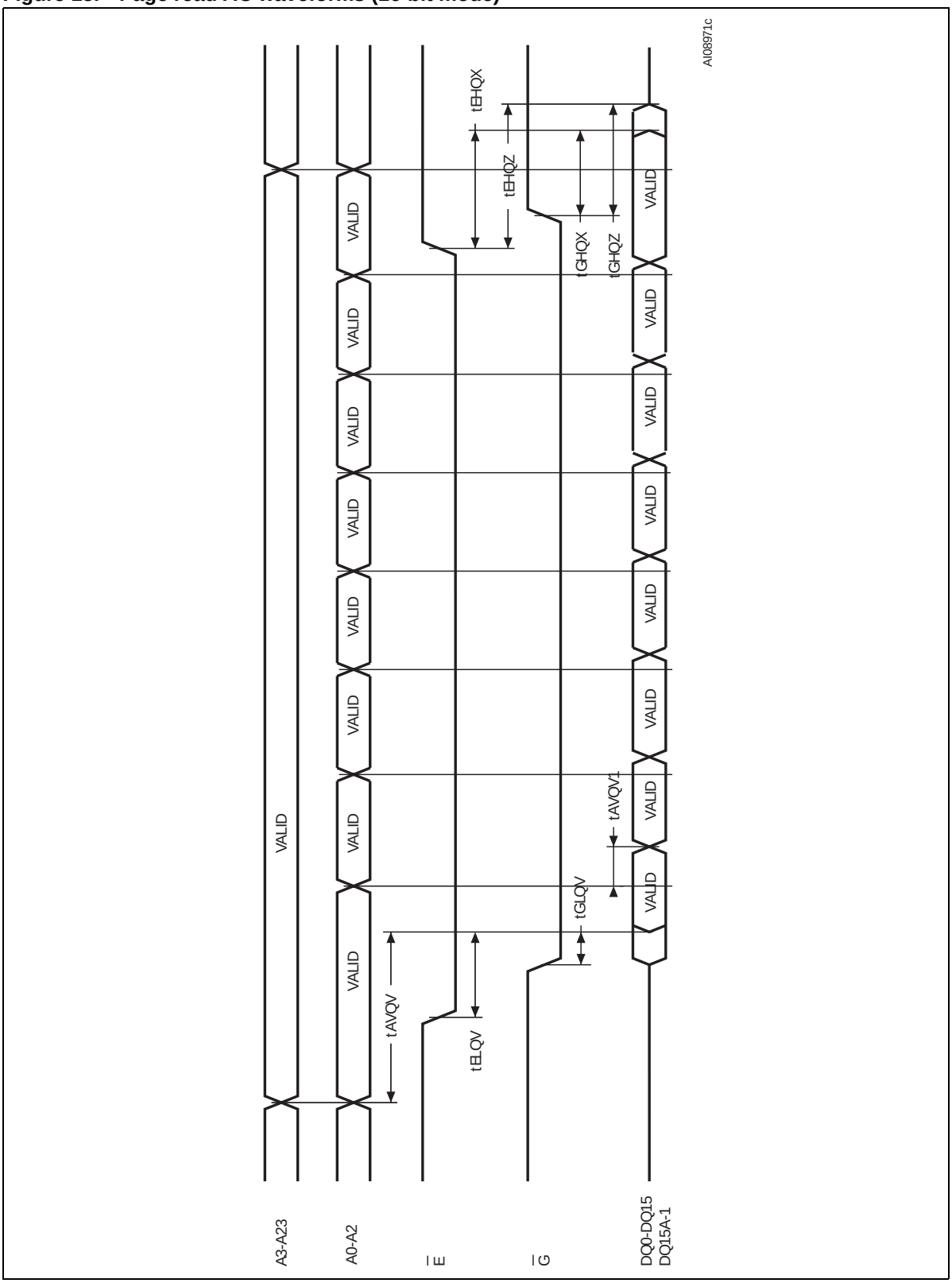
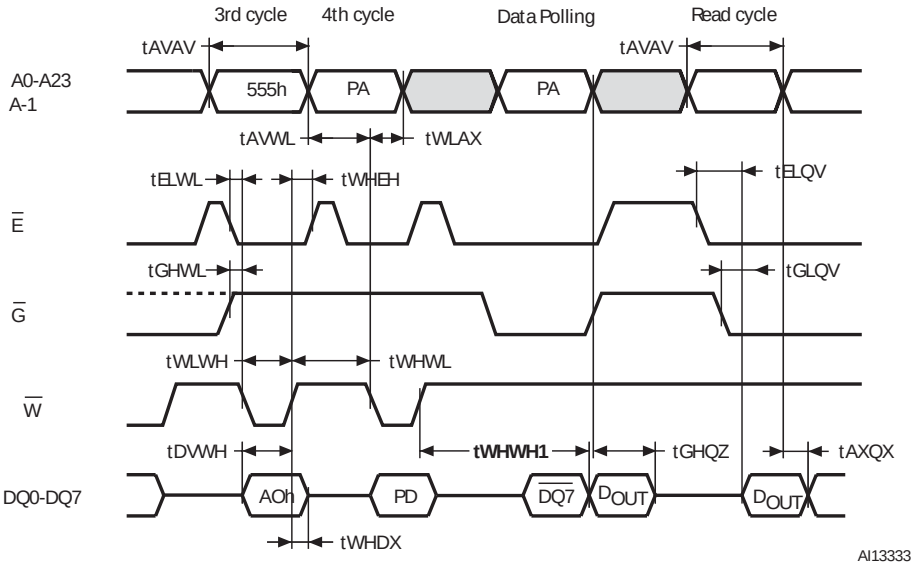


Table 28. Read AC characteristics

Symbol	Alt.	Parameter	Test condition		M29W256GH, M29W256GL			Unit
					60 ns(1) $V_{CCQ}=V_{CC}$	70 ns $V_{CCQ}=V_{CC}$	80 ns V_{CCQ}=1.65 V to V_{CC}	
t_{AVAV}	t_{RC}	Address Valid to Next Address Valid	$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$	Min	60	70	80	ns
t_{AVQV}	t_{ACC}	Address Valid to Output Valid	$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$	Max	60	70	80	ns
t_{AVQV1}	t_{PAGE}	Address Valid to Output Valid (page)	$\overline{E}=V_{IL}$, $\overline{G}=V_{IL}$	Max	25	25	30	ns
t_{ELQX}(2)	t_{LZ}	Chip Enable Low to Output transition	$\overline{G}=V_{IL}$	Min	0	0	0	ns
t_{ELQV}	$t_{\overline{E}}$	Chip Enable Low to Output Valid	$\overline{G}=V_{IL}$	Max	60	70	80	ns
t_{GLQX}(2)	t_{OLZ}	Output Enable Low to Output transition	$\overline{E}=V_{IL}$	Min	0	0	0	ns
t_{GLQV}	t_{OE}	Output Enable Low to Output Valid	$\overline{E}=V_{IL}$	Max	25	25	30	ns
t_{EHQZ}(2)	t_{HZ}	Chip Enable High to Output Hi-Z	$\overline{G}=V_{IL}$	Max	25	25	30	ns
t_{GHQZ}(2)	t_{DF}	Output Enable High to Output Hi-Z	$\overline{E}=V_{IL}$	Max	25	25	30	ns
t_{EHQX} t_{GHQX} t_{AXQX}	t_{OH}	Chip Enable, Output Enable or Address transition to Output transition		Min	0	0	0	ns
t_{ELBL} t_{ELBH}	t_{ELFL} t_{ELFH}	Chip Enable to $\overline{BYTE}$ Low or High		Max	5	5	5	ns
t_{BLQZ}	t_{FLQZ}	$\overline{BYTE}$ Low to Output Hi-Z		Max	25	25	30	ns
t_{BHQV}	t_{FHQV}	$\overline{BYTE}$ High to Output Valid		Max	30	30	30	ns

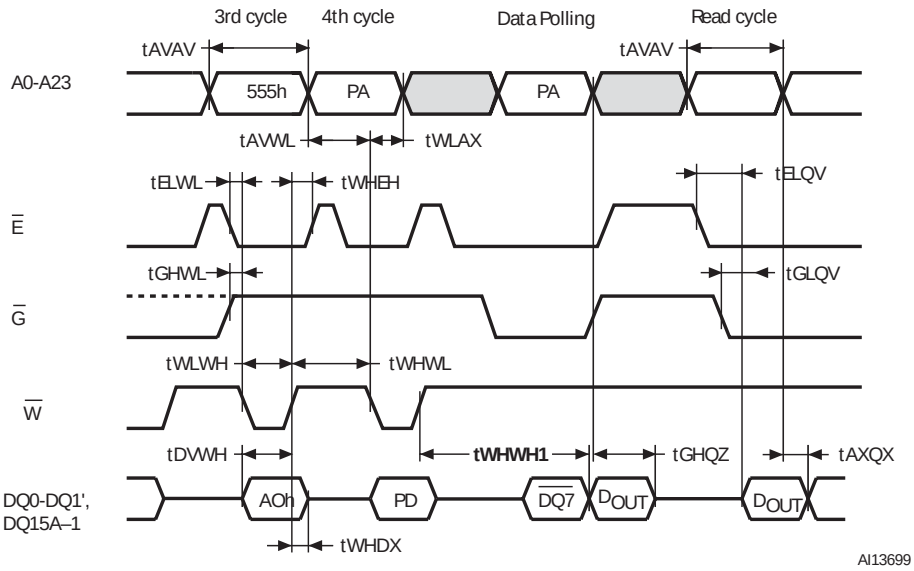
1. Only available upon customer request.
2. Sampled only, not 100% tested.

Figure 16. Write enable controlled program waveforms (8-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit and by a read operation that outputs the data, DOUT, programmed by the previous Program command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.1: Data polling bit (DQ7)*).
4. See *Table 29: Write AC characteristics, write enable controlled*, *Table 30: Write AC characteristics, chip enable controlled* and *Table 28: Read AC characteristics* for details on the timings.

Figure 17. Write enable controlled program waveforms (16-bit mode)



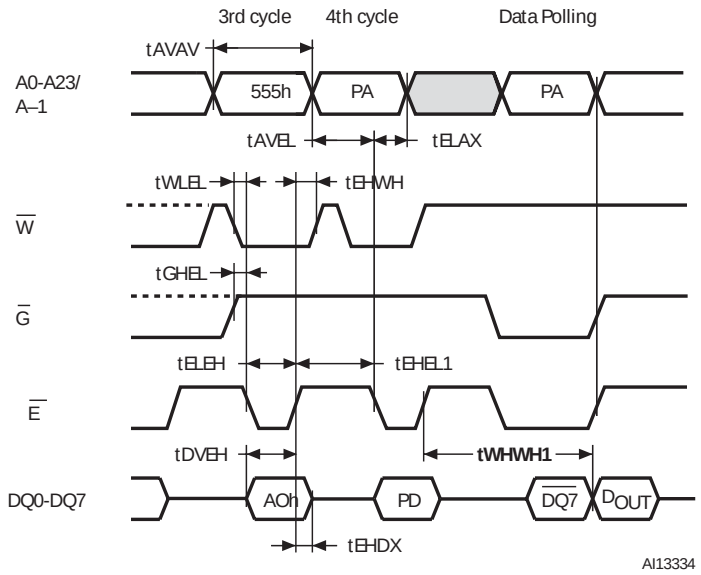
1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit and by a read operation that outputs the data, DOUT, programmed by the previous Program command.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.1: Data polling bit (DQ7)*).
4. See *Table 29: Write AC characteristics, write enable controlled*, *Table 30: Write AC characteristics, chip enable controlled* and *Table 28: Read AC characteristics* for details on the timings.

Table 29. Write AC characteristics, write enable controlled

Symbol	Alt	Parameter		M29W256GH, M29W256GL			Unit
				60 ns(1)	70 ns	80 ns	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	65	75	85	ns
t_{ELWL}	t_{CS}	Chip Enable Low to Write Enable Low	Min	0	0	0	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	Min	35	35	35	ns
t_{DVWH}	t_{DS}	Input Valid to Write Enable High	Min	45	45	45	ns
t_{WHDX}	t_{DH}	Write Enable High to Input transition	Min	0	0	0	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	Min	0	0	0	ns
t_{WHWL}	t_{WPH}	Write Enable High to Write Enable Low	Min	30	30	30	ns
t_{AVWL}	t_{AS}	Address Valid to Write Enable Low	Min	0	0	0	ns
t_{WLAX}	t_{AH}	Write Enable Low to Address transition	Min	45	45	45	ns
t_{GHWL}		Output Enable High to Write Enable Low	Min	0	0	0	ns
t_{WHGL}	t_{OEH}	Write Enable High to Output Enable Low	Min	0	0	0	ns
t_{WHRL}(2)	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	30	ns
t_{VCHEL}	t_{VCS}	V_{CC} High to Chip Enable Low	Min	50	50	50	µs

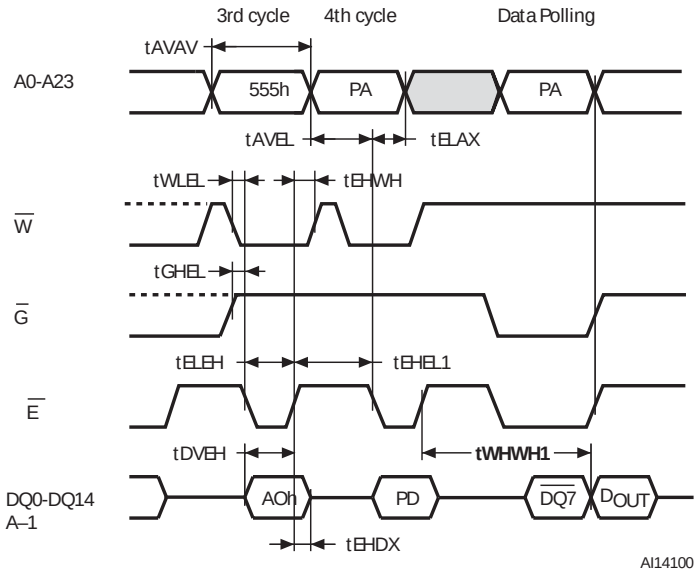
1. Only available upon customer request.
2. Sampled only, not 100% tested.

Figure 18. Chip enable controlled program waveforms (8-bit mode)



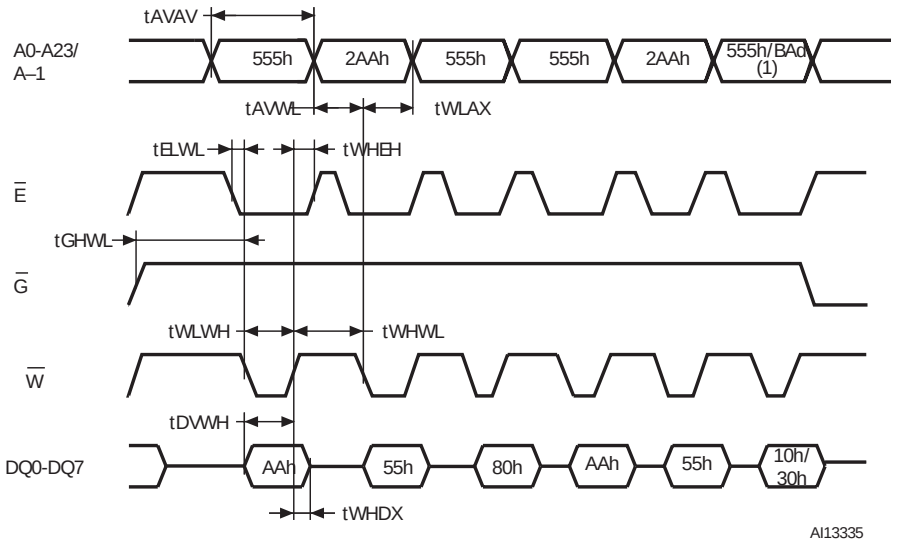
1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.1: Data polling bit (DQ7)*).
4. See *Table 29: Write AC characteristics, write enable controlled*, *Table 30: Write AC characteristics, chip enable controlled* and *Table 28: Read AC characteristics* for details on the timings.

Figure 19. Chip enable controlled program waveforms (16-bit mode)



1. Only the third and fourth cycles of the Program command are represented. The Program command is followed by the check of status register data polling bit.
2. PA is the address of the memory location to be programmed. PD is the data to be programmed.
3. DQ7 is the complement of the data bit being programmed to DQ7 (see *Section 7.1: Data polling bit (DQ7)*).
4. See *Table 29: Write AC characteristics, write enable controlled*, *Table 30: Write AC characteristics, chip enable controlled* and *Table 28: Read AC characteristics* for details on the timings.

Figure 20. Chip/block erase waveforms (8-bit mode)



1. For a Chip Erase command, addresses and data are 555h and 10h, respectively, while they are BAd and 30h for a Block Erase command.
2. BAd is the block address.
3. See *Table 29: Write AC characteristics, write enable controlled*, *Table 30: Write AC characteristics, chip enable controlled* and *Table 28: Read AC characteristics* for details on the timings.

Table 30. Write AC characteristics, chip enable controlled

Symbol	Alt.	Parameter		M29W256GH, M29W256GL			Unit
				60 ns(1)	70 ns	80 ns	
t_{AVAV}	t_{WC}	Address Valid to Next Address Valid	Min	65	75	85	ns
t_{WLEL}	t_{WS}	Write Enable Low to Chip Enable Low	Min	0	0	0	ns
t_{ELEH}	t_{CP}	Chip Enable Low to Chip Enable High	Min	35	35	35	ns
t_{DVEH}	t_{DS}	Input Valid to Chip Enable High	Min	45	45	45	ns
t_{EHDX}	t_{DH}	Chip Enable High to Input transition	Min	0	0	0	ns
t_{EHWH}	t_{WH}	Chip Enable High to Write Enable High	Min	0	0	0	ns
t_{EHEL}	t_{CPH}	Chip Enable High to Chip Enable Low	Min	30	30	30	ns
t_{AVEL}	t_{AS}	Address Valid to Chip Enable Low	Min	0	0	0	ns
t_{ELAX}	t_{AH}	Chip Enable Low to Address transition	Min	45	45	45	ns
t_{GHEL}		Output Enable High Chip Enable Low	Min	0	0	0	ns

1. Only available upon customer request.

Figure 21. Reset AC waveforms (no program/erase ongoing)

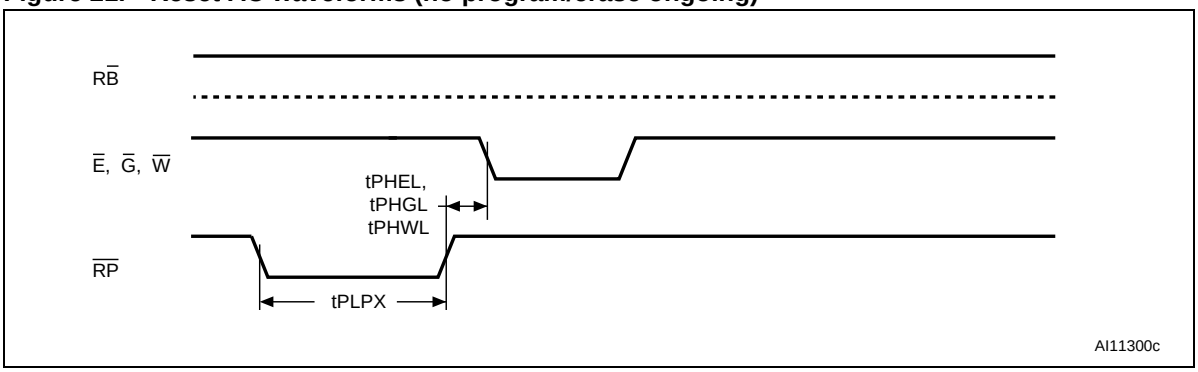


Figure 22. Reset during program/erase operation AC waveforms

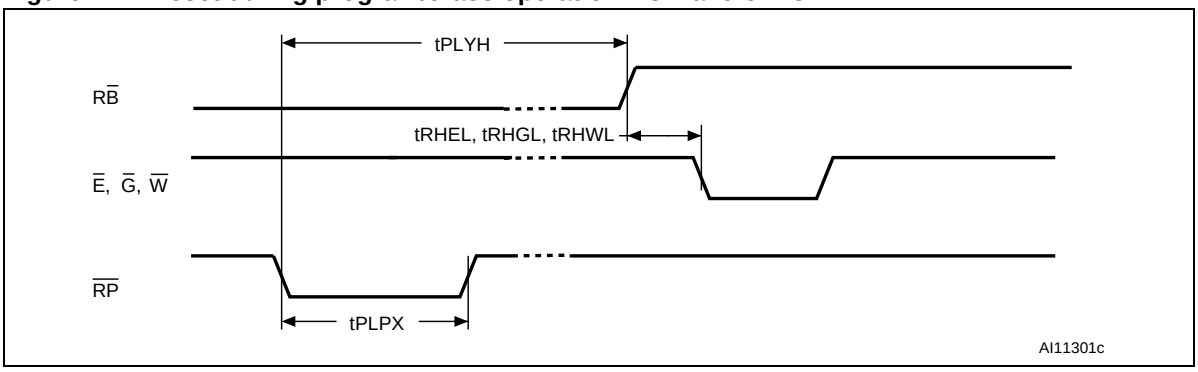


Table 31. Reset AC characteristics

Symbol	Alt.	Parameter		M29W256GH, M29W256GL			Unit
				60[1] ns	70 ns	80 ns	
t_{PLYH}[2]	t_{READY}	$\overline{RP}$ Low to read mode, during program or erase	Max	55	55	55	µs
t_{PLPX}	t_{RP}	$\overline{RP}$ pulse width	Min	20	20	20	µs
t_{PHEL}, t_{PHGL}, t_{PHWL}[2]	t_{RH}	$\overline{RP}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	55	55	55	ns
	t_{RPD}	$\overline{RP}$ Low to standby mode, during read mode	Min	20	20	20	µs
		$\overline{RP}$ Low to standby mode, during program or erase	Min	55	55	55	µs
t_{RHEL}, t_{RHGL}, t_{RHWL}[2]	t_{RB}	$\overline{RB}$ High to Write Enable Low, Chip Enable Low, Output Enable Low	Min	0	0	0	ns

1. Only available upon customer request.
2. Sampled only, not 100% tested.

Figure 23. Accelerated program timing waveforms

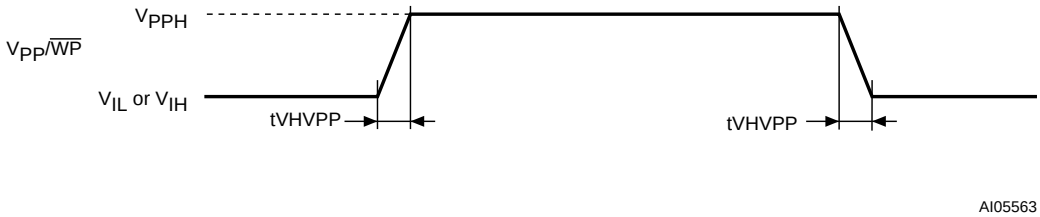
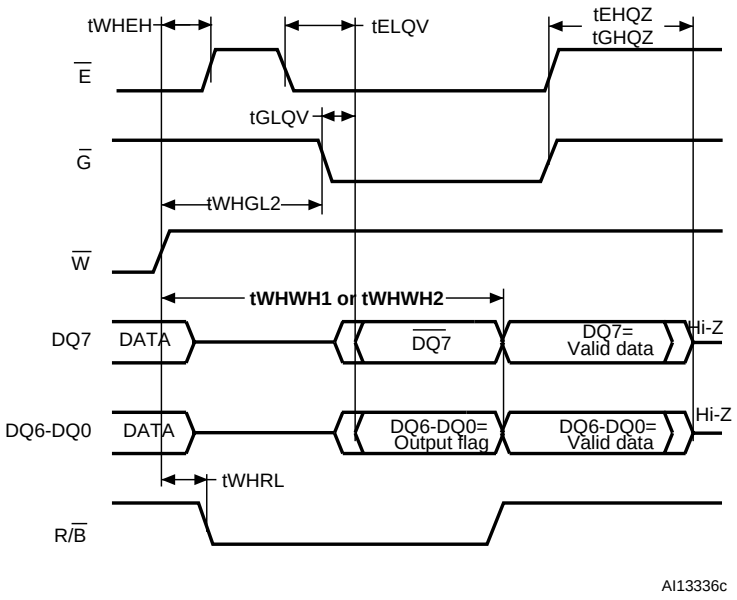
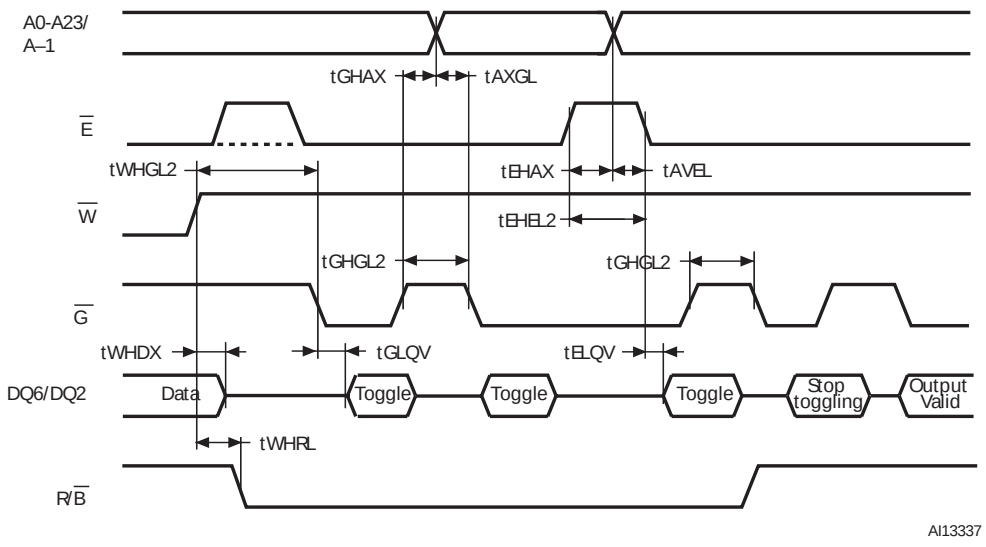


Figure 24. Data polling AC waveforms



1. DQ7 returns valid data bit when the ongoing Program or Erase command is completed.
2. See *Table 32: Accelerated program and data polling/data toggle AC characteristics* and *Table 28: Read AC characteristics* for details on the timings.

Figure 25. Toggle/alternative toggle bit polling AC waveforms (8-bit mode)



1. DQ6 stops toggling when the ongoing Program or Erase command is completed. DQ2 stops toggling when the ongoing Chip Erase or Block Erase command is completed.
2. See *Table 32: Accelerated program and data polling/data toggle AC characteristics* and *Table 28: Read AC characteristics* for details on the timings.

Table 32. Accelerated program and data polling/data toggle AC characteristics

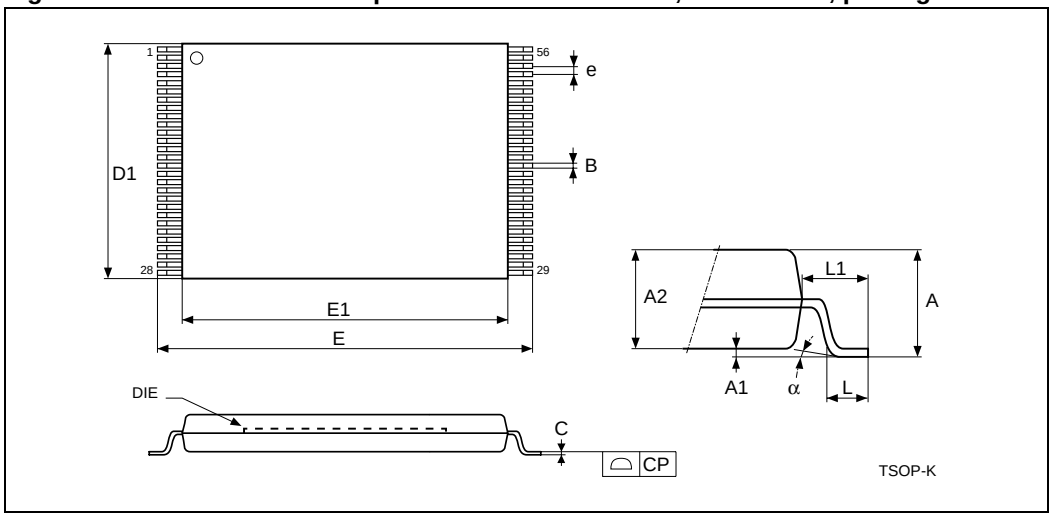
Symbol	Alt	Parameter		M29W256GH, M29W256GL			Unit
				60[1] ns	70 ns	80 ns	
t_{VHVPP}		$V_{PP}/\overline{WP}$ raising and falling time	Min	250	250	250	ns
t_{AXGL}	t_{ASO}	Address setup time to Output Enable Low during toggle bit polling	Min	10	10	10	ns
t_{GHAX}, t_{EHAX}	t_{AHT}	Address hold time from Output Enable during toggle bit polling	Min	10	10	10	ns
t_{EHEL2}	t_{EPH}	Chip Enable High during toggle bit polling	Min	10	10	10	ns
t_{WHGL2}, t_{GHGL2}	t_{OEH}	Output hold time during data and toggle bit polling	Min	20	20	20	ns
t_{WHRL}	t_{BUSY}	Program/Erase Valid to $\overline{RB}$ Low	Max	30	30	30	ns

1. Only available upon customer request.

10 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in RoHS compliant packages. RoHS compliant packages are lead-free. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 26. TSOP56 – 56 lead plastic thin small outline, 14 x 20 mm, package outline

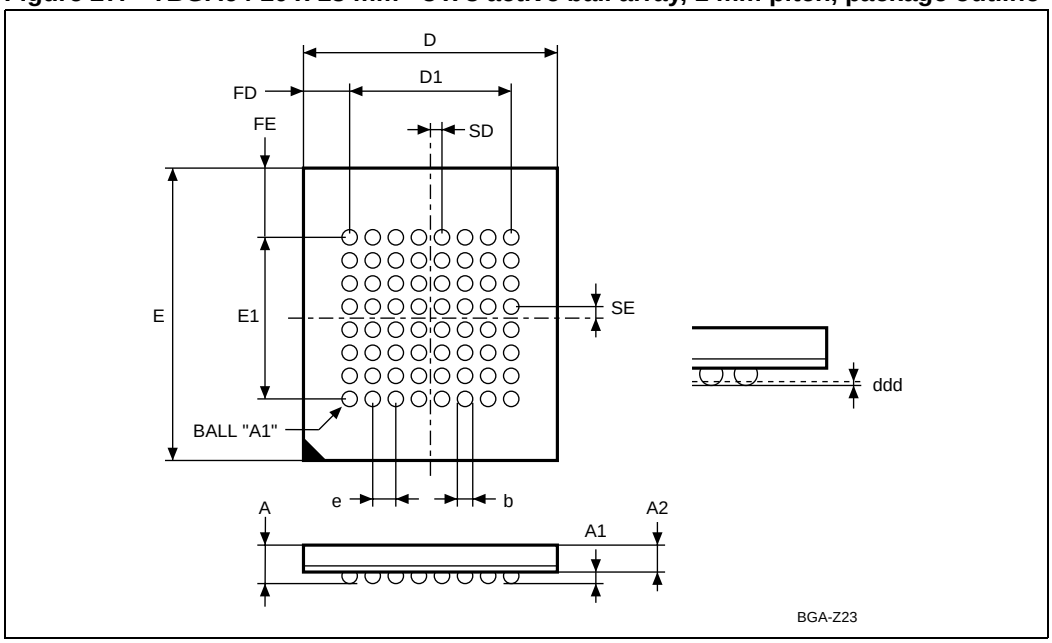


1. Drawing is not to scale.

Table 33. TSOP56 – 56 lead plastic thin small outline, 14 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A	—	—	1.20	—	—	0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C	—	0.10	0.21	—	0.004	0.008
CP	—	—	0.10	—	—	0.004
D1	14.00	13.90	14.10	0.551	0.547	0.555
E	20.00	19.80	20.20	0.787	0.780	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	—	—	0.020	—	—
L	0.60	0.50	0.70	0.024	0.020	0.028
α	3	0	5	3	0	5

Figure 27. TBGA64 10 x 13 mm - 8 x 8 active ball array, 1 mm pitch, package outline

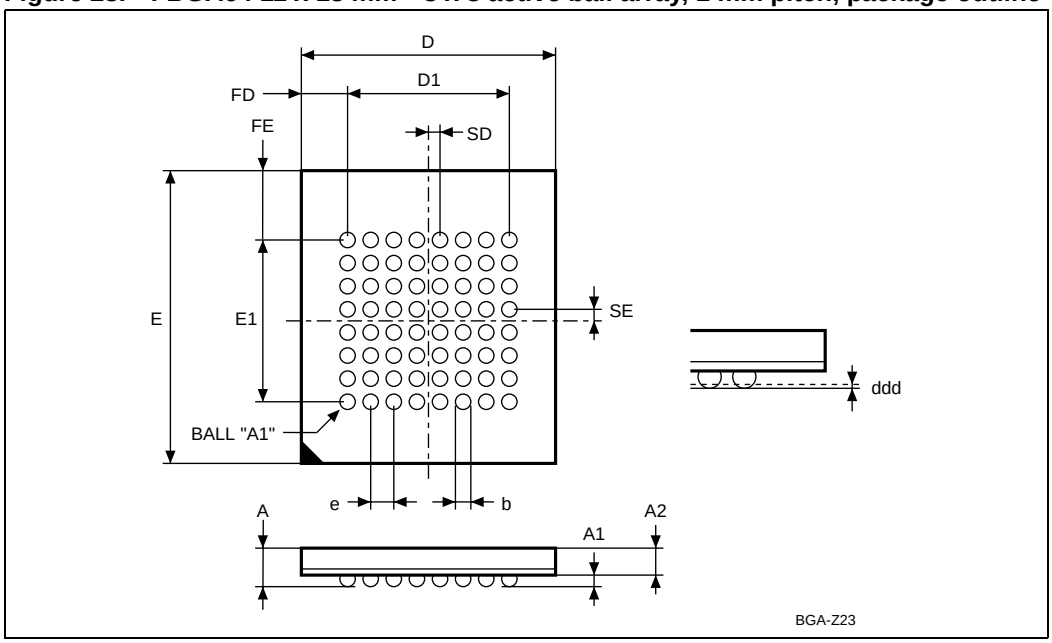


1. Drawing is not to scale.

Table 34. TBGA64 10 x 13 mm - 8 x 8 active ball array, 1 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	—	—	1.20	—	—	0.047
A1	0.30	0.20	0.35	0.012	0.008	0.014
A2	0.80	—	—	0.031	—	—
b	—	0.35	0.50	—	0.014	0.020
D	10.00	9.90	10.10	0.394	0.390	0.398
D1	7.000	—	—	0.276	—	—
ddd	—	—	0.10	—	—	0.004
e	1.00	—	—	0.039	—	—
E	13.00	12.90	13.10	0.512	0.508	0.516
E1	7.00	—	—	0.276	—	—
FD	1.50	—	—	0.059	—	—
FE	3.00	—	—	0.118	—	—
SD	0.50	—	—	0.020	—	—
SE	0.50	—	—	0.020	—	—

Figure 28. FBGA64 11 x 13 mm—8 x 8 active ball array, 1 mm pitch, package outline



1. Drawing is not to scale.

Table 35. FBGA64 11 x 13 mm—8 x 8 active ball array, 1 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A	—	—	1.40	—	—	0.055
A1	0.48	0.43	0.53	0.018	0.016	
A2	0.80	—	—	0.031	—	—
b	—	0.55	0.65	—	0.021	0.025
D	11.00	10.90	11.10	0.433	0.429	0.437
D1	7.00	—	—	0.275	—	—
ddd	—	—	0.15	—	—	0.0059
e	1.00	—	—	0.039	—	—
E	13.0	12.90	13.10	0.511	0.507	0.515
E1	7.00	—	—	0.275	—	—
FD	2.00	—	—	0.078	—	—
FE	3.00	—	—	0.118	—	—
SD	0.50	—	—	0.0196	—	—
SE	0.50	—	—	0.0196	—	—

11 Ordering information

Table 36. Ordering information scheme

Example: M29W256GH 70 N 6 F

Device type

M29

Operating voltage

W = V_{CC} = 2.7 to 3.6 V

Device function

256GH = 256-Mbit (x8/x16), page, uniform block, flash memory, highest block protected by V_{PP}/WP

256GL = 256-Mbit (x8/x16), page, uniform block, flash memory, lowest block protected by V_{PP}/WP

Speed

70 = 70 ns (80 ns if V_{CCQ} = 1.65 V to V_{CC})

60 = 60 ns (80 ns if V_{CCQ} = 1.65 V to V_{CC})(1)

7A = 70 ns (80 ns if V_{CCQ} = 1.65 V to V_{CC}) Automotive qualified (available only with option 6)

Package

N = TSOP56: 14 x 20 mm

ZA = TBGA64: 10 x 13 mm, 1 mm pitch

ZS = FBGA64: 11 x 13 mm, 1 mm pitch

Temperature range

1 = 0 to 70 °C

6 = –40 to 85 °C

Option

E = RoHS compliant package, standard packing

F = RoHS compliant package, tape & reel packing

1. Only available upon customer request.

Note: This product is also available with the extended memory block factory locked. For further details and ordering information contact your nearest Numonyx sales office.

Devices are shipped from the factory with the memory content bits erased to '1'. For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest Numonyx sales office.

Automotive Grade Part is qualified and characterized according to AEC Q100 and Q003 or equivalent; advanced screening according to AEC Q001 and Q002 or equivalent.

Appendix A Block addresses and read/modify protection groups

Table 37 shows block addresses 0-127. *Table 38* shows block addresses 128-255.

Table 37. Block addresses 0 - 127 (page 1 of 4)

Block	Protection group	Block size (Kbytes/ Kwords)	8-bit address range (in hexadecimal)	16-bit address range (in hexadecimal)
0	Protection group	128/64	0000000–001FFFF	0000000–000FFFF
1	Protection group	128/64	0020000–003FFFF	0010000–001FFFF
2	Protection group	128/64	0040000–005FFFF	0020000–002FFFF
3	Protection group	128/64	0060000–007FFFF	0030000–003FFFF
4	Protection group	128/64	0080000–009FFFF	0040000–004FFFF
5	Protection group	128/64	00A0000–00BFFFF	0050000–005FFFF
6	Protection group	128/64	00C0000–00DFFFF	0060000–006FFFF
7	Protection group	128/64	00E0000–00FFFFF	0070000–007FFFF
8	Protection group	128/64	0100000–011FFFF	0080000–008FFFF
9	Protection group	128/64	0120000–013FFFF	0090000–009FFFF
10	Protection group	128/64	0140000–015FFFF	00A0000–00AFFFF
11	Protection group	128/64	0160000–017FFFF	00B0000–00BFFFF
12	Protection group	128/64	0180000–019FFFF	00C0000–00CFFFF
13	Protection group	128/64	01A0000–01BFFFF	00D0000–00DFFFF
14	Protection group	128/64	01C0000–01DFFFF	00E0000–00EFFFF
15	Protection group	128/64	01E0000–01FFFFF	00F0000–00FFFFF
16	Protection group	128/64	0200000–021FFFF	0100000–010FFFF
17	Protection group	128/64	0220000–023FFFF	0110000–011FFFF
18	Protection group	128/64	0240000–025FFFF	0120000–012FFFF
19	Protection group	128/64	0260000–027FFFF	0130000–013FFFF
20	Protection group	128/64	0280000–029FFFF	0140000–014FFFF
21	Protection group	128/64	02A0000–02BFFFF	0150000–015FFFF
22	Protection group	128/64	02C0000–02DFFFF	0160000–016FFFF
23	Protection group	128/64	02E0000–02FFFFF	0170000–017FFFF
24	Protection group	128/64	0300000–031FFFF	0180000–018FFFF
25	Protection group	128/64	0320000–033FFFF	0190000–019FFFF
26	Protection group	128/64	0340000–035FFFF	01A0000–01AFFFF
27	Protection group	128/64	0360000–037FFFF	01B0000–01BFFFF
28	Protection group	128/64	0380000–039FFFF	01C0000–01CFFFF

Table 37. Block addresses 0 - 127 (page 2 of 4)

Block	Protection group	Block size (Kbytes/ Kwords)	8-bit address range (in hexadecimal)	16-bit address range (in hexadecimal)
29	Protection group	128/64	03A0000–03BFFFF	01D0000–01DFFFF
30	Protection group	128/64	03C0000–03DFFFF	01E0000–01EFFFF
31	Protection group	128/64	03E0000–03FFFFF	01F0000–01FFFFF
32	Protection group	128/64	0400000–041FFFF	0200000–020FFFF
33	Protection group	128/64	0420000–043FFFF	0210000–021FFFF
34	Protection group	128/64	0440000–045FFFF	0220000–022FFFF
35	Protection group	128/64	0460000–047FFFF	0230000–023FFFF
36	Protection group	128/64	0480000–049FFFF	0240000–024FFFF
37	Protection group	128/64	04A0000–04BFFFF	0250000–025FFFF
38	Protection group	128/64	04C0000–04DFFFF	0260000–026FFFF
39	Protection group	128/64	04E0000–04FFFFF	0270000–027FFFF
40	Protection group	128/64	0500000–051FFFF	0280000–028FFFF
41	Protection group	128/64	0520000–053FFFF	0290000–029FFFF
42	Protection group	128/64	0540000–055FFFF	02A0000–02AFFFF
43	Protection group	128/64	0560000–057FFFF	02B0000–02BFFFF
44	Protection group	128/64	0580000–059FFFF	02C0000–02CFFFF
45	Protection group	128/64	05A0000–05BFFFF	02D0000–02DFFFF
46	Protection group	128/64	05C0000–05DFFFF	02E0000–02EFFFF
47	Protection group	128/64	05E0000–05FFFFF	02F0000–02FFFFF
48	Protection group	128/64	0600000–061FFFF	0300000–030FFFF
49	Protection group	128/64	0620000–063FFFF	0310000–031FFFF
50	Protection group	128/64	0640000–065FFFF	0320000–032FFFF
51	Protection group	128/64	0660000–067FFFF	0330000–033FFFF
52	Protection group	128/64	0680000–069FFFF	0340000–034FFFF
53	Protection group	128/64	06A0000–06BFFFF	0350000–035FFFF
54	Protection group	128/64	06C0000–06DFFFF	0360000–036FFFF
55	Protection group	128/64	06E0000–06FFFFF	0370000–037FFFF
56	Protection group	128/64	0700000–071FFFF	0380000–038FFFF
57	Protection group	128/64	0720000–073FFFF	0390000–039FFFF
58	Protection group	128/64	0740000–075FFFF	03A0000–03AFFFF
59	Protection group	128/64	0760000–077FFFF	03B0000–03BFFFF
60	Protection group	128/64	0780000–079FFFF	03C0000–03CFFFF
61	Protection group	128/64	07A0000–07BFFFF	03D0000–03DFFFF

Table 37. Block addresses 0 - 127 (page 3 of 4)

Block	Protection group	Block size (Kbytes/ Kwords)	8-bit address range (in hexadecimal)	16-bit address range (in hexadecimal)
62	Protection group	128/64	07C0000–07DFFFF	03E0000–03EFFFF
63	Protection group	128/64	07E0000–07FFFFF	03F0000–03FFFFF
64	Protection group	128/64	0800000–081FFFF	0400000–040FFFF
65	Protection group	128/64	0820000–083FFFF	0410000–041FFFF
66	Protection group	128/64	0840000–085FFFF	0420000–042FFFF
67	Protection group	128/64	0860000–087FFFF	0430000–043FFFF
68	Protection group	128/64	0880000–089FFFF	0440000–044FFFF
69	Protection group	128/64	08A0000–08BFFFF	0450000–045FFFF
70	Protection group	128/64	08C0000–08DFFFF	0460000–046FFFF
71	Protection group	128/64	08E0000–08FFFFF	0470000–047FFFF
72	Protection group	128/64	0900000–091FFFF	0480000–048FFFF
73	Protection group	128/64	0920000–093FFFF	0490000–049FFFF
74	Protection group	128/64	0940000–095FFFF	04A0000–04AFFFF
75	Protection group	128/64	0960000–097FFFF	04B0000–04BFFFF
76	Protection group	128/64	0980000–099FFFF	04C0000–04CFFFF
77	Protection group	128/64	09A0000–09BFFFF	04D0000–04DFFFF
78	Protection group	128/64	09C0000–09DFFFF	04E0000–04EFFFF
79	Protection group	128/64	09E0000–09FFFFF	04F0000–04FFFFF
80	Protection group	128/64	0A00000–0A1FFFF	0500000–050FFFF
81	Protection group	128/64	0A20000–0A3FFFF	0510000–051FFFF
82	Protection group	128/64	0A40000–0A5FFFF	0520000–052FFFF
83	Protection group	128/64	0A60000–0A7FFFF	0530000–053FFFF
84	Protection group	128/64	0A80000–0A9FFFF	0540000–054FFFF
85	Protection group	128/64	0AA0000–0ABFFFF	0550000–055FFFF
86	Protection group	128/64	0AC0000–0ADFFFF	0560000–056FFFF
87	Protection group	128/64	0AE0000–0AFFFFF	0570000–057FFFF
88	Protection group	128/64	0B00000–0B1FFFF	0580000–058FFFF
89	Protection group	128/64	0B20000–0B3FFFF	0590000–059FFFF
90	Protection group	128/64	0B40000–0B5FFFF	05A0000–05AFFFF
91	Protection group	128/64	0B60000–0B7FFFF	05B0000–05BFFFF
92	Protection group	128/64	0B80000–0B9FFFF	05C0000–05CFFFF
93	Protection group	128/64	0BA0000–0BBFFFF	05D0000–05DFFFF
94	Protection group	128/64	0BC0000–0BDFFFF	05E0000–05EFFFF

Table 37. Block addresses 0 - 127 (page 4 of 4)

Block	Protection group	Block size (Kbytes/ Kwords)	8-bit address range (in hexadecimal)	16-bit address range (in hexadecimal)
95	Protection group	128/64	0BE0000–0BFFFFF	05F0000–05FFFFF
96	Protection group	128/64	0C00000–0C1FFFF	0600000–060FFFF
97	Protection group	128/64	0C20000–0C3FFFF	0610000–061FFFF
98	Protection group	128/64	0C40000–0C5FFFF	0620000–062FFFF
99	Protection group	128/64	0C60000–0C7FFFF	0630000–063FFFF
100	Protection group	128/64	0C80000–0C9FFFF	0640000–064FFFF
101	Protection group	128/64	0CA0000–0CBFFFF	0650000–065FFFF
102	Protection group	128/64	0CC0000–0CDFFFF	0660000–066FFFF
103	Protection group	128/64	0CE0000–0CFFFFF	0670000–067FFFF
104	Protection group	128/64	0D00000–0D1FFFF	0680000–068FFFF
105	Protection group	128/64	0D20000–0D3FFFF	0690000–069FFFF
106	Protection group	128/64	0D40000–0D5FFFF	06A0000–06AFFFF
107	Protection group	128/64	0D60000–0D7FFFF	06B0000–06BFFFF
108	Protection group	128/64	0D80000–0D9FFFF	06C0000–06CFFFF
109	Protection group	128/64	0DA0000–0DBFFFF	06D0000–06DFFFF
110	Protection group	128/64	0DC0000–0DDFFFF	06E0000–06EFFFF
111	Protection group	128/64	0DE0000–0DFFFFF	06F0000–06FFFFF
112	Protection group	128/64	0E00000–0E1FFFF	0700000–070FFFF
113	Protection group	128/64	0E20000–0E3FFFF	0710000–071FFFF
114	Protection group	128/64	0E40000–0E5FFFF	0720000–072FFFF
115	Protection group	128/64	0E60000–0E7FFFF	0730000–073FFFF
116	Protection group	128/64	0E80000–0E9FFFF	0740000–074FFFF
117	Protection group	128/64	0EA0000–0EBFFFF	0750000–075FFFF
118	Protection group	128/64	0EC0000–0EDFFFF	0760000–076FFFF
119	Protection group	128/64	0EE0000–0EFFFFF	0770000–077FFFF
120	Protection group	128/64	0F00000–0F1FFFF	0780000–078FFFF
121	Protection group	128/64	0F20000–0F3FFFF	0790000–079FFFF
122	Protection group	128/64	0F40000–0F5FFFF	07A0000–07AFFFF
123	Protection group	128/64	0F60000–0F7FFFF	07B0000–07BFFFF
124	Protection group	128/64	0F80000–0F9FFFF	07C0000–07CFFFF
125	Protection group	128/64	0FA0000–0FBFFFF	07D0000–07DFFFF
126	Protection group	128/64	0FC0000–0FDFFFF	07E0000–07EFFFF
127	Protection group	128/64	0FE0000–0FFFFFF	07F0000–07FFFFF

Table 38. Block addresses 128 - 255 (page 1 of 4)

Block	Block size, x8	Block size, x16	8-bit address range (in hexadecimal)		16-bit address range (in hexadecimal)	
128	128	64	1000000	101FFFF	0800000	080FFFF
129	128	64	1020000	103FFFF	0810000	081FFFF
130	128	64	1040000	105FFFF	0820000	082FFFF
131	128	64	1060000	107FFFF	0830000	083FFFF
132	128	64	1080000	109FFFF	0840000	084FFFF
133	128	64	10A0000	10BFFFF	0850000	085FFFF
134	128	64	10C0000	10DFFFF	0860000	086FFFF
135	128	64	10E0000	10FFFFF	0870000	087FFFF
136	128	64	1100000	111FFFF	0880000	088FFFF
137	128	64	1120000	113FFFF	0890000	089FFFF
138	128	64	1140000	115FFFF	08A0000	08AFFFF
139	128	64	1160000	117FFFF	08B0000	08BFFFF
140	128	64	1180000	119FFFF	08C0000	08CFFFF
141	128	64	11A0000	11BFFFF	08D0000	08DFFFF
142	128	64	11C0000	11DFFFF	08E0000	08EFFFF
143	128	64	11E0000	11FFFFF	08F0000	08FFFFF
144	128	64	1200000	121FFFF	0900000	090FFFF
145	128	64	1220000	123FFFF	0910000	091FFFF
146	128	64	1240000	125FFFF	0920000	092FFFF
147	128	64	1260000	127FFFF	0930000	093FFFF
148	128	64	1280000	129FFFF	0940000	094FFFF
149	128	64	12A0000	12BFFFF	0950000	095FFFF
150	128	64	12C0000	12DFFFF	0960000	096FFFF
151	128	64	12E0000	12FFFFF	0970000	097FFFF
152	128	64	1300000	131FFFF	0980000	098FFFF
153	128	64	1320000	133FFFF	0990000	099FFFF
154	128	64	1340000	135FFFF	09A0000	09AFFFF
155	128	64	1360000	137FFFF	09B0000	09BFFFF
156	128	64	1380000	139FFFF	09C0000	09CFFFF
157	128	64	13A0000	13BFFFF	09D0000	09DFFFF
158	128	64	13C0000	13DFFFF	09E0000	09EFFFF
159	128	64	13E0000	13FFFFF	09F0000	09FFFFF
160	128	64	1400000	141FFFF	0A00000	0A0FFFF
161	128	64	1420000	143FFFF	0A10000	0A1FFFF

Table 38. Block addresses 128 - 255 (page 2 of 4)

Block	Block size, x8	Block size, x16	8-bit address range (in hexadecimal)		16-bit address range (in hexadecimal)	
162	128	64	1440000	145FFFF	0A20000	0A2FFFF
163	128	64	1460000	147FFFF	0A30000	0A3FFFF
164	128	64	1480000	149FFFF	0A40000	0A4FFFF
165	128	64	14A0000	14BFFFF	0A50000	0A5FFFF
166	128	64	14C0000	14DFFFF	0A60000	0A6FFFF
167	128	64	14E0000	14FFFFF	0A70000	0A7FFFF
168	128	64	1500000	151FFFF	0A80000	0A8FFFF
169	128	64	1520000	153FFFF	0A90000	0A9FFFF
170	128	64	1540000	155FFFF	0AA0000	0AAFFFF
171	128	64	1560000	157FFFF	0AB0000	0ABFFFF
172	128	64	1580000	159FFFF	0AC0000	0ACFFFF
173	128	64	15A0000	15BFFFF	0AD0000	0ADFFFF
174	128	64	15C0000	15DFFFF	0AE0000	0AEFFFF
175	128	64	15E0000	15FFFFF	0AF0000	0AFFFFF
176	128	64	1600000	161FFFF	0B00000	0B0FFFF
177	128	64	1620000	163FFFF	0B10000	0B1FFFF
178	128	64	1640000	165FFFF	0B20000	0B2FFFF
179	128	64	1660000	167FFFF	0B30000	0B3FFFF
180	128	64	1680000	169FFFF	0B40000	0B4FFFF
181	128	64	16A0000	16BFFFF	0B50000	0B5FFFF
182	128	64	16C0000	16DFFFF	0B60000	0B6FFFF
183	128	64	16E0000	16FFFFF	0B70000	0B7FFFF
184	128	64	1700000	171FFFF	0B80000	0B8FFFF
185	128	64	1720000	173FFFF	0B90000	0B9FFFF
186	128	64	1740000	175FFFF	0BA0000	0BAFFFF
187	128	64	1760000	177FFFF	0BB0000	0BBFFFF
188	128	64	1780000	179FFFF	0BC0000	0BCFFFF
189	128	64	17A0000	17BFFFF	0BD0000	0BDFFFF
190	128	64	17C0000	17DFFFF	0BE0000	0BEFFFF
191	128	64	17E0000	17FFFFF	0BF0000	0BFFFFF
192	128	64	1800000	181FFFF	0C00000	0C0FFFF
193	128	64	1820000	183FFFF	0C10000	0C1FFFF
194	128	64	1840000	185FFFF	0C20000	0C2FFFF
195	128	64	1860000	187FFFF	0C30000	0C3FFFF

Table 38. Block addresses 128 - 255 (page 3 of 4)

Block	Block size, x8	Block size, x16	8-bit address range (in hexadecimal)		16-bit address range (in hexadecimal)	
196	128	64	1880000	189FFFF	0C40000	0C4FFFF
197	128	64	18A0000	18BFFFF	0C50000	0C5FFFF
198	128	64	18C0000	18DFFFF	0C60000	0C6FFFF
199	128	64	18E0000	18FFFFF	0C70000	0C7FFFF
200	128	64	1900000	191FFFF	0C80000	0C8FFFF
201	128	64	1920000	193FFFF	0C90000	0C9FFFF
202	128	64	1940000	195FFFF	0CA0000	0CAFFFF
203	128	64	1960000	197FFFF	0CB0000	0CBFFFF
204	128	64	1980000	199FFFF	0CC0000	0CCFFFF
205	128	64	19A0000	19BFFFF	0CD0000	0CDFFFF
206	128	64	19C0000	19DFFFF	0CE0000	0CEFFFF
207	128	64	19E0000	19FFFFF	0CF0000	0CFFFFF
208	128	64	1A00000	1A1FFFF	0D00000	0D0FFFF
209	128	64	1A20000	1A3FFFF	0D10000	0D1FFFF
210	128	64	1A40000	1A5FFFF	0D20000	0D2FFFF
211	128	64	1A60000	1A7FFFF	0D30000	0D3FFFF
212	128	64	1A80000	1A9FFFF	0D40000	0D4FFFF
213	128	64	1AA0000	1ABFFFF	0D50000	0D5FFFF
214	128	64	1AC0000	1ADFFFF	0D60000	0D6FFFF
215	128	64	1AE0000	1AFFFFF	0D70000	0D7FFFF
216	128	64	1B00000	1B1FFFF	0D80000	0D8FFFF
217	128	64	1B20000	1B3FFFF	0D90000	0D9FFFF
218	128	64	1B40000	1B5FFFF	0DA0000	0DAFFFF
219	128	64	1B60000	1B7FFFF	0DB0000	0DBFFFF
220	128	64	1B80000	1B9FFFF	0DC0000	0DCFFFF
221	128	64	1BA0000	1BBFFFF	0DD0000	0DDFFFF
222	128	64	1BC0000	1BDFFFF	0DE0000	0DEFFFF
223	128	64	1BE0000	1BFFFFF	0DF0000	0DFFFFF
224	128	64	1C00000	1C1FFFF	0E00000	0E0FFFF
225	128	64	1C20000	1C3FFFF	0E10000	0E1FFFF
226	128	64	1C40000	1C5FFFF	0E20000	0E2FFFF
227	128	64	1C60000	1C7FFFF	0E30000	0E3FFFF
228	128	64	1C80000	1C9FFFF	0E40000	0E4FFFF
229	128	64	1CA0000	1CBFFFF	0E50000	0E5FFFF

Table 38. Block addresses 128 - 255 (page 4 of 4)

Block	Block size, x8	Block size, x16	8-bit address range (in hexadecimal)		16-bit address range (in hexadecimal)	
230	128	64	1CC0000	1CDFFFF	0E60000	0E6FFFF
231	128	64	1CE0000	1CFFFFF	0E70000	0E7FFFF
232	128	64	1D00000	1D1FFFF	0E80000	0E8FFFF
233	128	64	1D20000	1D3FFFF	0E90000	0E9FFFF
234	128	64	1D40000	1D5FFFF	0EA0000	0EAFFFF
235	128	64	1D60000	1D7FFFF	0EB0000	0EBFFFF
236	128	64	1D80000	1D9FFFF	0EC0000	0ECFFFF
237	128	64	1DA0000	1DBFFFF	0ED0000	0EDFFFF
238	128	64	1DC0000	1DDFFFF	0EE0000	0EEFFFF
239	128	64	1DE0000	1DFFFFF	0EF0000	0EFFFFF
240	128	64	1E00000	1E1FFFF	0F00000	0F0FFFF
241	128	64	1E20000	1E3FFFF	0F10000	0F1FFFF
242	128	64	1E40000	1E5FFFF	0F20000	0F2FFFF
243	128	64	1E60000	1E7FFFF	0F30000	0F3FFFF
244	128	64	1E80000	1E9FFFF	0F40000	0F4FFFF
245	128	64	1EA0000	1EBFFFF	0F50000	0F5FFFF
246	128	64	1EC0000	1EDFFFF	0F60000	0F6FFFF
247	128	64	1EE0000	1EFFFFF	0F70000	0F7FFFF
248	128	64	1F00000	1F1FFFF	0F80000	0F8FFFF
249	128	64	1F20000	1F3FFFF	0F90000	0F9FFFF
250	128	64	1F40000	1F5FFFF	0FA0000	0FAFFFF
251	128	64	1F60000	1F7FFFF	0FB0000	0FBFFFF
252	128	64	1F80000	1F9FFFF	0FC0000	0FCFFFF
253	128	64	1FA0000	1FBFFFF	0FD0000	0FDFFFF
254	128	64	1FC0000	1FDFFFF	0FE0000	0FEFFFF
255	128	64	1FE0000	1FFFFFF	0FF0000	0FFFFFF

Appendix B Common flash interface (CFI)

The common flash interface is a JEDEC approved, standardized data structure that can be read from the flash memory device. It allows a system software to query the device to determine various electrical and timing parameters, density information and functions supported by the memory. The system can interface easily with the device, enabling the software to upgrade itself when necessary.

When the Read CFI Query command is issued, the memory enters read CFI query mode and read operations output the CFI data. *Table 39*, *Table 40*, *Table 41*, *Table 42*, *Table 43* and *Table 44* show the addresses (A-1, A0-A7) used to retrieve the data. The CFI data structure also contains a security area where a 64-bit unique security number is written (see *Table 44: Security code area*). This area can be accessed only in read mode by the final user. It is impossible to change the security number after it has been written by Numonyx.

Table 39. Query structure overview(1)

Address		Sub-section name	Description
x16	x8		
10h	20h	CFI query identification string	Command set ID and algorithm data offset
1Bh	36h	System interface information	Device timing & voltage information
27h	4Eh	Device geometry definition	Flash device layout
40h	80h	Primary algorithm-specific extended query table	Additional information specific to the primary algorithm (optional)
61h	C2h	Security code area	64-bit unique device number

1. Query data are always presented on the lowest order data outputs.

Table 40. CFI query identification string(1)

Address		Data	Description	Value
x16	x8			
10h	20h	0051h	Query unique ASCII string ‘QRY’	‘Q’
11h	22h	0052h		‘R’
12h	24h	0059h		‘Y’
13h	26h	0002h	Primary algorithm command set and control interface ID code 16 bit ID code defining a specific algorithm	Spansion compatible
14h	28h	0000h		
15h	2Ah	0040h	Address for primary algorithm extended query table (see *Table 43*)	P = 40h
16h	2Ch	0000h		
17h	2Eh	0000h	Alternate vendor command set and control interface ID code second vendor - specified algorithm supported	NA
18h	30h	0000h		
19h	32h	0000h	Address for alternate algorithm extended query table	NA
1Ah	34h	0000h		

1. Query data are always presented on the lowest order data outputs (DQ7-DQ0) only. DQ8-DQ15 are ‘0’.

Table 41. CFI query system interface information(1)

Address		Data	Description	Value
x16	x8			
1Bh	36h	0027h	V_{CC} logic supply minimum program/erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	2.7 V
1Ch	38h	0036h	V_{CC} logic supply maximum program/erase voltage bit 7 to 4BCD value in volts bit 3 to 0BCD value in 100 mV	3.6 V
1Dh	3Ah	00B5h	V_{PPH} [programming] supply minimum program/erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	11.5 V
1Eh	3Ch	00C5h	V_{PPH} [programming] supply maximum program/erase voltage bit 7 to 4HEX value in volts bit 3 to 0BCD value in 100 mV	12.5 V
1Fh	3Eh	0004h	Typical timeout for single byte/word program = 2^n µs	16 µs
20h	40h	0004h	Typical timeout for minimum size write buffer program = 2^n µs	16 µs
21h	42h	0009h	Typical timeout for individual block erase = 2^n ms	0.5 s
22h	44h	0011h	Typical timeout for full chip erase = 2^n ms	80 s
23h	46h	0004h	Maximum timeout for byte/word program = 2^n times typical	200 µs
24h	48h	0004h	Maximum timeout for write buffer program = 2^n times typical	200 µs
25h	4Ah	0003h	Maximum timeout per individual block erase = 2^n times typical	2.3 s
26h	4Ch	0004h	Maximum timeout for chip erase = 2^n times typical	800 s

1. The values given in the above table are valid for both packages.

Table 42. Device geometry definition

Address		Data	Description	Value
x16	x8			
27h	4Eh	0019h	Device size = 2^n in number of bytes	32 Mbytes
28h 29h	50h 52h	0002h 0000h	Flash device interface code description	x8, x16 async.
2Ah 2Bh	54h 56h	0006h 0000h	Maximum number of bytes in multiple-byte program or page= 2^n	64
2Ch	58h	0001h	Number of Erase block regions. It specifies the number of regions containing contiguous Erase blocks of the same size.	1
2Dh 2Eh	5Ah 5Ch	00FFh 0000h	Erase block region 1 information Number of Erase blocks of identical size = 007Fh +1	256
2Fh 30h	5Eh 60h	0000h 0002h	Erase block region 1 information Block size in region 1 = 0200h * 256 byte	128 Kbytes
31h 32h 33h 34h	62h 64h 66h 68h	0000h 0000h 0000h 0000h	Erase block region 2 information	0
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase block region 3 information	0
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information	0

Table 43. Primary algorithm-specific extended query table (1)

Address		Data	Description	Value
x16	x8			
40h	80h	0050h	Primary algorithm extended query table unique ASCII string “PRI”	‘P’
41h	82h	0052h		‘R’
42h	84h	0049h		‘I’
43h	86h	0031h	Major version number, ASCII	‘1’
44h	88h	0033h	Minor version number, ASCII	‘3’
45h	8Ah	0010h	Address sensitive unlock (bits 1 to 0) 00 = required, 01= not required Silicon revision number (bits 7 to 2)	Yes 65 nm
46h	8Ch	0002h	Erase suspend 00 = not supported, 01 = read only, 02 = read and write	2
47h	8Eh	0001h	Block protection 00 = not supported, x = number of blocks per group	1
48h	90h	0000h	Temporary block unprotect 00 = not supported, 01 = supported	Not supported
49h	92h	0008h	Block protect /unprotect 06 = M29W256GH/M29W256GL	6
4Ah	94h	0000h	Simultaneous operations: not supported	NA
4Bh	96h	0000h	Burst mode, 00 = not supported, 01 = supported	Not supported
4Ch	98h	0002h	Page mode, 00 = not supported, 02 = 8-word page	02
4Dh	9Ah	00B5h	V_{PPH} supply minimum program/erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	11.5 V
4Eh	9Ch	00C5h	V_{PPH} supply maximum program/erase voltage bit 7 to 4 HEX value in volts bit 3 to 0 BCD value in 100 mV	12.5 V
4Fh	9Eh	00xxh	Top/bottom boot block flag xx = 04 = M29W256GL. First block protected by $V_{PP}/\overline{WP}$ xx = 05 = M29W256GH. Last block protected by $V_{PP}/\overline{WP}$	Uniform + $V_{PP}/\overline{WP}$ protecting highest or lowest block
50h	A0h	0001h	Program suspend, 00 = not supported, 01 = supported	Supported

1. The values given in the above table are valid for both packages.

Table 44. Security code area

Address		Data	Description
x16	x8		
61h	C3h, C2h	XXXX	64-bit: unique device number
62h	C5h, C4h	XXXX	
63h	C7h, C6h	XXXX	
64h	C9h, C8h	XXXX	

Appendix C Extended memory block

The M29W256GH/L has an extra block, the extended memory block, that can be accessed using a dedicated command. This extended memory block is 128 words in x 16 mode and 256 bytes in x 8 mode. It is used as a security block (to provide a permanent security identification number) or to store additional information.

The device can be shipped either with the extended memory block factory locked, or factory unlocked.

The extended memory block cannot be erased, and is one-time programmable (OTP) memory. If memory block is factory locked or customer protected by setting the extended memory block protection bit, it cannot be further modified.

If the extended memory block is not factory locked, it can be customer lockable. Its status is indicated by bit DQ7 in autoselect mode. This bit is permanently set to either ‘1’ or ‘0’ at the factory and cannot be changed. When set to ‘1’, it indicates that the device is factory locked and the extended memory block is protected. When set to ‘0’, it indicates that the device is customer lockable. Bit DQ7 being permanently locked to either ‘1’ or ‘0’ is another security feature which ensures that a customer lockable device cannot be used instead of a factory locked one.

Bit DQ7 is the most significant bit in the extended memory block verify indicator. It can be read in auto select mode using either the programmer (see *Table 8* and *Table 9*) or the in-system method (see *Table 12* and *Table 13*).

The extended memory block can only be accessed when the device is in extended memory block mode. For details of how the extended memory block mode is entered and exited, refer to the *Section 6.4.2: Extended Memory Block* and to *Table 19* and *Table 20*.

C.1 Factory locked extended memory block

In devices where the extended memory block is factory locked, the security identification number is written to the extended memory block address space (see *Table 45: Extended memory block address and data*) in the factory. The DQ7 bit is set to ‘1’ and the extended memory block cannot be unprotected.

C.2 Customer lockable extended memory block

A device where the extended memory block is customer lockable is delivered with the DQ7 bit set to ‘0’ and the extended memory block unprotected. It is up to the customer to program and protect the extended memory block but care must be taken because the protection of the extended memory block is not reversible.

If the device has not been shipped with the extended memory block factory protected, the block can be protected by setting the extended memory block protection bit, DQ0, to ‘0’.

However, this bit is one-time programmable and once protected the extended memory block cannot be unprotected.

Once the extended memory block is programmed, the Exit Extended Memory Block command must be issued to exit the extended memory block mode and return the device to read mode.

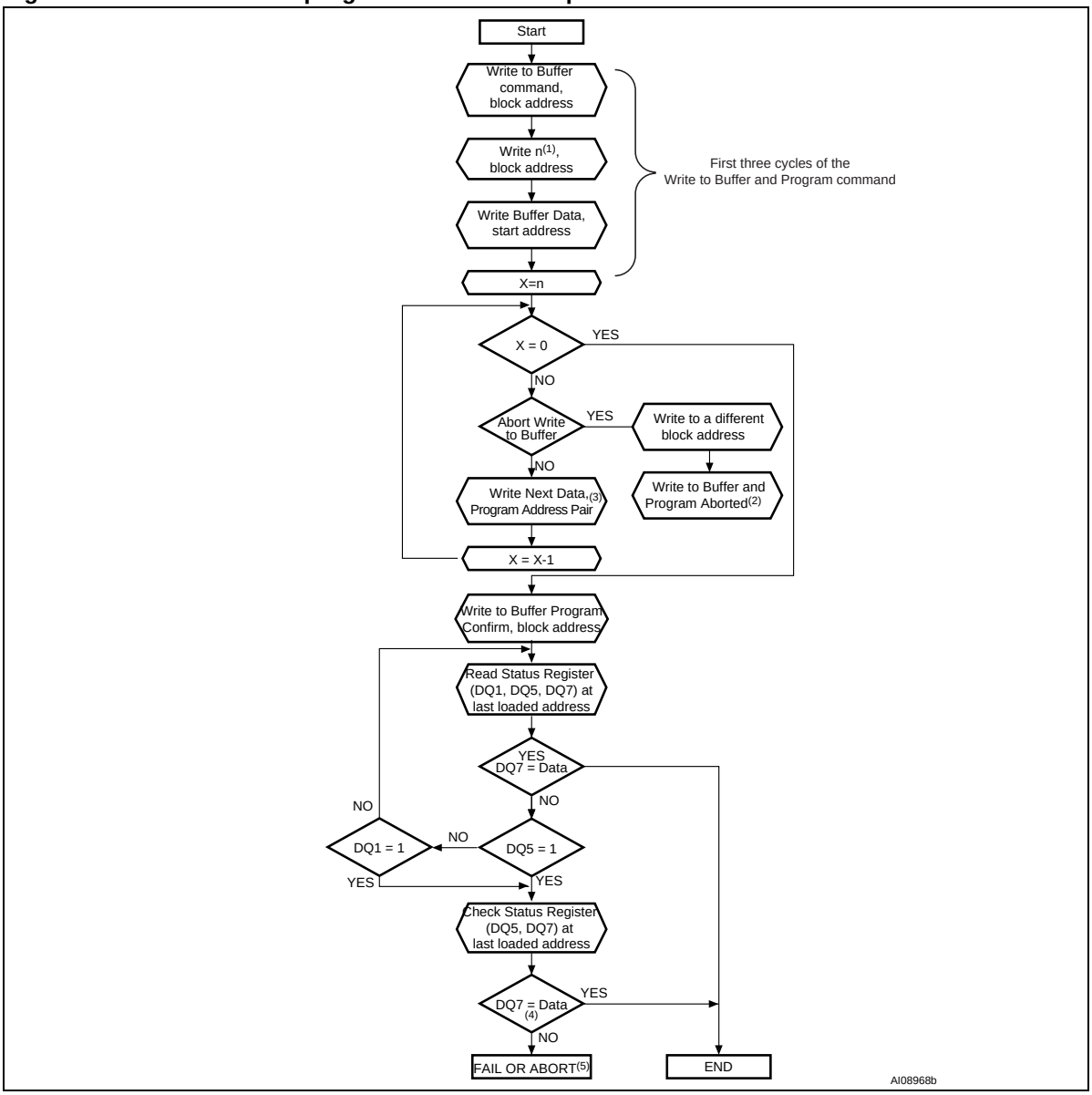
Table 45. Extended memory block address and data

Address(1)		Data	
x8	**x16**	**Factory locked**	**Customer lockable**
000000h-0000FFh	000000h-00007Fh	Security identification number	Determined by customer

1. See *Table 37: Block addresses 0 - 127* and *Table 38: Block addresses 128 - 255*.

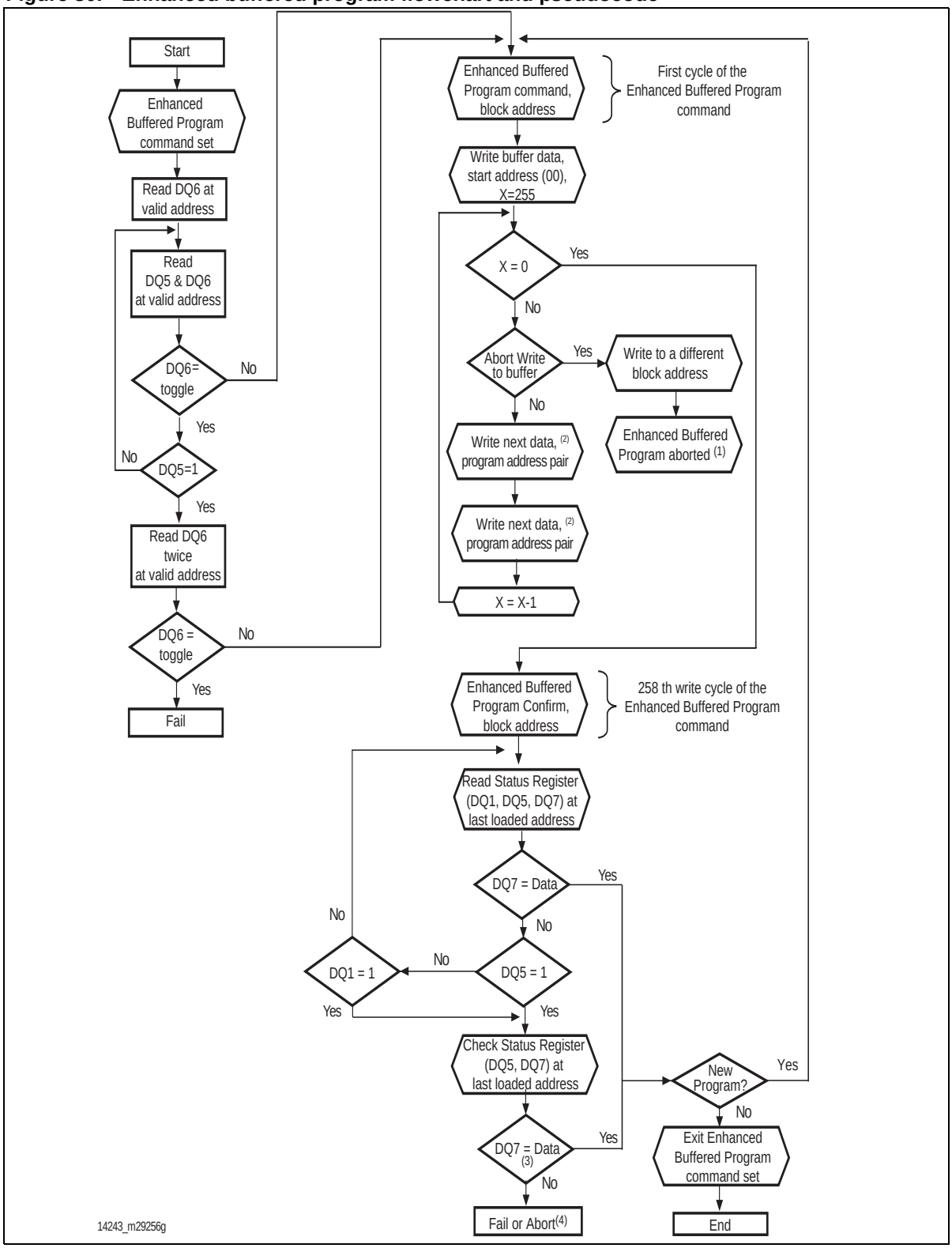
Appendix D Flowcharts

Figure 29. Write to buffer program flowchart and pseudocode



1. n+1 is the number of addresses to be programmed.
2. A write to buffer program abort and reset must be issued to return the device in read mode.
3. When the block address is specified, any address in the selected block address space is acceptable. However when loading write buffer address with data, all addresses must fall within the selected write buffer page.
4. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
5. If this flowchart location is reached because DQ5='1', then the Write to Buffer Program command failed. If this flowchart location is reached because DQ1='1', then the Write to Buffer Program command aborted. In both cases, the appropriate reset command must be issued to return the device in read mode: a Reset command if the operation failed, a Write to Buffer Program Abort and Reset command if the operation aborted.
6. See *Table 12* and *Table 13*, for details on Write to Buffer Program command sequence.

Figure 30. Enhanced buffered program flowchart and pseudocode



1. An Enhanced buffered program abort reset command must be issued to return the device in read mode.

2. When the block address is specified, all the addresses in the selected block address space must be issued starting from (00). Furthermore, when loading write buffer address with data, data program addresses must be consecutive.
3. DQ7 must be checked since DQ5 and DQ7 may change simultaneously.
4. If this flowchart location is reached because DQ5='1', then the Enhanced Buffered Program command failed. If this flowchart location is reached because DQ1='1', then the Enhanced Buffered Program command aborted. In both cases, the appropriate reset command must be issued to return the device in read mode: a Reset command if the operation failed, a Buffered Program Abort and Reset command if the operation aborted.
5. See *Table 18: Enhanced buffered program commands, 16-bit mode*, for details on Enhanced Buffered Program command sequence.

12 Revision history

Table 46. Document revision history

Date	Version	Changes
24-Nov-2008	01	Initial release.
25-March-2009	02	Revised data in the following tables: – *Table 21: Program/erase times and program/erase endurance cycles*; – *Table 27: DC characteristics*; – *Table 28: Read AC characteristics*; – *Table 29: Write AC characteristics, write enable controlled*; – *Table 30: Write AC characteristics, chip enable controlled*; – *Table 31: Reset AC characteristics*. – *Table 36.: Ordering information scheme*: corrected product order information size from 128-Mbit to 256-Mbit.
20-May-2009	03	Corrected address ranges in *Figure 4.: Block addresses*; Revised values for the following parameters in the *Table 28.: Read AC characteristics*: – tAVQV1 60, 70, and 80 ns AC Read Characteristics data from from 20, 20, and 25 ns to 25, 25, and 30 ns, respectively; – tGLQV 60, 70, and 80 ns AC Read Characteristics data from 20, 20, and 25 ns to to 25, 25, and 30 ns respectively; – tEHQz and tGHQZ, 60, 70, and 80 ns: from 20, 20, and 20 ns to 25, 25, and 30 ns, respectively; – tBLQZ 80 ns from 25 to 30 ns. Added table heading to *Table 38.: Block addresses 128 - 255*.
19-June-2009	04	Changed LBGA to FBGA (package name change)
19-January-2010	05	In *Table 21.: Program/erase times and program/erase endurance cycles*, changed Erase Suspend Latency time from 35 µs to 45 µs.

Please Read Carefully: