LTC4007

4A, High Efficiency, Standalone Li-Ion Battery Charger

FEATURES

- **Complete Charger Controller for 3- or 4-Cell Lithium-Ion Batteries**
- **High Conversion Efficiency: Up to 96%**
- **Output Currents Exceeding 4A**
- **±0.8% Charging Voltage Accuracy**
- **Built-In Charge Termination for Li-Ion Batteries**
- **AC Adapter Current Limiting Maximizes Charge Rate***
- Thermistor Input for Temperature Qualified Charging
- Wide Input Voltage Range: 6V to 28V
- 0.5V Dropout Voltage; Maximum Duty Cycle: 98%
- Programmable Charge Current: ±4% Accuracy
- Indicator Outputs for Charging, C/10 Current Detection, AC Adapter Present, Low Battery, Input Current Limiting and Faults
- Charging Current Monitor Output
- Available in a 24-Pin Narrow SSOP Package

APPLICATIONS

- Notebook Computers
- Portable Instruments
- Battery-Backup Systems
- Standalone Li-Ion Chargers

DESCRIPTION

The LTC®4007 is a complete constant-current/constant-voltage charger controller for 3- or 4-cell lithium-ion batteries. The PWM controller uses a synchronous, quasi-constant frequency, constant off-time architecture that will not generate audible noise even when using ceramic capacitors. Charging current is programmable to ±4% accuracy using a programming resistor. Charging current can also be monitored as a voltage across the programming resistor.

The output float voltage is pin programmed for cell count (3 cells or 4 cells) and chemistry (4.2V/4.1V). A timer, programmed by an external resistor, sets the charge termination time. Charging is automatically restarted when cell voltage falls below 3.9V/cell.

LTC4007 includes a thermistor input, which suspends charging if an unsafe temperature condition is detected. If the cell voltage is less than 2.5V, a low-battery indicator asserts and can be used to program a trickle charge current to safely charge depleted batteries. The $\overline{\text{FAULT}}$ pin is also asserted and charging terminates if the low-battery condition persists for more than 1/4 of the total charge time.

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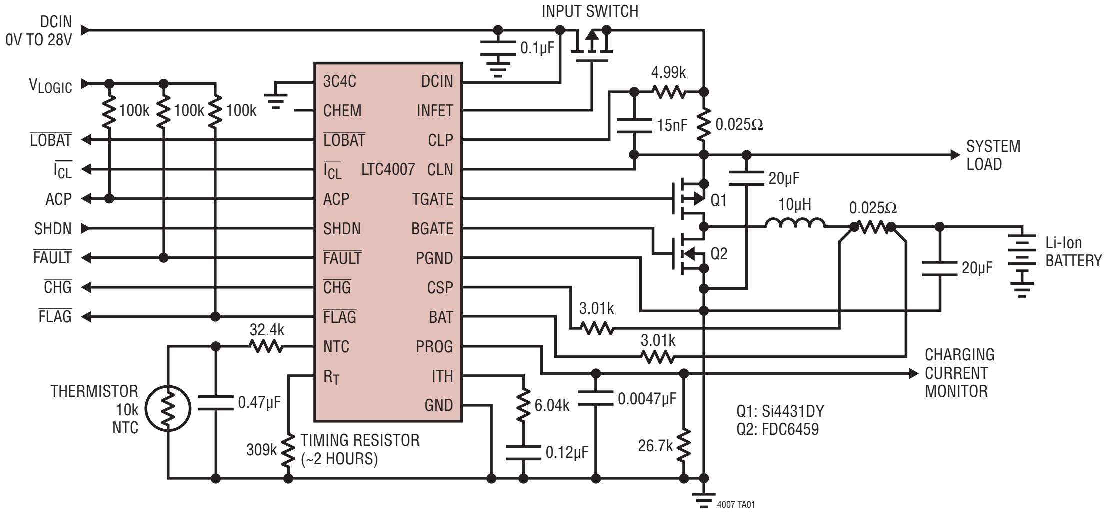
TYPICAL APPLICATION

12.6V, 4A Li-Ion Battery Charger

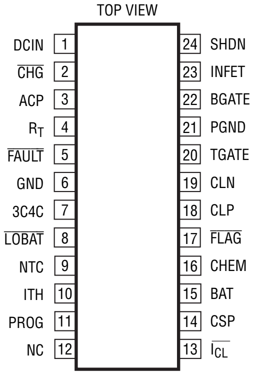


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Voltage from DCIN, CLP, CLN to GND.......... +32V/–0.3V
PGND with Respect to GND .... ±0.3V
CSP, BAT to GND .... +28V/–0.3V
CHEM, 3C4C, R_T to GND .... +7V/–0.3V
NTC .... +10V/–0.3V
ACP, SHDN, $\overline{\text{CHG}}$, $\overline{\text{FLAG}}$,
$\overline{\text{FAULT}}$, $\overline{\text{LOBAT}}$, I_{CL} .... +32V/–0.3V
CLP to CLN ....±0.5V
Operating Ambient Temperature Range
(Note 4) .... –40°C to 85°C
Operating Junction Temperature .... –40°C to 125°C
Storage Temperature Range...................–65°C to 150°C
Lead Temperature (Soldering, 10 sec) .... 300°C

PIN CONFIGURATION



GN PACKAGE
24-LEAD PLASTIC SSOP

$T_{JMAX} = 125°C, \theta_{JA} = 90°C/W$

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4007EGN#PBF	LTC4007EGN#TRPBF	LTC4007EGN	24-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at $T_A = 25°C$. $V_{DCIN} = 20V$, $V_{BAT} = 12V$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	DCIN Operating Range			6		28	V
I_Q	Operating Current	Sum of Current from CLP, CLN , DCIN			3	5	mA
V_{TOL}	Charge Voltage Accuracy	Nominal Values: 12.3V, 12.6V, 16.4V, 16.8V (Note 2)	 ●	–0.8 –1.0		0.8 1.0	% %
I_{TOL}	Charge Current Accuracy (Note 3)	$V_{CSP} – V_{BAT}$ Target = 100mV $V_{BAT} < 6V$, $V_{CSP} – V_{BAT}$ Target = 10mV $6V \le V_{BAT} \le V_{LOBAT}$, $V_{CSP} – V_{BAT}$ Target = 10mV	 ●	–4 –5 –60 –35		4 5 60 35	% % % %
T_{TOL}	Termination Timer Accuracy	$R_{RT} = 270k$	●	–15		15	%
Shutdown							
	Battery Leakage Current	DCIN = 0V SHDN = 3V	● ●	 –10	15	35 10	µA µA
UVLO	Undervoltage Lockout Threshold	DCIN Rising, $V_{BAT} = 0$	●	4.2	4.7	5.5	V
	Shutdown Threshold at SHDN		●	1	1.6	2.5	V
	SHDN Pin Current				–10		µA
	Operating Current in Shutdown	$V_{SHDN} = 0V$, Sum of Current from CLP, CLN, DCIN			2	3	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense Amplifier, CA1							
	Input Bias Current Into BAT Pin				11.67		µA
CMSL	CA1/I_1 Input Common Mode Low		●	0			V
CMSH	CA1/I_1 Input Common Mode High		●			V_{CLN} – 0.2	V
Current Comparators I_{CMP} and I_{REV}							
I_{TMAX}	Maximum Current Sense Threshold (V_{CSP} – V_{BAT})	V_{ITH} = 2.5V	●	140	165	200	mV
I_{TREV}	Reverse Current Threshold (V_{CSP} – V_{BAT})				–30		mV
Current Sense Amplifier, CA2							
	Transconductance				1		mmho
	Source Current	Measured at I_{TH}, V_{ITH} = 1.4V			–40		µA
	Sink Current	Measured at I_{TH}, V_{ITH} = 1.4V			40		µA
Current Limit Amplifier							
	Transconductance				1.4		mmho
V_{CLP}	Current Limit Threshold		●	93	100	107	mV
I_{CLP}	CLP Input Bias Current				100		nA
Voltage Error Amplifier, EA							
	Transconductance				1		mmho
	Sink Current	Measured at I_{TH}, V_{ITH} = 1.4V			36		µA
OVSD	Overvoltage Shutdown Threshold as a Percent of Programmed Charger Voltage		●	102	107	110	%
Input P-Channel FET Driver (INFET)							
	DCIN Detection Threshold (V_{DCIN} – V_{CLN})	DCIN Voltage Ramping Up from V_{CLN} – 0.1V	●	0	0.17	0.25	V
	Forward Regulation Voltage (V_{DCIN} – V_{CLN})		●		25	50	mV
	Reverse Voltage Turn-Off Voltage (V_{DCIN} – V_{CLN})	DCIN Voltage Ramping Down	●	–60	–25		mV
	INFET "On" Clamping Voltage (V_{DCIN} – V_{INFET})	I_{INFET} = 1µA	●	5	5.8	6.5	V
	INFET "Off" Clamping Voltage (V_{DCIN} – V_{INFET})	I_{INFET} = –25µA				0.25	V
Thermistor							
NTCVR	Reference Voltage During Sample Time				4.5		V
	High Threshold	V_{NTC} Rising	●	NTCVR • 0.48	NTCVR • 0.5	NTCVR • 0.52	V
	Low Threshold	V_{NTC} Falling	●	NTCVR • 0.115	NTCVR • 0.125	NTCVR • 0.135	V
	Thermistor Disable Current	V_{NTC} ≤ 10V				10	µA
Indicator Outputs (ACP, $\overline{\text{CHG}}$, $\overline{\text{FLAG}}$, $\overline{\text{LOBAT}}$, $\overline{I_{CL}}$, $\overline{\text{FAULT}}$							
C10TOL	$\overline{\text{FLAG}}$ (C/10) Accuracy	Voltage Falling at PROG	●	0.375	0.397	0.420	V
LBTOL	$\overline{\text{LOBAT}}$ Threshold Accuracy	3C4C = 0V, CHEM = 0V	●	7.10	7.32	7.52	V
		3C4C = 0V, CHEM = Open	●	7.27	7.50	7.71	V
		3C4C = Open, CHEM = 0V	●	9.46	9.76	10.10	V
		3C4C = Open, CHEM = Open	●	9.70	10	10.28	V
	RESTART Threshold Accuracy	3C4C = 0V, CHEM = 0V	●	11.13	11.42	11.65	V
		3C4C = 0V, CHEM = Open	●	11.40	11.70	11.94	V
		3C4C = Open, CHEM = 0V	●	14.84	15.23	15.54	V
		3C4C = Open, CHEM = Open	●	15.20	15.60	15.92	V
	$\overline{I_{CL}}$ Threshold Accuracy			83	93	105	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range (Note 4), otherwise specifications are at T_A = 25°C. V_{DCIN} = 20V, V_{BAT} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OL}	Low Logic Level of ACP, $\overline{CHG}$, $\overline{FLAG}$, $\overline{LOBAT}$, $\overline{I_{CL}}$, $\overline{FAULT}$	I_{OL} = 100µA	●			0.5	V
V_{OH}	High Logic Level of $\overline{CHG}$, $\overline{LOBAT}$, $\overline{I_{CL}}$	I_{OH} = –1µA	●	2.7			V
I_{OFF}	Off State Leakage Current of ACP, $\overline{FLAG}$, $\overline{FAULT}$	V_{OH} = 3V		–1		1	µA
I_{PO}	Pull-Up Current on $\overline{CHG}$, $\overline{LOBAT}$, $\overline{I_{CL}}$	V = 0V			–10		µA
	Charge Termination Defeat Threshold at CHG			1			V
Programming Inputs (CHEM and 3C4C)							
V_{IH}	High Logic Level		●			3.3	V
V_{IL}	Low Logic Level		●	1			V
I_{PI}	Pull-Up Current	V = 0V			–14		µA
Oscillator							
f_{OSC}	Regulator Switching Frequency			255	300	345	kHz
f_{MIN}	Regulator Switching Frequency in Drop Out	Duty Cycle ≥ 98%		20	25		kHz
DC_{MAX}	Regulator Maximum Duty Cycle	V_{CSP} = V_{BAT}		98	99		%
Gate Drivers (TGATE, BGATE)							
	V_{TGATE} High (V_{CLN} – V_{TGATE})	I_{TGATE} = –1mA				50	mV
	V_{BGATE} High	C_{LOAD} = 3000pF		4.5	5.6	10	V
	V_{TGATE} Low (V_{CLN} – V_{TGATE})	C_{LOAD} = 3000pF		4.5	5.6	10	V
	V_{BGATE} Low	I_{BGATE} = 1mA				50	mV
 TGTR TGTF	TGATE Transition Time TGATE Rise Time TGATE Fall Time	 C_{LOAD} = 3000pF, 10% to 90% C_{LOAD} = 3000pF, 10% to 90%			 50 50	 110 100	 ns ns
 BGTR BGTF	BGATE Transition Time BGATE Rise Time BGATE Fall Time	 C_{LOAD} = 3000pF, 10% to 90% C_{LOAD} = 3000pF, 10% to 90%			 40 40	 90 80	 ns ns
	V_{TGATE} at Shutdown (V_{CLN} – V_{TGATE})	I_{TGATE} = –1µA, DCIN = 0V, CLN = 12V				100	mV
	V_{BGATE} at Shutdown	I_{BGATE} = 1µA, DCIN = 0V, CLN = 12V				100	mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

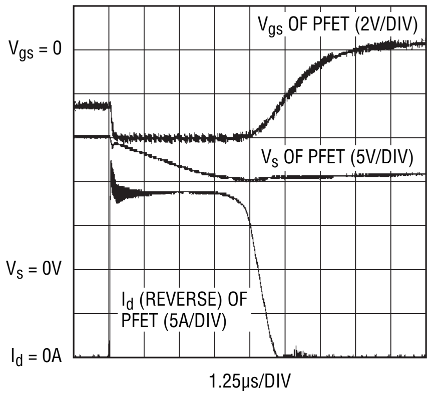
Note 2: See Test Circuit.

Note 3: Does not include tolerance of current sense resistor or current programming resistor.

Note 4: The LTC4007E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls.

TYPICAL PERFORMANCE CHARACTERISTICS

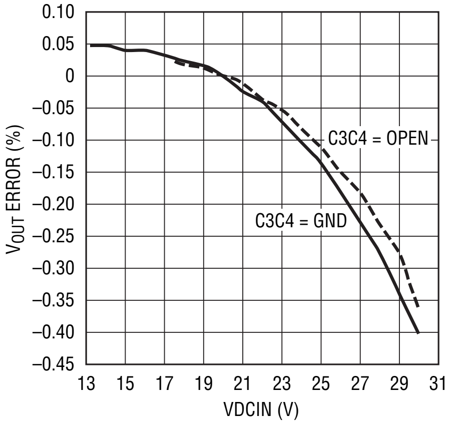
INFET Response Time to Reverse Current



TEST PERFORMED ON DEMOBOARD
V_{IN} = 15VDC　V_{CHARGE} = 12.6V
CHARGER = ON　PFET = 1/2 Si4925DY
I_{CHARGE} = <10mA

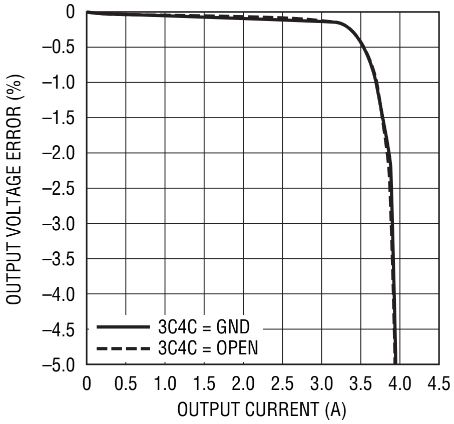
4007 G01

Line Regulation



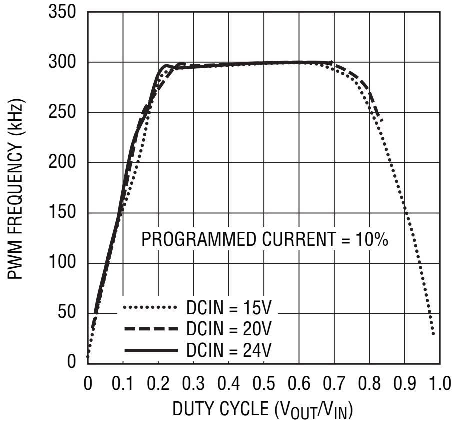
4007 G02

V_{OUT} vs I_{OUT}



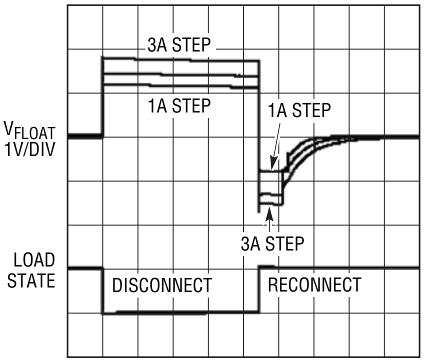
4007 G03

PWM Frequency vs Duty Cycle



4007 G04

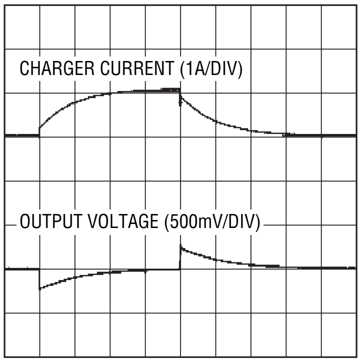
Disconnect/Reconnect Battery (Load Dump)



LOAD CURRENT = 1A, 2A, 3A
DCIN = 20V
V_{FLOAT} = 12.6V (3C4C = GND, CHEM = OPEN)

4007 G05

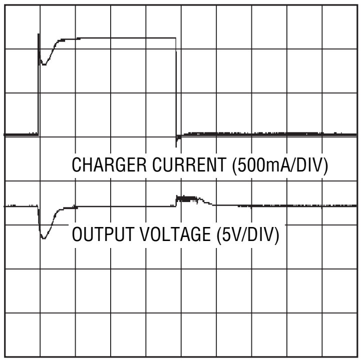
1A Load Step (Battery Present)



DCIN = 20V
V_{FLOAT} = 12.6V

4007 G06

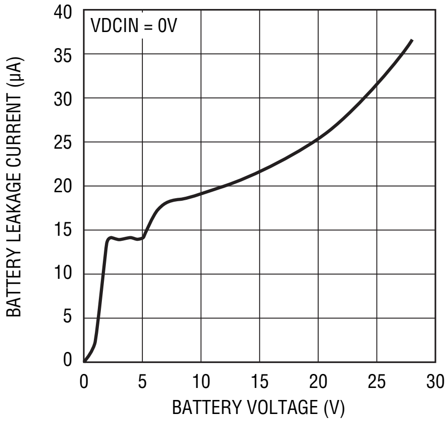
1A Load Step (Battery Not Present)



DCIN = 20V
V_{FLOAT} = 12.6V

4007 G07

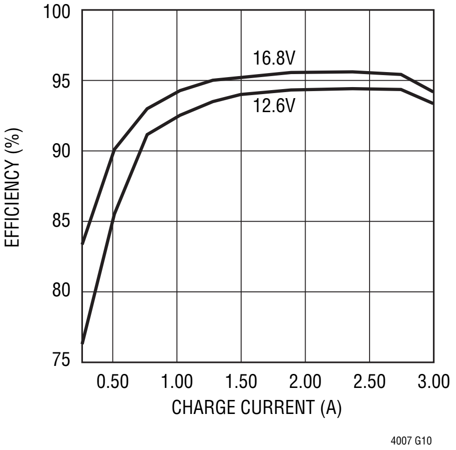
Battery Leakage Current vs Battery Voltage



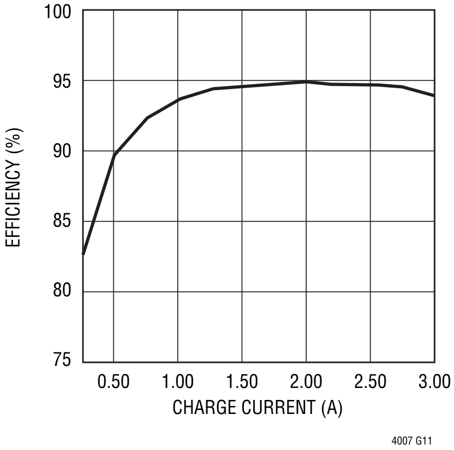
4007 G08

TYPICAL PERFORMANCE CHARACTERISTICS

Efficiency at 19VDC V_{IN}



Efficiency at 12.6V with 15VDC V_{IN}



PIN FUNCTIONS

DCIN (Pin 1): External DC Power Source Input. Bypass this pin with at least 0.01µF. See Applications Information.

$\overline{\text{CHG}}$ (Pin 2): Charge Status Output. When the battery is being charged, the $\overline{\text{CHG}}$ pin is pulled low by an internal N-channel MOSFET. Internal 10µA pull-up to 3.5V. If V_{LOGIC} is greater than 3.3V, add an external pull-up. The timer charge termination can be defeated by forcing this pin below 1V (or connecting it to GND).

ACP (Pin 3): Open-Drain output to indicate if the AC adapter voltage is adequate for charging. This pin is pulled low by an internal N-channel MOSFET if DCIN is below BAT. A pull-up resistor is required. The pin is capable of sinking at least 100µA.

R_T (Pin 4): Timer Resistor. The timer period is set by placing a resistor, R_{RT}, to GND. This resistor is always required.

The timer period is t_{TIMER} = (1hour • R_{RT}/154K).

If this resistor is not present, the charger will not start.

$\overline{\text{FAULT}}$ (Pin 5): Active low open-drain output that indicates charger operation has stopped due to a low-battery conditioning error, or that charger operation is suspended due to the thermistor exceeding allowed values. A pull-up resistor is required if this function is used. The pin is capable of sinking at least 100µA.

GND (Pin 6): Ground for Low Power Circuitry.

3C4C (Pin 7): Select 3-cell or 4-cell float voltage by connecting this pin to GND or open, respectively. Internal 14µA pull-up to 5.3V. This pin can also be driven with open-collector/drain logic levels. High: 4 cell. Low: 3 cell.

$\overline{\text{LOBAT}}$ (Pin 8): Low-Battery Indicator. Active low digital output. Internal 10µA pull-up to 3.5V. If the battery voltage is below 2.5V/cell (or 2.44V/cell for 4.1V chemistry batteries) $\overline{\text{LOBAT}}$ will be low. The pin is capable of sinking at least 100µA. If V_{LOGIC} is greater than 3.3V, add an external pull-up.

NTC (Pin 9): A thermistor network is connected from NTC to GND. This pin determines if the battery temperature is safe for charging. The charger and timer are suspended and the $\overline{\text{FAULT}}$ pin is driven low if the thermistor indicates a temperature that is unsafe for charging. The thermistor function may be disabled with a 300k to 500k resistor from DCIN to NTC.

PIN FUNCTIONS

ITH (Pin 10): Control Signal of the Inner Loop of the Current Mode PWM. Higher ITH voltage corresponds to higher charging current in normal operation. A 6k resistor, in series with a capacitor of at least 0.1µF to GND provides loop compensation. Typical full-scale output current is 40µA. Nominal voltage range for this pin is 0V to 3V.

PROG (Pin 11): Current Programming/Monitoring Input/Output. An external resistor to GND programs the peak charging current in conjunction with the current sensing resistor. The voltage at this pin provides a linear indication of charging current. Peak current is equivalent to 1.19V. Zero current is approximately 0.3V. A capacitor from PROG to ground is required to filter higher frequency components. The maximum resistance to ground is 100k. Values higher than 100k can cause the charger to shut down.

NC (Pin 12): No Connect.

$\overline{I_{CL}}$ (Pin 13): Input Current Limit Indicator. Active low digital output. Internal 10µA pull-up to 3.5V. Pulled low if the charger current is being reduced by the input current limiting function. The pin is capable of sinking at least 100µA. If V_{LOGIC} is greater than 3.3V, add an external pull-up.

CSP (Pin 14): Current Amplifier CA1 Input. The CSP and BAT pins measure the voltage across the sense resistor, R_{SENSE}, to provide the instantaneous current signals required for both peak and average current mode operation.

BAT (Pin 15): Battery Sense Input and the Negative Reference for the Current Sense Resistor. A precision internal resistor divider sets the final float potential on this pin. The resistor divider is disconnected during shutdown.

CHEM (Pin 16): Select 4.1V or 4.2V cell chemistry by connecting the pin to GND or open, respectively. Internal 14µA pull-up to 5.3V. Can also be driven with open-collector/drain logic levels.

$\overline{\text{FLAG}}$ (Pin 17): Active low open-drain output that indicates when charging current has declined to 10% of maximum programmed current. A pull-up resistor is required if this function is used. The pin is capable of sinking at least 100µA.

CLP (Pin 18): Positive input to the supply current limiting amplifier, CL1. The threshold is set at 100mV above the voltage at the CLN pin. When used to limit supply current, a filter is needed to filter out the switching noise. If no current limit function is desired, connect this pin to CLN.

CLN (Pin 19): Negative Reference for the Input Current Limit Amplifier, CL1. This pin also serves as the power supply for the IC. A 10µF to 22µF bypass capacitor should be connected as close as possible to this pin.

TGATE (Pin 20): Drives the top external P-channel MOSFET of the battery charger buck converter.

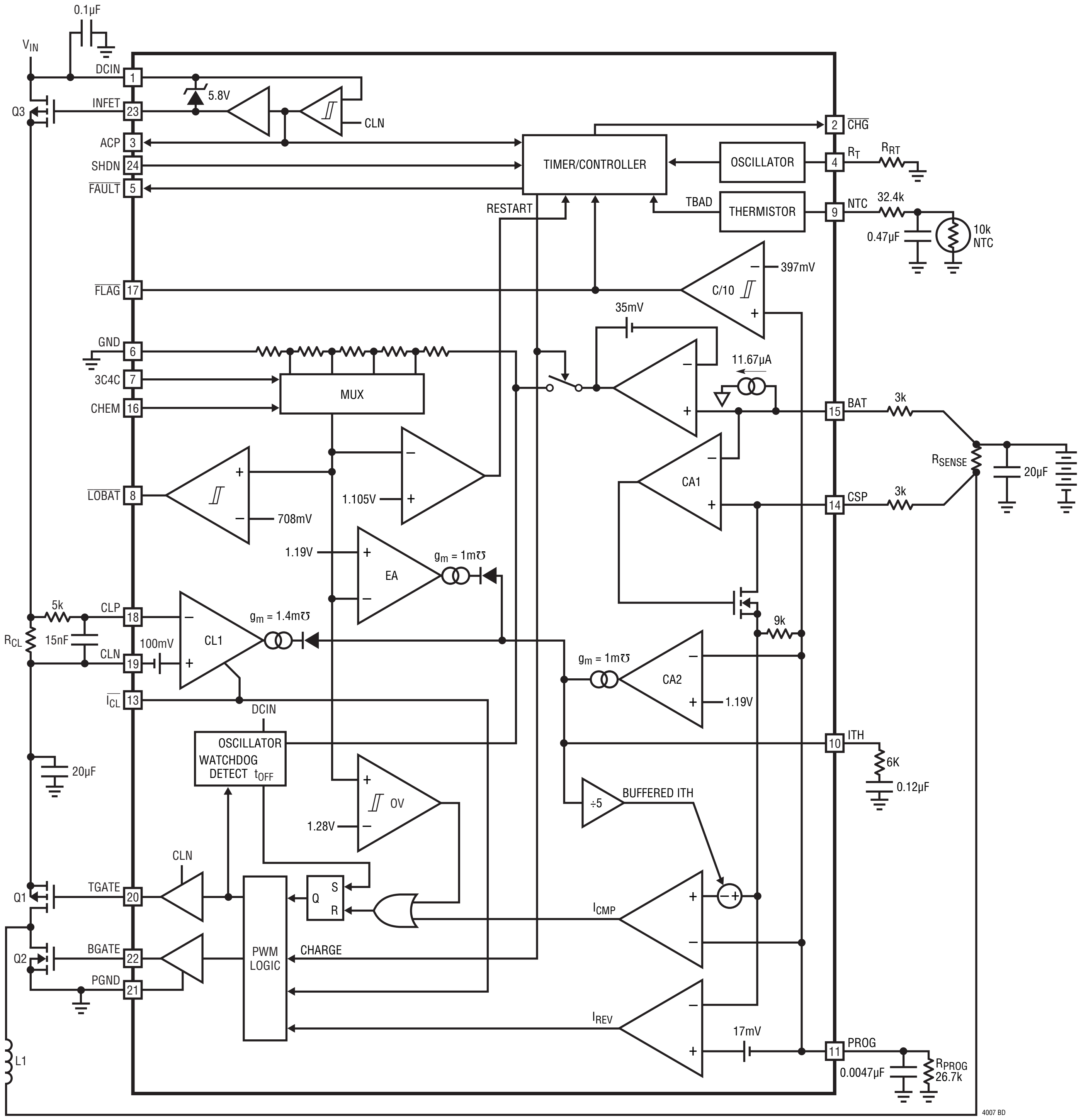
PGND (Pin 21): High Current Ground Return for the BGATE Driver.

BGATE (Pin 22): Drives the bottom external N-channel MOSFET of the battery charger buck converter.

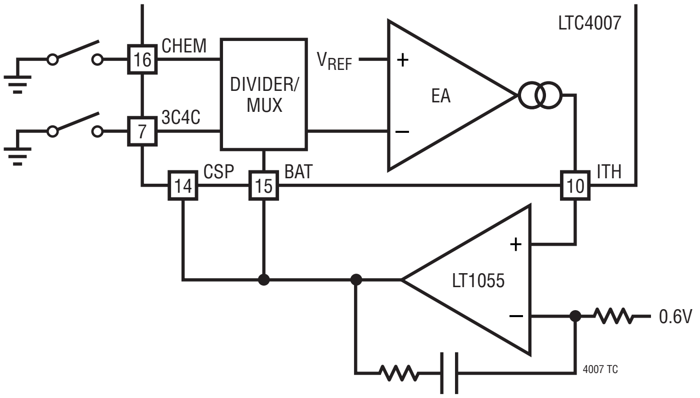
INFET (Pin 23): Drives the Gate of the External Input PFET.

SHDN (Pin 24):
Charger is shut down and timer is reset when this pin is HIGH. Internal 10µA pull-up to 3.5V. This pin can also be used to reset the charger by applying a positive pulse that is a minimum of 0.1µs long.

BLOCK DIAGRAM



TEST CIRCUIT



OPERATION

Overview

The LTC4007 is a synchronous current mode PWM step-down (buck) switcher battery charger controller. The charge current is programmed by the combination of a program resistor (R_{PROG}) from the PROG pin to ground and a sense resistor (R_{SENSE}) between the CSP and BAT pins. The final float voltage is programmed to one of four values (12.3V, 12.6V, 16.4V, 16.8V) with ±1% maximum accuracy using pins 3C4C and CHEM. Charging begins when the potential at the DCIN pin rises above the voltage at BAT (and the UVLO voltage) and the SHDN pin is low; the $\overline{\text{CHG}}$ pin is set low. At the beginning of the charge cycle, if the cell voltage is below 2.5V (2.44V if CHEM is low), the $\overline{\text{LOBAT}}$ pin will be low. The $\overline{\text{LOBAT}}$ indicator can be used to reduce the charging current to a low value, typically 10% of full scale. If the cell voltage stays below 2.5V for 25% of the total charge time, the charge sequence will be terminated immediately and the $\overline{\text{FAULT}}$ pin will be set low.

An external thermistor network is sampled at regular intervals. If the thermistor value exceeds design limits, charging is suspended and the $\overline{\text{FAULT}}$ pin is set low. If the thermistor value returns to an acceptable value, charging resumes and the $\overline{\text{FAULT}}$ pin is set high. An external resistor on the R_T pin sets the charge termination time. Charge termination can be defeated by forcing the $\overline{\text{CHG}}$ pin to a low voltage.

As the battery approaches the final float voltage, the charge current will begin to decrease. When the current drops to 10% of the full-scale charge current, an internal C/10 comparator will indicate this condition by latching the $\overline{\text{FLAG}}$ pin low. The charge timer is also reset to 1/4 of the total charge time when $\overline{\text{FLAG}}$ goes low. If this condition is caused by an input current limit condition, described below, then the $\overline{\text{FLAG}}$ indicator will be inhibited. When a time-out occurs, charging is terminated immediately and the $\overline{\text{CHG}}$ pin is forced to a high impedance state. The charger will automatically restart if the cell voltage is below 3.9V (or 3.81V if CHEM is low). To restart the charge cycle manually, simply remove the input voltage and reapply it, or set the SHDN pin high momentarily. When the input voltage is not present, the charger goes into a sleep mode, dropping battery current drain to 15μA. This greatly reduces the current drain on the battery and increases the standby time. The charger is inhibited any time the SHDN pin is high.

Input FET

The input FET circuit performs two functions. It enables the charger if the input voltage is higher than the CLN pin and provides the logic indicator of AC present on the ACP pin. It controls the gate of the input FET to keep a low forward voltage drop when charging and also prevents reverse current flow through the input FET.

If the input voltage is less than V_{CLN}, it must go at least 170mV higher than V_{CLN} to activate the charger. When this occurs the ACP pin is released and pulled up with an external load to indicate that the adapter is present. The gate of the input FET is driven to a voltage sufficient to

OPERATION

Table 1. Truth Table For Indicator States

MODE	DCIN	SHDN	ACP**	$\overline{\text{LOBAT}}$	$\overline{\text{FLAG}}$**	$\overline{\text{FAULT}}$**	$\overline{\text{I}_{\text{CL}}}$	TIMER STATE	$\overline{\text{CHG}}$**
Shut down by low adapter voltage	<BAT	LOW	LOW	LOW	HIGH	HIGH	LOW	Reset	HIGH
Charging a low bat	>BAT	LOW	HIGH	LOW	HIGH*	HIGH*	HIGH*	Running	LOW
Normal charging	>BAT	LOW	HIGH	HIGH	HIGH	HIGH*	HIGH*	Running	LOW
Input current limited charging	>BAT	LOW	HIGH	HIGH	HIGH*	HIGH*	LOW	Running	LOW
Charger paused due to thermistor out of range	>BAT	LOW	HIGH	X	X	LOW (from NTC)	HIGH	Paused	LOW
Shut down by SHDN pin	X	HIGH	X	X	HIGH	HIGH	LOW	Reset	HIGH
Terminated by low-battery fault (Note 1)	>BAT	LOW	HIGH	LOW	HIGH*	LOW	LOW	>T/4	HIGH (Faulted)
Timer is reset when $\overline{\text{FLAG}}$ goes low, then terminates after 1/4 T	>BAT	LOW	HIGH	HIGH	LOW	HIGH	LOW	>T/4 after FLAG = LOW	HIGH (Waiting for Restart
Terminated by expired timer	>BAT	LOW	HIGH	HIGH	HIGH	HIGH	LOW	>T	HIGH (Waiting for Restart
Charge termination defeated	X	X	X	X	X	X	X	X	Forced LOW
Shut down by undervoltage lockout	>BAT + <UVL	LOW	HIGH	HIGH	HIGH	HIGH*	LOW	Reset	HIGH*

*Most probable condition X = Don't care, ** Open-drain output HIGH = OPEN with pull-up

Note 1: If a depleted battery is inserted while the charger is in this state, the charger must be reset to initiate charging.

keep a low forward voltage drop from drain to source. If the voltage between DCIN and CLN drops to less than 25mV, the input FET is turned off slowly. If the voltage between DCIN and CLN is ever less than –25mV, then the input FET is turned off in less than 10µs to prevent significant reverse current from flowing in the input FET. In this condition, the ACP pin is driven low and the charger is disabled.

Battery Charger Controller

The LTC4007 charger controller uses a constant off-time, current mode step-down architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the SR latch and turned off when the main current comparator I_{CMP} resets the SR latch. While the top MOSFET is off, the bottom MOSFET is turned on until either the inductor current trips the current comparator I_{REV} or the beginning of the next cycle. The oscillator uses the equation:

$$t_{OFF} = \frac{V_{DCIN} - V_{BAT}}{V_{DCIN} \bullet f_{OSC}}$$

to set the bottom MOSFET on time. The result is a nearly constant switching frequency over a wide input/output voltage range. This activity is diagrammed in Figure 1.

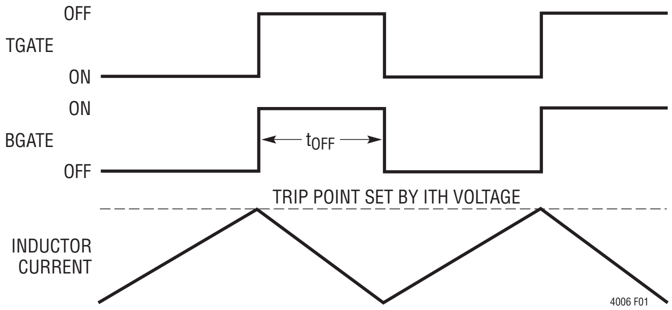


Figure 1

OPERATION

The peak inductor current, at which I_{CMP} resets the SR latch, is controlled by the voltage on ITH. ITH is in turn controlled by several loops, depending upon the situation at hand. The average current control loop converts the voltage between CSP and BAT to a representative current. Error amp CA2 compares this current against the desired current programmed by RPROG at the PROG pin and adjusts ITH until:

$$\frac{V_{REF}}{R_{PROG}} = \frac{V_{CSP} - V_{BAT} + 11.67\mu A \bullet 3.01k\Omega}{3.01k\Omega}$$

therefore,

$$I_{CHARGE(MAX)} = \left(\frac{V_{REF}}{R_{PROG}} - 11.67\mu A\right) \bullet \frac{3.01k\Omega}{R_{SENSE}}$$

The voltage at BAT is divided down by an internal resistor divider and is used by error amp EA to decrease ITH if the divider voltage is above the 1.19V reference. When the charging current begins to decrease, the voltage at PROG will decrease in direct proportion. The voltage at PROG is then given by:

$$V_{PROG} = (I_{CHARGE} \bullet R_{SENSE} + 11.67\mu A \bullet 3.01k\Omega) \bullet \frac{R_{PROG}}{3.01k\Omega}$$

V_{PROG} is plotted in Figure 2.

The amplifier CL1 monitors and limits the input current, normally from the AC adapter to a preset level ($100mV/R_{CL}$). At input current limit, CL1 will decrease the ITH voltage, thereby reducing charging current. The $\overline{I_{CL}}$ indicator output will go low when this condition is detected and the $\overline{FLAG}$ indicator will be inhibited if it is not already LOW.

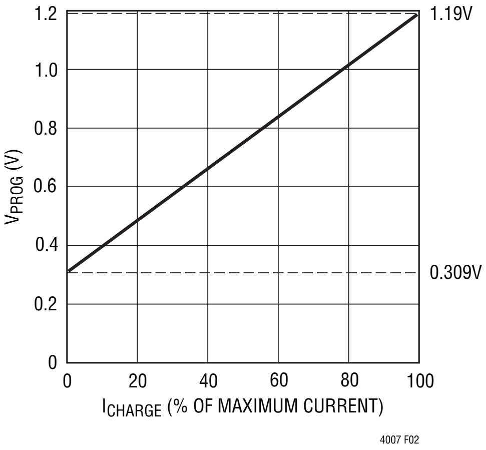


Figure 2. V_{PROG} vs I_{CHARGE}

If the charging current decreases below 10% to 15% of programmed current while engaged in input current limiting, BGATE will be forced low to prevent the charger from discharging the battery. Audible noise can occur in this mode of operation.

An overvoltage comparator guards against voltage transient overshoots (>7% of programmed value). In this case, both MOSFETs are turned off until the overvoltage condition is cleared. This feature is useful for batteries which "load dump" themselves by opening their protection switch to perform functions such as calibration or pulse mode charging.

PWM Watchdog Timer

There is a watchdog timer that observes the activity on the BGATE and TGATE pins. If TGATE stops switching for more than 40µs, the watchdog activates and turns off the top MOSFET for about 400ns. The watchdog engages to prevent very low frequency operation in dropout—a potential source of audible noise when using ceramic input and output capacitors.

Charger Start-Up

When the charger is enabled, it will not begin switching until the ITH voltage exceeds a threshold that assures initial current will be positive. This threshold is 5% to 15% of the maximum programmed current. After the charger begins switching, the various loops will control the current at a level that is higher or lower than the initial current. The duration of this transient condition depends upon the loop compensation, but is typically less than 100µs.

Thermistor Detection

The thermistor detection circuit is shown in Figure 3. It requires an external resistor and capacitor in order to function properly.

The thermistor detector performs a sample-and-hold function. An internal clock, whose frequency is determined

OPERATION

by the timing resistor connected to R_T, keeps switch S1 closed to sample the thermistor:

$t_{SAMPLE} = 127.5 \bullet 20 \bullet R_{RT} \bullet 17.5pF = 13.8ms,$

for $R_{RT} = 309k$

The external RC network is driven to approximately 4.5V and settles to a final value across the thermistor of:

$$V_{RTH(FINAL)} = \frac{4.5V \bullet R_{TH}}{R_{TH} + R9}$$

This voltage is stored by C7. Then the switch is opened for a short period of time to read the voltage across the thermistor.

$t_{HOLD} = 10 \bullet R_{RT} \bullet 17.5pF = 54\mu s,$

for $R_{RT} = 309k$

When the t_{HOLD} interval ends the result of the thermistor testing is stored in the D flip-flop (DFF). If the voltage at NTC is within the limits provided by the resistor divider feeding the comparators, then the NOR gate output will be low and the DFF will set T_{BAD} to zero and charging will continue. If the voltage at NTC is outside of the resistor divider limits, then the DFF will set T_{BAD} to one, the charger will be shut down, $\overline{FAULT}$ pin is set low and the timer will be suspended until T_{BAD} returns to zero (see Figure 4).

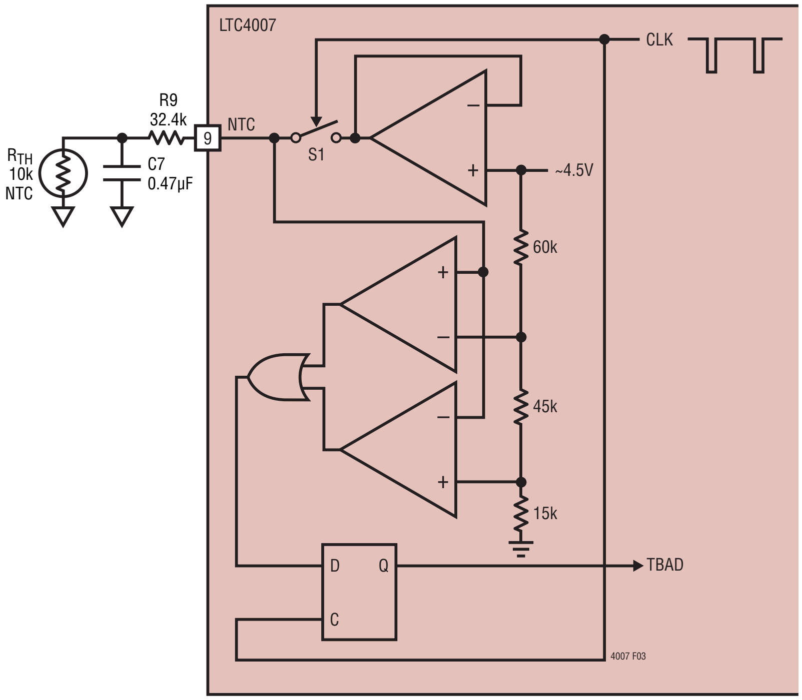


Figure 3

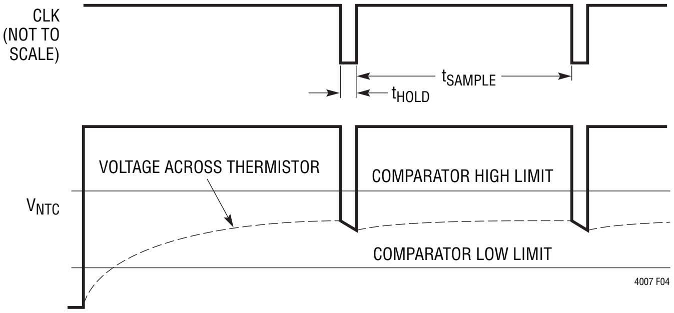


Figure 4

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Battery Detection

It is generally not good practice to connect a battery while the charger is running. The timer is in an unknown state and the charger could provide a large surge current into the battery for a brief time. The Figure 5 circuit keeps the charger shut down and the timer reset while a battery is not connected.

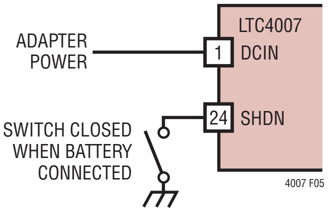

Figure 5

Charger Current Programming

The basic formula for charging current is:

$$I_{CHARGE(MAX)} = \frac{V_{REF} \bullet 3.01k\Omega / R_{PROG} - 0.035V}{R_{SENSE}}$$

$V_{REF} = 1.19V$

This leaves two degrees of freedom: R_{SENSE} and R_{PROG}. The 3.01k input resistors must not be altered since internal currents and voltages are trimmed for this value. Pick R_{SENSE} by setting the average voltage between C_{SP} and BAT to be close to 100mV during maximum charger current. Then R_{PROG} can be determined by solving the above equation for R_{PROG}.

$$R_{PROG} = \frac{V_{REF} \bullet 3.01k\Omega}{R_{SENSE} \bullet I_{CHARGE(MAX)} + 0.035V}$$

Table 2. Recommended R_{SNS} and R_{PROG} Resistor Values

I_{MAX} (A)	R_{SENSE} (Ω) 1%	R_{SENSE} (W)	R_{PROG} (kΩ) 1%
1.0	0.100	0.25	26.7
2.0	0.050	0.25	26.7
3.0	0.033	0.5	26.7
4.0	0.025	0.5	26.7

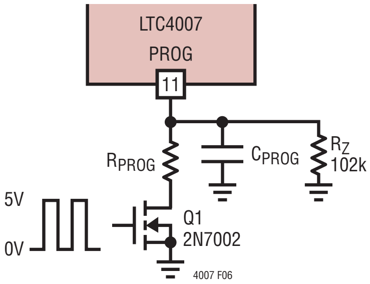

Figure 6. PWM Current Programming

Charging current can be programmed by pulse width modulating R_{PROG} with a switch Q1 to R_{PROG} at a frequency higher than a few kHz (Figure 6). C_{PROG} must be increased to reduce the ripple caused by the R_{PROG} switching. The compensation capacitor at ITH will probably need to be increased also to improve stability and prevent large overshoot currents during start-up conditions. Charging current will be proportional to the duty cycle of the switch with full current at 100% duty cycle and zero current when Q1 is off.

Maintaining C/10 Accuracy

The C/10 comparator threshold that drives the $\overline{\text{FLAG}}$ pin has a fixed threshold of approximately V_{PROG} = 400mV. This threshold works well when R_{PROG} is 26.7k, but will not yield a 10% charging current indication if R_{PROG} is a different value. There are situations where a standard value of R_{SENSE} will not allow the desired value of charging current when using the preferred R_{PROG} value. In these cases, where the full-scale voltage across R_{SENSE} is within ±20mV of the 100mV full-scale target, the input resistors connected to CSP and BAT can be adjusted to provide the desired maximum programming current as well as the correct $\overline{\text{FLAG}}$ trip point.

For example, the desired max charging current is 2.5A but the best R_{SENSE} value is 0.033Ω. In this case, the voltage across R_{SENSE} at maximum charging current is only 82.5mV, normally R_{PROG} would be 30.1k but the nominal $\overline{\text{FLAG}}$ trip point is only 5% of maximum charging current. If the input resistors are reduced by the same

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amount as the full-scale voltage is reduced then, R4 = R5 = 2.49k and R_{PROG} = 26.7k, the maximum charging current is still 2.5A but the $\overline{\text{FLAG}}$ trip point is maintained at 10% of full scale.

There are other effects to consider. The voltage across the current comparator is scaled to obtain the same values as the 100mV sense voltage target, but the input referred sense voltage is reduced, causing some careful consideration of the ripple current. Input referred maximum comparator threshold is 117mV, which is the same ratio of 1.4x the DC target. Input referred I_{REV} threshold is scaled back to –24mV. The current at which the switcher starts will be reduced as well so there is some risk of boost activity. These concerns can be addressed by using a slightly larger inductor to compensate for the reduction of tolerance to ripple current.

Charger Voltage Programming

Pins CHEM and C3C4 are used to program the charger final output voltage. The CHEM pin programs Li-Ion battery chemistry for 4.1V/cell (low) or 4.2V/cell (high). The C3C4 pin selects either 3 series cells (low) or 4 series cells (high). It is recommended that these pins be shorted to ground (logic low) or left open (logic high) to effect the desired logic level. Use open-collector or open-drain outputs when interfacing to the CHEM and 3C4C pins from a logic control circuit.

Table 3. Charger Voltage Programming

V_{FINAL} (V)	3C4C	CHEM
12.3	LOW	LOW
12.6	LOW	HIGH
16.4	HIGH	LOW
16.8	HIGH	HIGH

Setting the Timer Resistor

The charger termination timer is designed for a range of 1hour to 3 hour with a ±15% uncertainty. The timer is programmed by the resistor R_{RT} using the following equation:

$$t_{TIMER} = 10 \bullet 2^{27} \bullet R_{RT} \bullet 17.5\text{pF (seconds)}$$

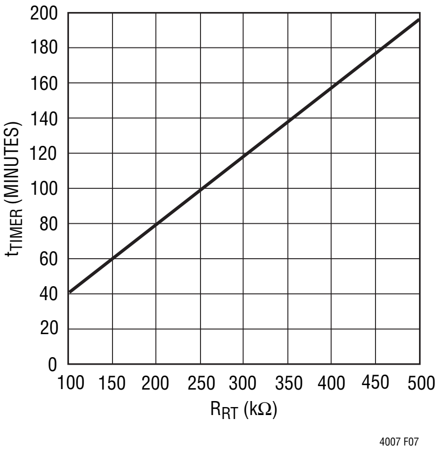

Figure 7. t_{TIMER} vs R_{RT}

It is important to keep the parasitic capacitance on the R_T pin to a minimum. The trace connecting R_T to R_{RT} should be as short as possible.

Soft-Start

The LTC4007 is soft started by the 0.12μF capacitor on the ITH pin. On start-up, ITH pin voltage will rise quickly to 0.5V, then ramp up at a rate set by the internal 40μA pull-up current and the external capacitor. Battery charging current starts ramping up when ITH voltage reaches 0.8V and full current is achieved with ITH at 2V. With a 0.12μF capacitor, time to reach full charge current is about 2ms and it is assumed that input voltage to the charger will reach full value in less than 2ms. The capacitor can be increased up to 1μF if longer input start-up times are needed.

Input and Output Capacitors

The input capacitor (C2) is assumed to absorb all input switching ripple current in the converter, so it must have adequate ripple current rating. Worst-case RMS ripple current will be equal to one half of output charging current. Actual capacitance value is not critical. Solid tantalum low ESR capacitors have high ripple current rating in a relatively small surface mount package, *but caution must*

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be used when tantalum capacitors are used for input or output bypass. High input surge currents can be created when the adapter is hot-plugged to the charger or when a battery is connected to the charger. Solid tantalum capacitors have a known failure mechanism when subjected to very high turn-on surge currents. Kemet T495 series of "Surge Robust" low ESR tantalums are rated for high surge conditions such as battery to ground.

The relatively high ESR of an aluminum electrolytic for C1, located at the AC adapter input terminal, is helpful in reducing ringing during the hot-plug event. Refer to AN88 for more information.

Highest possible voltage rating on the capacitor will minimize problems. Consult with the manufacturer before use. Alternatives include high capacity ceramic (at least 20µF) from Tokin, United Chemi-Con/Marcon, et al. Other alternative capacitors include OS-CON capacitors from Sanyo.

The output capacitor (C3) is also assumed to absorb output switching current ripple. The general formula for capacitor current is:

$$I_{RMS} = \frac{0.29(V_{BAT})\left(1 - \frac{V_{BAT}}{V_{DCIN}}\right)}{(L1)(f)}$$

For example:

V_{DCIN} = 19V, V_{BAT} = 12.6V, L1 = 10µH, and
f = 300kHz, I_{RMS} = 0.41A.

EMI considerations usually make it desirable to minimize ripple current in the battery leads, and beads or inductors may be added to increase battery impedance at the 300kHz switching frequency. Switching ripple current splits between the battery and the output capacitor depending on the ESR of the output capacitor and the battery impedance. If the ESR of C3 is 0.2Ω and the battery impedance is raised to 4Ω with a bead or inductor, only 5% of the current ripple will flow in the battery.

Inductor Selection

Higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition, the effect of inductor value on ripple current and low current operation must also be considered. The inductor ripple current ΔI_L decreases with higher frequency and increases with higher V_{IN}.

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{MAX})$. In no case should ΔI_L exceed $0.6(I_{MAX})$ due to limits imposed by I_{REV} and CA1. Remember the maximum ΔI_L occurs at the maximum input voltage. In practice 10µH is the lowest value recommended for use.

Lower charger currents generally call for larger inductor values. Use Table 4 as a guide for selecting the correct inductor value for your application.

Table 4

MAX AVERAGE CURRENT (A)	INPUT VOLTAGE (V)	MINIMUM INDUCTOR VALUE (µH)
1	≤20	40 ±20%
1	>20	56 ±20%
2	≤20	20 ±20%
2	>20	30 ±20%
3	≤20	15 ±20%
3	>20	20 ±20%
4	≤20	10 ±20%
4	>20	15 ±20%

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Charger Switching Power MOSFET and Diode Selection

Two external power MOSFETs must be selected for use with the charger: a P-channel MOSFET for the top (main) switch and an N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak gate drive levels are set internally. This voltage is typically 6V. Consequently, logic-level threshold MOSFETs must be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, total gate capacitance QG, reverse transfer capacitance C_{RSS}, input voltage and maximum output current. The charger is operating in continuous mode at moderate to high currents so the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = V_{OUT}/V_{IN}$$

$$\text{Synchronous Switch Duty Cycle} = (V_{IN} - V_{OUT})/V_{IN}.$$

The MOSFET power dissipations at maximum output current are given by:

$$\begin{aligned} PMAIN = {} & V_{OUT}/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)R_{DS(ON)} \\ & + k(V_{IN})^2(I_{MAX})(C_{RSS})(f_{OSC}) \end{aligned}$$

$$PSYNC = (V_{IN} - V_{OUT})/V_{IN}(I_{MAX})^2(1 + \delta\Delta T)R_{DS(ON)}$$

Where $\delta\Delta T$ is the temperature dependency of $R_{DS(ON)}$ and k is a constant inversely related to the gate drive current. Both MOSFETs have I^2R losses while the PMAIN equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 20V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{RSS} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage or during a short circuit when the duty cycle in this switch in nearly 100%. The term $(1 + \delta\Delta T)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs. $C_{RSS} = Q_{GD}/\Delta V_{DS}$ is usually specified in the MOSFET characteristics. The constant k = 2 can be used to estimate the contributions of the two terms in the main switch dissipation equation.

If the charger is to operate in low dropout mode or with a high duty cycle greater than 85%, then the topside P-channel efficiency generally improves with a larger MOSFET. Using asymmetrical MOSFETs may achieve cost savings or efficiency gains.

The Schottky diode D1, shown in the Typical Application on the back page, conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on and storing charge during the dead-time, which could cost as much as 1% in efficiency. A 1A Schottky is generally a good size for 4A regulators due to the relatively small average current. Larger diodes can result in additional transition losses due to their larger junction capacitance.

The diode may be omitted if the efficiency loss can be tolerated.

Calculating IC Power Dissipation

The power dissipation of the LTC4007 is dependent upon the gate charge of the top and bottom MOSFETs (QG1 & QG2 respectively) The gate charge is determined from the manufacturer's data sheet and is dependent upon both the gate voltage swing and the drain voltage swing of the MOSFET. Use 6V for the gate voltage swing and V_{DCIN} for the drain voltage swing.

$$PD = V_{DCIN} \bullet (f_{OSC}\,(QG1 + QG2) + I_Q)$$

Example:

$V_{DCIN} = 19V$, $f_{OSC} = 345kHz$, $QG1 = QG2 = 15nC$,
$I_Q = 5mA$

$PD = 292mW$

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Adapter Limiting

An important feature of the LTC4007 is the ability to automatically adjust charging current to a level which avoids overloading the wall adapter. This allows the product to operate at the same time that batteries are being charged without complex load management algorithms. Additionally, batteries will automatically be charged at the maximum possible rate of which the adapter is capable.

This feature is created by sensing total adapter output current and adjusting charging current downward if a preset adapter current limit is exceeded. True analog control is used, with closed-loop feedback ensuring that adapter load current remains within limits. Amplifier CL1 in Figure 8 senses the voltage across R_{CL}, connected between the CLP and CLN pins. When this voltage exceeds 100mV, the amplifier will override programmed charging current to limit adapter current to $100mV/R_{CL}$. A lowpass filter formed by 5kΩ and 15nF is required to eliminate switching noise. If the current limit is not used, CLP and CLN should be connected together and tied to DCIN.

Note that the $\overline{I_{CL}}$ pin will be asserted when the voltage across R_{CL} is 93mV, before the adapter limit regulation threshold.

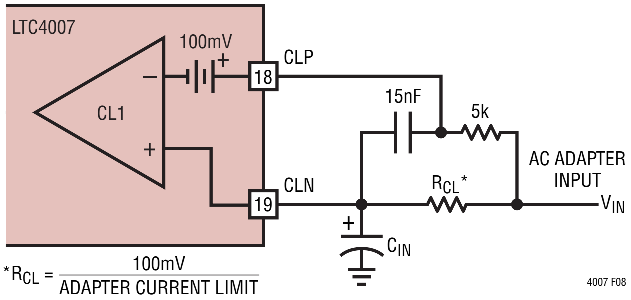

Figure 8. Adapter Current Limiting

Setting Input Current Limit

To set the input current limit, you need to know the minimum wall adapter current rating. Subtract 7% for the input current limit tolerance and use that current to determine the resistor value.

$$R_{CL} = 100mV/I_{LIM}$$
$$I_{LIM} = \text{Adapter Min Current} - (\text{Adapter Min Current} \bullet 7\%)$$

Table 5. Common R_{CL} Resistor Values

ADAPTER RATING (A)	R_{CL} VALUE* (Ω) 1%	R_{CL} POWER DISSIPATION (W)	R_{CL} POWER RATING (W)
1.5	0.06	0.135	0.25
1.8	0.05	0.162	0.25
2	0.045	0.18	0.25
2.3	0.039	0.206	0.25
2.5	0.036	0.225	0.5
2.7	0.033	0.241	0.5
3	0.03	0.27	0.5

* Values shown above are rounded to nearest standard value.

As is often the case, the wall adapter will usually have at least a +10% current limit margin and many times one can simply set the adapter current limit value to the actual adapter rating (see Table 5).

Designing the Thermistor Network

There are several networks that will yield the desired function of voltage vs temperature needed for proper operation of the thermistor. The simplest of these is the voltage divider shown in Figure 9. Unfortunately, since the HIGH/LOW comparator thresholds are fixed internally, there is only one thermistor type that can be used in this network; the thermistor must have a HIGH/LOW resistance ratio of 1:7. If this happy circumstance is true for you, then simply set R9 = $R_{TH(LOW)}$.

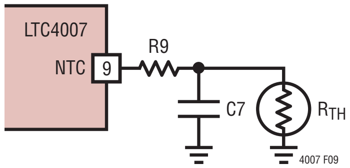

Figure 9. Voltage Divider Thermistor Network

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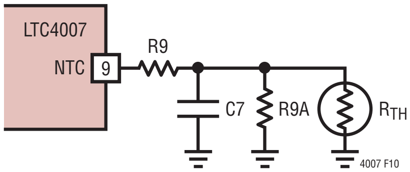

Figure 10. General Thermistor Network

If you are using a thermistor that doesn't have a 1:7 HIGH/LOW ratio, or you wish to set the HIGH/LOW limits to different temperatures, then the more generic network in Figure 10 should work.

Once the thermistor, R_{TH}, has been selected and the thermistor value is known at the temperature limits, then resistors R9 and R9A are given by:

For NTC thermistors:

$$R9 = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(LOW)} - R_{TH(HIGH)})$$

$$R9A = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(LOW)} - 7 \bullet R_{TH(HIGH)})$$

$$\text{Where } R_{TH(LOW)} > 7 \bullet R_{TH(HIGH)}$$

For PTC thermistors:

$$R9 = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(HIGH)} - R_{TH(LOW)})$$

$$R9A = 6\ R_{TH(LOW)} \bullet R_{TH(HIGH)}/(R_{TH(HIGH)} - 7 \bullet R_{TH(LOW)})$$

$$\text{Where } R_{TH(HIGH)} > 7 \bullet R_{TH(LOW)}$$

Example #1: 10kΩ NTC with custom limits

TLOW = 0°C, THIGH = 50°C
R_{TH} = 10k at 25°C,
$R_{TH(LOW)}$ = 32.582k at 0°C
$R_{TH(HIGH)}$ = 3.635k at 50°C
R9 = 24.55k → 24.3k (nearest 1% value)
R9A = 99.6k → 100k (nearest 1% value)

Example #2: 100kΩ NTC

TLOW = 5°C, THIGH = 50°C
R_{TH} = 100k at 25°C,
$R_{TH(LOW)}$ = 272.05k at 5°C
$R_{TH(HIGH)}$ = 33.195k at 50°C
R9 = 226.9k → 226k (nearest 1% value)
R9A = 1.365M → 1.37M (nearest 1% value)

Example #3: 22kΩ PTC

TLOW = 0°C, THIGH = 50°C
R_{TH} = 22k at 25°C,
$R_{TH(LOW)}$ = 6.53k at 0°C
$R_{TH(HIGH)}$ = 61.4k at 50°C
R9 = 43.9k → 44.2k (nearest 1% value)
R9A = 154k

Sizing the Thermistor Hold Capacitor

During the hold interval, C7 must hold the voltage across the thermistor relatively constant to avoid false readings. A reasonable amount of ripple on NTC during the hold interval is about 10mV to 15mV. Therefore, the value of C7 is given by:

$$\begin{aligned} C7 &= t_{HOLD}/(R9/7 \bullet -\ln(1 - 8 \bullet 15mV/4.5V)) \\ &= 10 \bullet R_{RT} \bullet 17.5pF/(R9/7 \bullet -\ln(1 - 8 \bullet 15mV/4.5V) \end{aligned}$$

Example:

R9 = 24.3k
R_{RT} = 309k (~2 hour timer)
C7 = 0.57µF → 0.56µF (nearest value)

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Disabling the Thermistor Function

If the thermistor is not needed, connecting a resistor between DCIN and NTC will disable it. The resistor should be sized to provide at least 10μA with the minimum voltage applied to DCIN and 10V at NTC. Do not exceed 30μA. Generally, a 301k resistor will work for DCIN less than 15V. A 499k resistor is recommended for DCIN between 15V and 24V.

Conditioning Depleted Batteries

Severely depleted batteries, with less than 2.5V/cell, should be conditioned with a trickle charge to prevent possible damage. This trickle charge is typically 10% of the 1C rate of the battery. The LTC4007 can automatically trickle charge depleted batteries using the circuit in Figure 11. If the battery voltage is less than 2.5V/cell (2.44V/cell if CHEM is low) then the $\overline{\text{LOBAT}}$ indicator will be low and Q4 is off. This programs the charging current with R_{PROG} = R6 + R14. Charging current is approximately 300mA. When the cell voltage becomes greater than 2.5V the $\overline{\text{LOBAT}}$ indicator goes high, Q4 shorts out R13, then R_{PROG} = R6. Charging current is then equal to 3A.

PCB Layout Considerations

For maximum efficiency, the switch node rise and fall times should be minimized. To prevent magnetic and electrical field radiation and high frequency resonant problems, proper layout of the components connected to the IC is essential (see Figure 12). Here is a PCB layout priority list for proper layout. Layout the PCB using this specific order.

1. Input capacitors need to be placed as close as possible to switching FET's supply and ground connections. Shortest copper trace connections possible. These parts must be on the same layer of copper. Vias must not be used to make this connection.
2. The control IC needs to be close to the switching FET's gate terminals. Keep the gate drive signals short for a clean FET drive. This includes IC supply pins that connect to the switching FET source pins. The IC can be placed on the opposite side of the PCB relative to above.
3. Place inductor input as close as possible to switching FET's output connection. Minimize the surface area of this trace. Make the trace width the minimum amount needed to support current—no copper fills or pours. Avoid running the connection using multiple layers in parallel. Minimize capacitance from this node to any other trace or plane.
4. Place the output current sense resistor right next to the inductor output but oriented such that the IC's current sense feedback traces going to resistor are not long. The feedback traces need to be routed together as a single pair on the same layer at any given time with smallest trace spacing possible. Locate any filter component on these traces next to the IC and not at the sense resistor location.
5. Place output capacitors next to the sense resistor output and ground.
6. Output capacitor ground connections need to feed into same copper that connects to the input capacitor ground before tying back into system ground.

APPLICATIONS INFORMATION

General Rules

7. Connection of switching ground to system ground or internal ground plane should be single point. If the system has an internal system ground plane, a good way to do this is to cluster vias into a single star point to make the connection.
8. Route analog ground as a trace tied back to IC ground (analog ground pin if present) before connecting to any other ground. Avoid using the system ground plane. CAD trick: make analog ground a separate ground net and use a 0Ω resistor to tie analog ground to system ground.
9. A good rule of thumb for via count for a given high current path is to use 0.5A per via. Be consistent.
10. If possible, place all the parts listed above on the same PCB layer.
11. Copper fills or pours are good for all power connections except as noted above in Rule 3. You can also use copper planes on multiple layers in parallel too—this helps with thermal management and lower trace inductance improving EMI performance further.
12. For best current programming accuracy provide a Kelvin connection from R_{SENSE} to CSP and BAT. See Figure 12 as an example.

It is important to keep the parasitic capacitance on the R_T, CSP and BAT pins to a minimum. The traces connecting these pins to their respective resistors should be as short as possible.

APPLICATIONS INFORMATION

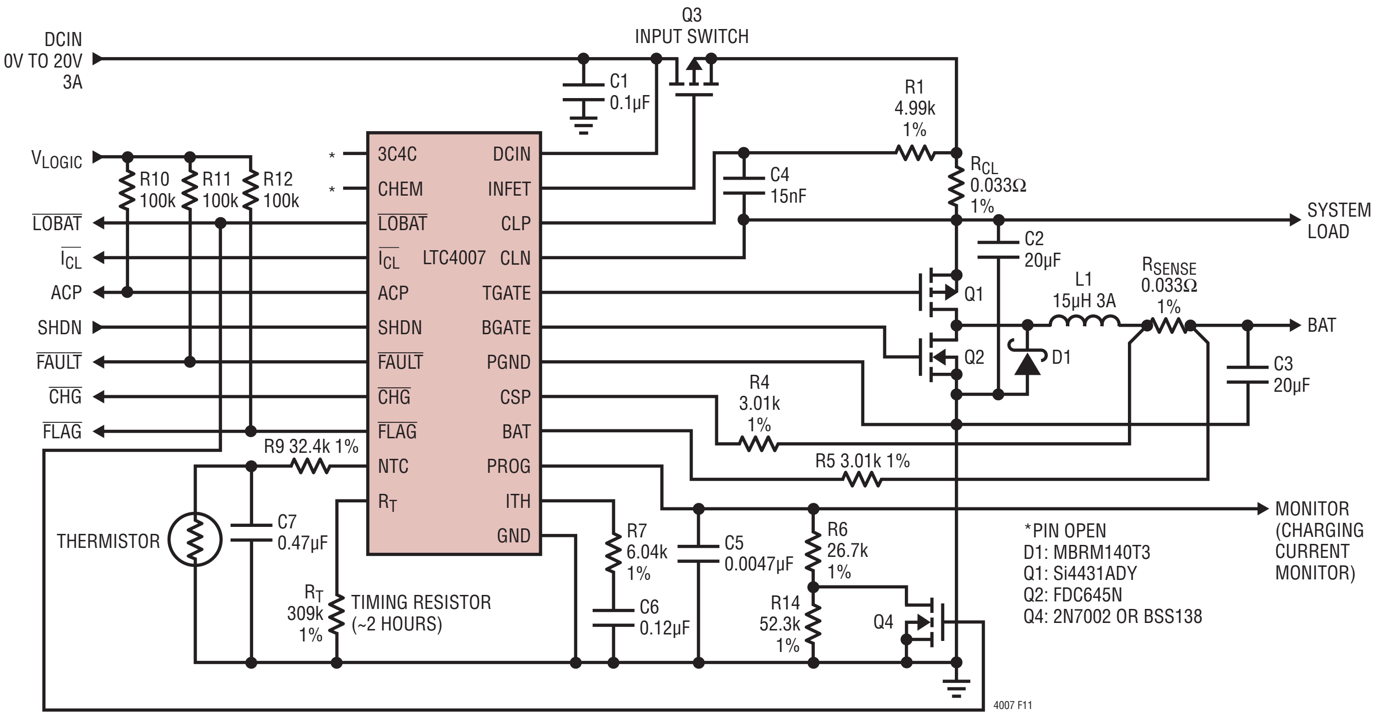


Figure 11. Circuit Application (16.8V/3A) to Automatically Trickle Charge Depleted Batteries

APPLICATIONS INFORMATION

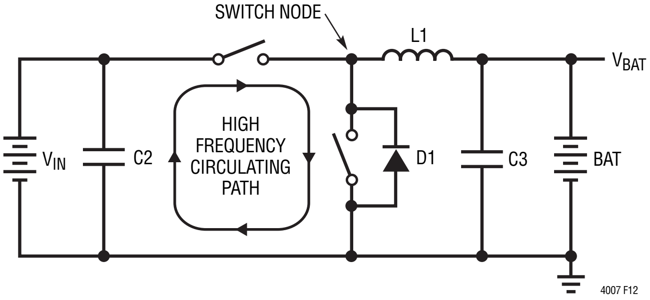


Figure 12. High Speed Switching Path

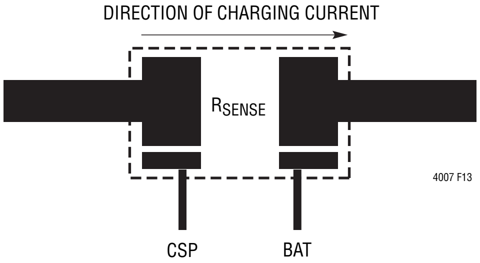
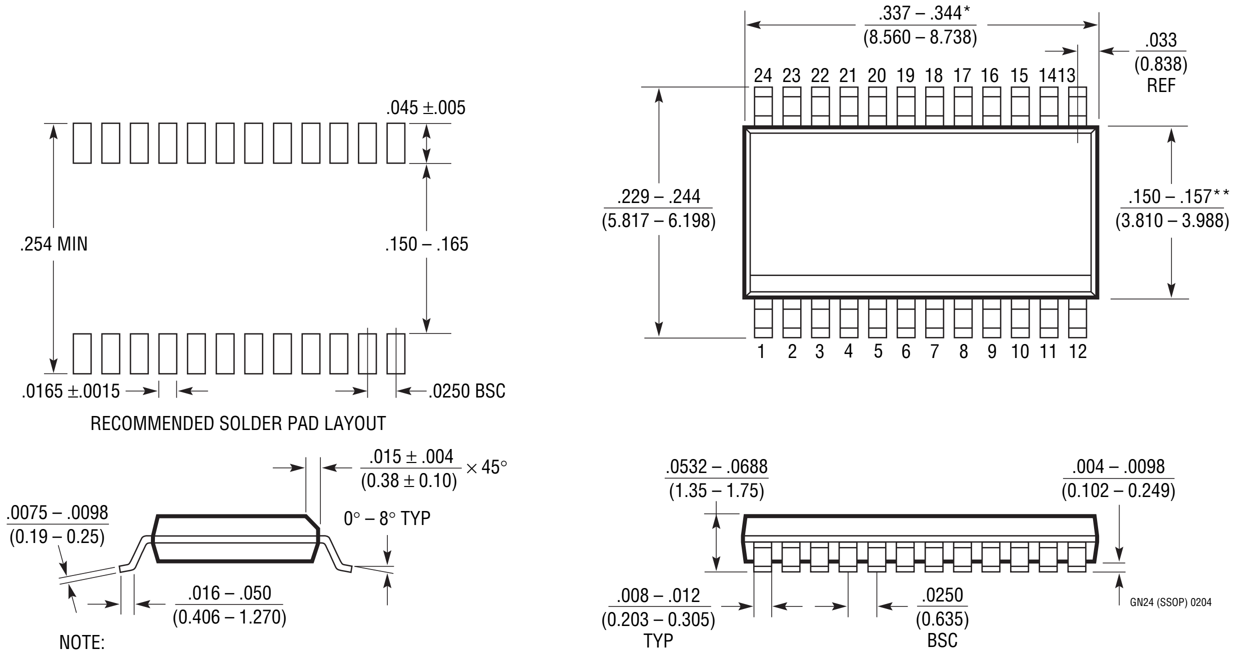


Figure 13. Kelvin Sensing of Charging Current

PACKAGE DESCRIPTION

GN Package
24-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)



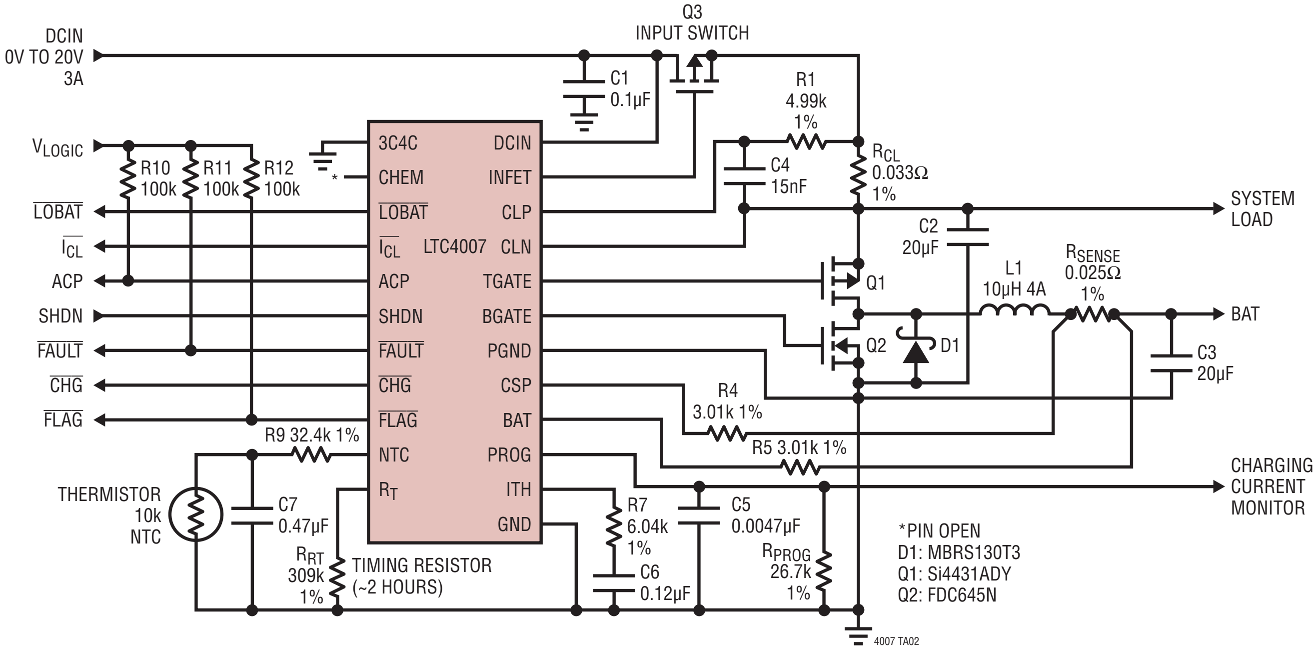
NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE
*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE
**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	7/10	Changed ±5% to ±4% in Description text	1
		Updated Figure 6	13
C	8/10	"Charge Termination" text added	1, 4, 6, 9, 10, 17

TYPICAL APPLICATION

12.6V/4A Li-Ion Battery Charger



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1511	Constant-Current/Constant-Voltage 3A Battery Charger with Input Current Limiting	High Efficiency Current Mode PWM with 4A Internal Switch
LT1513	SEPIC Constant- or Programmable-Current/ Constant-Voltage Battery Charger	Charger Input Voltage May Be Higher, Equal to or Lower Than Battery Voltage; Charges Any Number of Cells Up to 20V, 500kHz Switching Frequency
LT1571	1.5A Switching Charger	1- or 2-Cell Li-Ion, 500kHz or 200kHz Switching Frequency, Termination Flag
LTC1628-PG	2-Phase, Dual Synchronous Step-Down Controller	Minimizes C_{IN} and C_{OUT}, Power Good Output, $3.5V \le V_{IN} \le 36V$
LTC1709	2-Phase, Dual Synchronous Step-Down Controller with VID	Up to 42A Output, Minimum C_{IN} and C_{OUT}, Uses Smallest Components for Intel and AMD Processors
LTC1729		
LT1769	2A Switching Battery Charger	Constant-Current/Constant-Voltage Switching Regulator, Input Current Limiting Maximizes Charge Current
LTC1778	Wide Operating Range, No R_{SENSE} Synchronous Step-Down Controller	2% to 90% Duty Cycle at 200kHz, Stable with Ceramic C_{OUT}
LTC1960	Dual Battery Charger/Selector with SPI Interface	Simultaneous Charge or Discharge of Two Batteries, DAC Programmable Current and Voltage, Input Current Limiting Maximizes Charge Current
LTC3711	No R_{SENSE}™ Synchronous Step-Down Controller with VID	$3.5V \le V_{IN} \le 36V$, $0.925V \le V_{OUT} \le 2V$, for Transmeta, AMD and Intel Mobile Processors
LTC4006	Small, High Efficiency, Fixed Voltage, Lithium-Ion Battery Charger	Constant-Current/Constant-Voltage Switching Regulator with Termination Timer, AC Adapter Current Limit and Thermistor Sensor in a Small 16-Pin Package
LTC4008	High Efficiency, Programmable Voltage/Current Battery Charger	Constant-Current/Constant-Voltage Switching Regulator, Resistor Voltage Current Programming, AC Adapter Current Limit and Thermistor Sensor

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