PowerPath Controller for Dual Battery Systems

FEATURES

- **Complete Power Path Management for Two Batteries, DC Power Source, Charger and Backup**
- **Compatible with Li-Ion, NiCd, NiMH and Lead-Acid Battery Chemistries**
- **"3-Diode" Mode Ensures Powers is Available under "Cold Start" Conditions**
- **All N-Channel Switching Reduces Power Losses**
- Capacitor and Battery Inrush Current Limited
- "Seamless" Switching Between Power Sources
- Independent Charging and Monitoring of Two Battery Packs
- New, Small Footprint, 36-Lead SSOP Package

APPLICATIONS

- Notebook Computer Power Management
- Portable Instruments
- Handheld Terminals
- Portable Medical Equipment
- Portable Industrial Control Equipment

DESCRIPTION

The LTC®1479 is the "heart" of a total power management solution for single and dual battery notebook computers and other portable equipment. The LTC1479 directs power from up to two battery packs and a DC power source to the input of the main system switching regulator. It works in concert with related LTC power management products (e.g. LTC1435, LT®1511, etc.) to create a total system solution; starting from the batteries and the DC power source, and ending at the input of each of the computer's complex loads. A system-provided power management µP monitors and actively directs the LTC1479.

The LTC1479 uses low loss N-channel MOSFET switches to direct power from three main sources. An adaptive current limiting scheme reduces capacitor and battery inrush current by controlling the gates of the MOSFET switches during transitions. The LTC1479 interfaces directly to the LT1510, LT1511 and LT1620/LTC1435 battery charging circuits.

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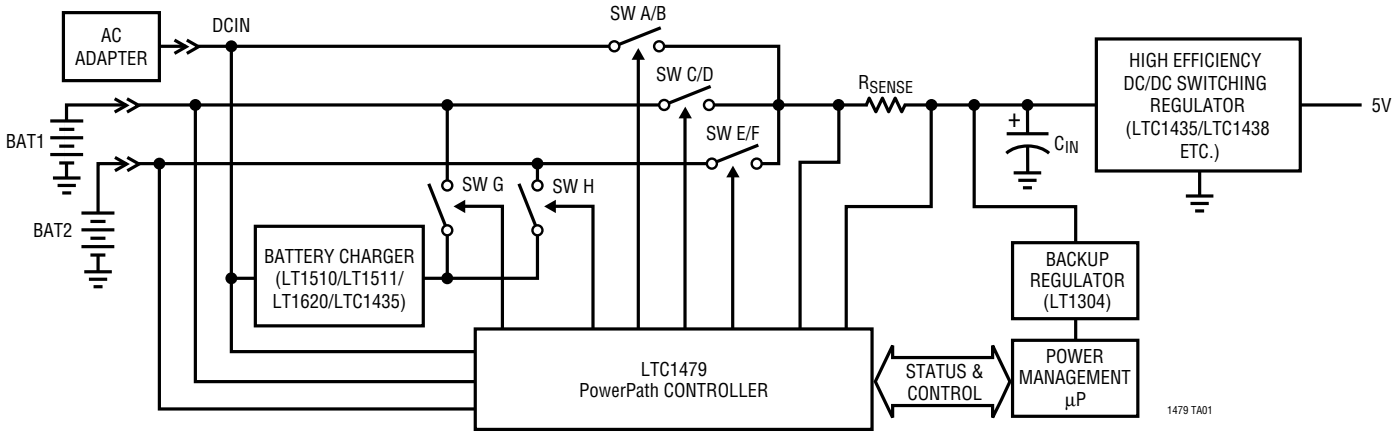
PowerPath is a trademark of Linear Technology Corporation.

TYPICAL APPLICATION

Dual Battery PowerPath™ Controller System Block Diagram



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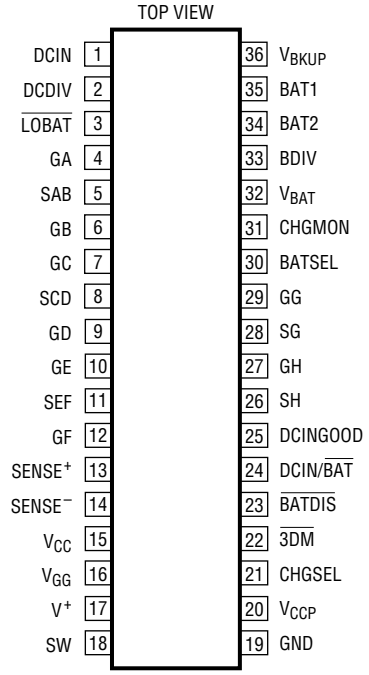
ABSOLUTE MAXIMUM RATINGS

DCIN, BAT1, BAT2 Supply Voltages ..... –0.3V to 32V
SENSE$^+$, SENSE$^-$, V_{BAT}, V^+ ..... –0.3V to 32V
GA, GB, GC, GD, GE, GF, GG, GH ..... –0.3V to 42V
SAB, SCD, SEF, SG, SH ..... –0.3V to 32V
SW, V_{GG} ..... –0.3V to 42V
DCDIV, BDIV ..... –0.3V to 5.5V
All Logic Inputs (Note 1) ..... –0.3V to 7.5V
All Logic Outputs (Note 1) ..... –0.3V to 7.5V
V_{CC} Regulator Output Current 1mA
V_{CCP} Regulator Output Current 1mA
V^+ Output Current 1mA
V_{GG} Regulator Output Current 100µA
Operating Temperature
LTC1479CG ..... 0°C to 70°C
LTC1479IG ..... –40°C to 85°C
Junction Temperature ..... 125°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



G PACKAGE (209 mils)
36-LEAD PLASTIC SSOP

T_{JMAX} = 100°C, θ_{JA} = 95°C/W

ORDER PART NUMBER
LTC1479CG LTC1479IG

Consult factory for Military grade parts.

DC ELECTRICAL CHARACTERISTICS

V_{DCIN} = 25V, V_{BAT1} = 16V, V_{BAT2} = 12V, T_A = 25°C unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supplies							
V_{DCIN}	DCIN Operating Range	(Mode 1) DCIN Selected		6		28	V
V_{BAT1}	Battery 1 Operating Range	(Mode 5) Battery 1 Selected		6		28	V
V_{BAT2}	Battery 2 Operating Range	(Mode 6) Battery 2 Selected		6		28	V
V_{BKUP}	Backup Operating Range	(Mode 8) Backup Operation		6		28	V
I_{DCIN}	DCIN Operating Current	(Mode 1) DCIN Selected			175	500	µA
I_{VBAT1}	Battery 1 Operating Current	(Mode 5) Battery 1 Selected			150	500	µA
I_{VBAT2}	Battery 2 Operating Current	(Mode 6) Battery 2 Selected			150	500	µA
I_{VBKUP}	Backup Operating Current	(Mode 8) Backup Operation (V_{BKUP} = 6V)			40	100	µA
V_{CCP}	V_{CCP} Regulator Output Voltage	(Modes 1, 5, 6) DCIN, Battery 1 or Battery 2 Selected	●	4.0	4.8	6.0	V
V_{CC}	V_{CC} Regulator Output Voltage	(Modes 1, 5, 6) DCIN, Battery 1 or Battery 2 Selected	●	3.3	3.6	3.9	V
V_{GG}	V_{GG} Gate Supply Voltage	(Modes 1, 5, 6) DCIN, Battery 1 or Battery 2 Selected	●	34.0	36.3	40.0	V
V_{UVLO}	UV Lockout Threshold	(Mode 9) No Power, V_{BATX} Falling from 12V		4.0	4.5	5.0	V
$V_{UVLOHYS}$	UV Lockout Hysteresis	(Mode 9) No Power, V_{BATX} Rising from 1V		0.2	0.5	1.0	V

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DC ELECTRICAL CHARACTERISTICS

V_{DCIN} = 25V, V_{BAT1} = 16V, V_{BAT2} = 12V, T_A = 25°C unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DCIN Good Monitor							
$V_{THDCDIV}$	DCDIV Threshold Voltage	(Mode 1) V_{DCDIV} Rising from 1V to 1.5V	●	1.190	1.215	1.240	V
$V_{HYSDCDIV}$	DCDIV Hysteresis Voltage	(Mode 1) V_{DCDIV} Falling from 1.5V to 1V		10	35	50	mV
$I_{BIASDCDIV}$	DCDIV Input Bias Current	(Mode 1) V_{DCDIV} = 1.5V			20		nA
V_{LODCGD}	DCINGOOD Output Low Voltage	(Mode 1) V_{DCDIV} = 1V, $I_{DCINGOOD}$ = 100µA		0	0.1	0.4	V
I_{PUDCGD}	DCINGOOD Pull-Up Current	(Mode 1) V_{DCDIV} = 1.5V, $V_{DCINGOOD}$ = 0V		1	2	6	µA
$I_{LKGDCGD}$	DCINGOOD Leakage Current	(Mode 1) V_{DCDIV} = 1.5V, $V_{DCINGOOD}$ = 7V				±1	µA
Battery Monitor							
$V_{THLOBAT}$	Low-Battery Threshold Voltage	(Modes 5, 6) V_{BDIV} Falling from 1.5V to 1V	●	1.190	1.215	1.240	V
$V_{HYSLOBAT}$	Low-Battery Hysteresis Voltage	(Modes 5, 6) V_{BDIV} Rising from 1V to 1.5V		10	35	50	mV
$I_{BIASBDIV}$	BDIV Input Bias Current	(Modes 5, 6) V_{BDIV} = 1.5V			20		nA
$V_{LOLOBAT}$	$\overline{LOBAT}$ Output Low Voltage	(Modes 5, 6) V_{BDIV} = 1V, $I_{\overline{LOBAT}}$ = 100µA		0	0.1	0.4	V
$I_{LKGLOBAT}$	$\overline{LOBAT}$ Output Leakage Current	(Modes 5, 6) V_{BDIV} = 1.5V, $V_{\overline{LOBAT}}$ = 7V				±1	µA
$R_{ONBATSW}$	Battery Switch ON Resistance	(Modes 5, 6) Each Switch Tested Independently		200	400	800	Ω
$I_{LKGBATSW}$	Battery Switch OFF Leakage	(Modes 5, 6) Each Switch Tested Independently				±1	µA
Gate Drivers							
$V_{GS(ON)}$	Gate-to-Source ON Voltage (GA to GF) Gate-to-Source ON Voltage (GG, GH)	(Modes 1, 2, 4, 5, 6) I_{GS} = –1µA (Modes 2, 4) I_{GS} = –1µA		5.0 4.5	5.5 5.2	7.0 7.0	V V
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	(Modes 1, 2, 4, 5, 6) I_{GS} = 100µA			0	0.4	V
$I_{BSENSE+}$	$SENSE^+$ Input Bias Current	(Modes 1, 5, 6)		5	15	30	µA
$I_{BSENSE–}$	$SENSE^–$ Input Bias Current	(Modes 1, 5, 6)		5	15	30	µA
V_{SENSE}	Inrush Current Limit Sense Voltage	(Modes 1, 5, 6)	●	0.15	0.20	0.25	V
I_{PDSAB}	SAB Pull-Down Current	(Modes 5, 6) V_{SAB} = 10V		30	100	300	µA
I_{PDSCD}	SCD Pull-Down Current	(Mode 1) V_{SCD} = 10V		30	100	300	µA
I_{PDSEF}	SEF Pull-Down Current	(Mode 1) V_{SEF} = 10V		30	100	300	µA
I_{PDSG}	SG Pull-Down Current	(Mode 1) V_{SG} = 10V			3		mA
I_{PDSH}	SH Pull-Down Current	(Mode 1) V_{SH} = 10V			3		mA
Charge Monitor							
R_{ONCMON}	CHGMON Switch ON Resistance	(Modes 5, 6) Each Switch Tested Independently		50	150	250	Ω
$I_{LKGCMON}$	CHGMON Switch OFF Leakage	(Modes 5, 6) Each Switch Tested Independently				±1	µA
Digital Inputs							
$V_{HIDIGIN}$	Input High Voltage	(Mode 1) All Digital Inputs	●	2			V
$V_{LODIGIN}$	Input Low Voltage	(Mode 1) All Digital Inputs	●			0.8	V
$I_{HIDIGIN}$	Input Leakage Current	(Mode 1) All Digital Inputs, V_{DIGINX} = 7V				±1	µA
$I_{LODIGIN}$	Input Leakage Current	(Mode 1) V_{DIGINX} = 0V (Note 3)				±1	µA
$I_{PUDIGIN}$	Input Pull-Up Current	(Mode 1) V_{DIGINX} = 0V (Note 4)		1	2	6	µA

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AC ELECTRICAL CHARACTERISTICS

V_{DCIN} = 25V, V_{BAT1} = 16V, V_{BAT2} = 12V, T_A = 25°C unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{ONGA/GB}$	Gate A/B Turn-On Time	V_{GS} > 3V (Note 5)			30		µs
$t_{ONGC/GD}$	Gate C/D Turn-On Time	V_{GS} > 3V (Note 5)			30		µs
$t_{ONGE/GF}$	Gate E/F Turn-On Time	V_{GS} > 3V (Note 5)			30		µs
$t_{OFFGA/GB}$	Gate A/B Turn-Off Time	V_{GS} < 1V (Note 5)			3		µs
$t_{OFFGC/GD}$	Gate C/D Turn-Off Time	V_{GS} < 1V (Note 5)			3		µs
$t_{OFFGE/GF}$	Gate E/F Turn-Off Time	V_{GS} < 1V (Note 5)			3		µs
$t_{ONGG/GH}$	Gate G/H Turn-On Time	V_{GS} > 3V (Note 5)			300		µs
$t_{OFFGG/GH}$	Gate G/H Turn-Off Time	V_{GS} < 1V (Note 5)			5		µs
f_{OVGG}	V_{GG} Reg Operating Frequency				30		kHz
t_{dLOBAT}	$\overline{LOBAT}$ Delay Times	ΔV_{BDIV} = ±100mV, R_{PULLUP} = 51k			5		µs
$t_{dDCINGOOD}$	DCINGOOD Delay Times	ΔV_{DCDIV} = ±100mV, R_{PULLUP} = 51k			5		µs

The ● denotes specifications which apply over the full operating temperature range.

Note 1: The logic inputs are high impedance CMOS gates with ESD protection diodes to ground and therefore should not be forced below ground. These inputs can however be driven above the V_{CCP} or V_{CC} supply rails as there are no clamping diodes connected between the input pins and the supply rails. This facilitates operation in mixed 5V/3V systems.

Note 2: The Selected Operating Mode Truth Table, which defines the operating conditions and logical states associated with each "normal" operating mode, should be used in conjunction with the Electrical Characteristics table to establish test conditions. Actual production test conditions may be more stringent.

Note 3: The following inputs are high impedance CMOS inputs: $\overline{3DM}$ and DCIN/$\overline{BAT}$ and have no internal pull-up current.

Note 4: The following inputs have built-in 2µA pull-up current sources (passed through series diodes): BATSEL, $\overline{BATDIS}$ and CHGSEL.

Note 5: Gate turn-on and turn-off times are measured with no inrush current limiting, i. e., V_{SENSE} = 0V, using Si4936DY MOSFETs in the typical application circuit.

TRUTH TABLE (Selected Operating Modes)

SELECTED MODES		LOGIC INPUTS					SWITCH STATUS					OUTPUTS			
NO.	MODE	$\overline{3DM}$	DCIN/$\overline{BAT}$	BATSEL	$\overline{BATDIS}$	CHGSEL	SW A/B	SW C/D	SW E/F	SW G	SW H	CHGMON	V_{BAT}	$\overline{LOBAT}$	DCINGOOD
1	DC Operation	H	H	H	L	H	On	Off	Off	Off	Off	Hi-Z	BAT1	H	H
2	DC Operation and BAT1 Charging	H	H	H	H	H	On	Off	Off	On	Off	BAT1	BAT1	H	H
3	DC Operation and BAT2 Disconnected	H	H	L	L	L	On	Off	Off	Off	Off	Hi-Z	BAT2	H	H
4	DC Operation and BAT2 Charging	H	H	L	H	L	On	Off	Off	Off	On	BAT2	BAT2	H	H
5	BAT1 Operation	H	L	H	H	H	Off	On	Off	Off	Off	Hi-Z	BAT1	H	L
6	BAT2 Operation	H	L	L	H	H	Off	Off	On	Off	Off	Hi-Z	BAT2	H	L
7	BAT1 Low and Disconnected	H	L	H	L	H	Off	Off	Off	Off	Off	Hi-Z	BAT1	L	L
8	Backup Operation	H	L	H	L	H	Off	Off	Off	Off	Off	Hi-Z	BAT1	L	L
9	No Power (No Backup)	L	L	L	L	L	Off	Off	Off	Off	Off	Hi-Z	BAT2	L	L
10	DC Reconnected	L	L	H	L	H	$\overline{3DM}$*	$\overline{3DM}$*	$\overline{3DM}$*	Off	Off	Hi-Z	BAT1	L	H
11	DC Connected and Reset	H	H	H	L	H	On	Off	Off	Off	Off	Hi-Z	BAT1	L	H

* $\overline{3DM}$ = Three Diode Mode. When this mode is invoked, only the first MOSFET switch in each back-to-back switch pair, i. e., SW A, SW C and SW E is turned on. Current may still pass through the inherent body diode of the idled switches, i.e., SW B, SW D and SW F to help restart the system after abnormal operating conditions have been encountered. See the Timing Diagram and Applications Information sections for further details.

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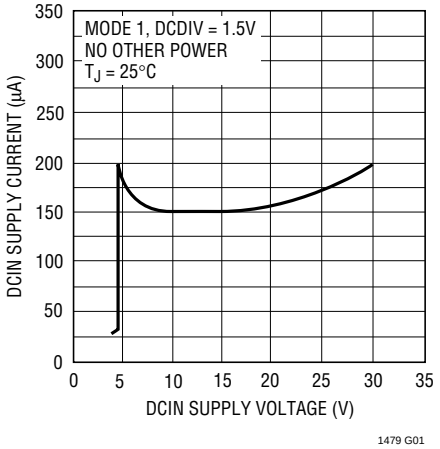
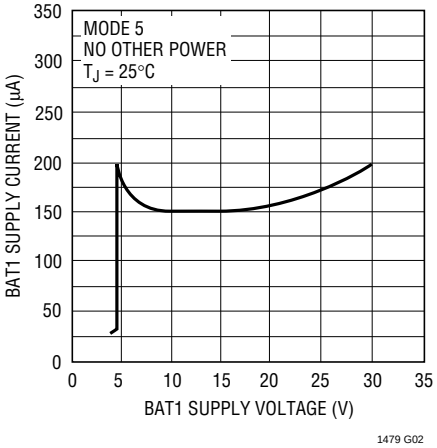
TYPICAL PERFORMANCE CHARACTERISTICS

DCIN Supply Current



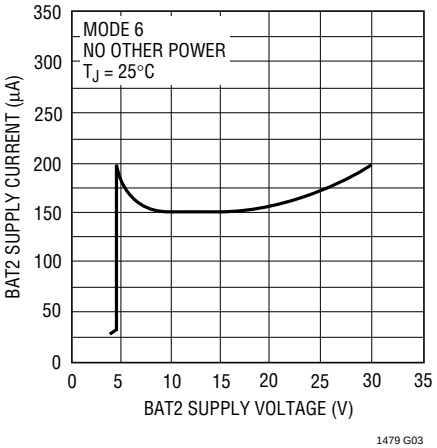
1479 G01

BAT1 Supply Current



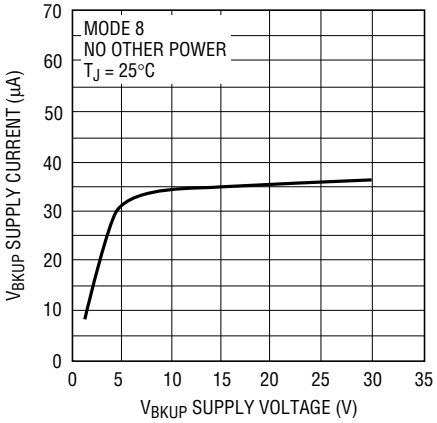
1479 G02

BAT2 Supply Current



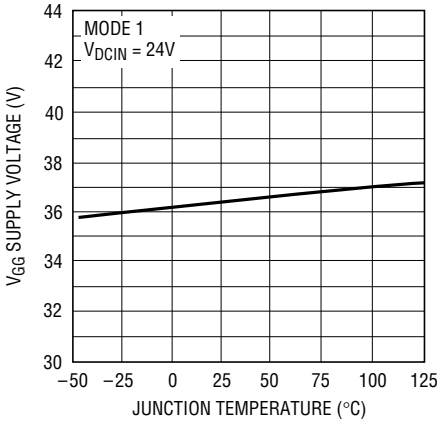
1479 G03

V_{BKUP} Supply Current



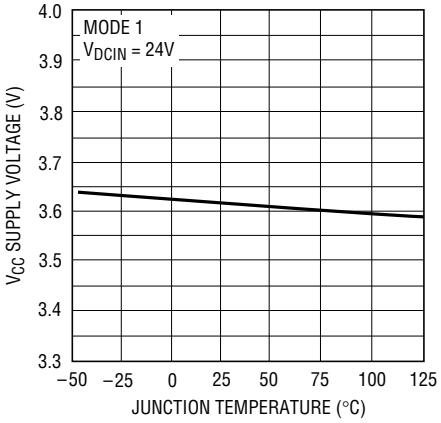
1479 G04

V_{GG} Supply Voltage



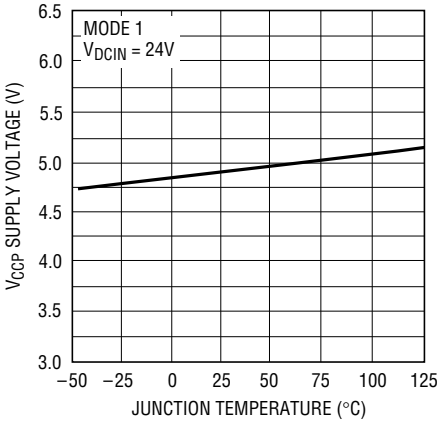
1479 G05

V_{CC} Supply Voltage



1479 G06

V_{CCP} Supply Voltage



1479 G07

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PIN FUNCTIONS

External Power Supply Pins

DCIN (Pin 1): Supply Input. A 330Ω resistor should be put in series with this pin and the external DC power source. A 0.1µF bypass capacitor should be connected to this pin as close as possible.

DCDIV (Pin 2): Supply Divider Input. This is a high impedance comparator input with a 1.215V threshold (rising edge) and approximately –35mV hysteresis.

BAT1, BAT2 (Pins 35, 34): Supply Input. These two pins are the inputs from the two batteries. A 1µF bypass capacitor should be connected to each pin as close as possible if there is no larger battery supply capacitor within 2".

V_{BAT} (Pin 32): Battery Voltage Sense. This pin connects the top of the battery resistor ladder to either BAT1 or BAT2.

BDIV (Pin 33): Battery Divider Input. A high impedance comparator input with a 1.215V threshold (falling edge) and approximately 35mV hysteresis.

V_{BKUP} (Pin 36): Supply Input. This input supplies power to the LTC1479 when in the backup mode of operation. A 1µF bypass capacitor should be connected to the V_{BKUP} pin as close as possible if there is no larger backup supply capacitor within 2".

Internal Power Supply Pins

V_{CCP} (Pin 20): Power Supply Output. Bypass this output with at least a 0.1µF capacitor. The V_{CCP} power supply is used primarily to power internal logic circuitry.

V_{CC} (Pin 15): Power Supply Output. This is a nominal 3.60V output. Bypass this regulator output with a 2.2µF tantalum capacitor. *This capacitor is required for stability.*

V^+ (Pin 17): Supply. The V^+ pin is connected via three internal diodes to the DCIN, BAT1 and BAT2 pins and powers the top of the V_{GG} switching regulator inductor. Bypass this pin with a 1µF/35V capacitor.

V_{GG} (Pin 16): Gate Supply. This high voltage (36.5V) switching regulator is intended only for driving the internal micropower gate drive circuitry. *Do not load this pin with any external circuitry.* Bypass this pin with a 1µF/50V capacitor.

SW (Pin 18): Output. This pin drives the "bottom" of the V_{GG} switching regulator inductor which is connected between this pin and the V^+ pin.

GND (Pin 19): Ground. The V_{GG} and V^+ bypass capacitors should be returned to this ground which is connected directly to the source of the N-channel switch in the V_{GG} regulator.

Input Power Switches

GA, GB (Pins 4, 6): DCIN Switch Gate Drive. These two pins drive the gates of the back-to-back N-channel switches in series with the DCIN input.

SAB (Pin 5): Source Return. The SAB pin is connected to the sources of SW A and SW B. A small pull-down current source returns this node to 0V when the switches are turned off.

GC, GD (Pins 7, 9): BAT1 Switch Gate Drive. These two pins drive the gates of the back-to-back N-channel switches in series with the BAT1 input.

SCD (Pin 8): Source Return. The SCD pin is connected to the sources of SW C and SW D. A small pull-down current source returns this node to 0V when the switches are turned off.

GE, GF (Pins 10, 12): BAT2 Switch Gate Drive. These two pins drive the gates of the back-to-back N-channel switches in series with the BAT2 input.

SEF (Pin 11): Source Return. The SEF pin is connected to the sources of SW E and SW F. A small pull-down current source returns this node to 0V potential when the switches are turned off.

$SENSE^+$ (Pin 13): Inrush Current Input. This pin should be connected directly to the "top" (switch side) of the low valued resistor in series with the three input power selector switch pairs, SW A/B, SW C/D and SW E/F, for detecting and controlling the inrush current into and out of the power supply sources and the output capacitor.

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PIN FUNCTIONS

SENSE⁻ (Pin 14): Inrush Current Input. This pin should be connected directly to the "bottom" (output side) of the low valued resistor in series with the three input power selector switch pairs, SW A/B, SW C/D and SW E/F, for detecting and controlling the inrush current into and out of the power supply sources and the output capacitor.

Battery Charging Switches

GG, GH (Pins 29, 27): Charger Switch Gate Drive. These two pins drive the gates of the back-to-back N-channel switch pairs, SW G and SW H, between the charger output and the two batteries.

SG, SH (Pin 28, 26): Source Returns. These two pins are connected to the sources of SW G and SW H respectively. A small pull-down current source returns these nodes to 0V when the switches are turned off.

CHGMON (Pin 31): Battery Selector Output. This pin is the output of an internal switch which is connected to BAT1 and BAT2 and connects the positive terminal of the selected battery to the voltage feedback resistors in the charger circuit.

Microprocessor Interface

DCINGOOD (Pin 25): Comparator Output. This open-drain output has an internal 2μA pull-up current source connected through a diode to the V_{CCP} power supply. An external pull-up resistor can be added if more pull-up current is required. This output is active high when the DC supply rises above the programmed voltage.

$\overline{\text{LOBAT}}$ (Pin 3): Comparator Output. This open-drain output does not have an internal pull-up current source and is active low when the selected battery voltage drops below the programmed voltage.

DCIN/$\overline{\text{BAT}}$ (Pin 24): Selector Input. This high impedance logic input allows the μP to make the ultimate decision on the connection of the DC power source, based upon the DCINGOOD pin information. In some minimized systems, the DCIN/$\overline{\text{BAT}}$ pin may be connected directly to the DCINGOOD pin.

$\overline{\text{BATDIS}}$ (Pin 23): Battery Disconnect Input. This high-impedance logic input has a built-in 2μA pull-up current source and allows the μP to disconnect the battery from the system.

$\overline{\text{3DM}}$ (Pin 22): Three Diode Mode Input. This high impedance logic input has no built-in pull-up current source. Connect a 100k resistor from this pin to ground to ensure three diode mode operation from a "cold start."

CHGSEL (Pin 21): Battery Charger Selector Input. This high impedance logic input has a built-in 2μA pull-up current source and allows the μP to determine which battery is being charged by connecting the selected battery to the charger output via one of the switch pairs, SW G or SW H. (The charger voltage feedback ladder is simultaneously switched to the selected battery.)

BATSEL (Pin 30): Battery Selector Input. This high impedance logic input has a built-in 2μA pull-up current source and allows the μP to select which battery is connected to the system and the battery monitor comparator input. Battery 1 is selected with a logic high on this input and battery 2 is selected with a logic low.

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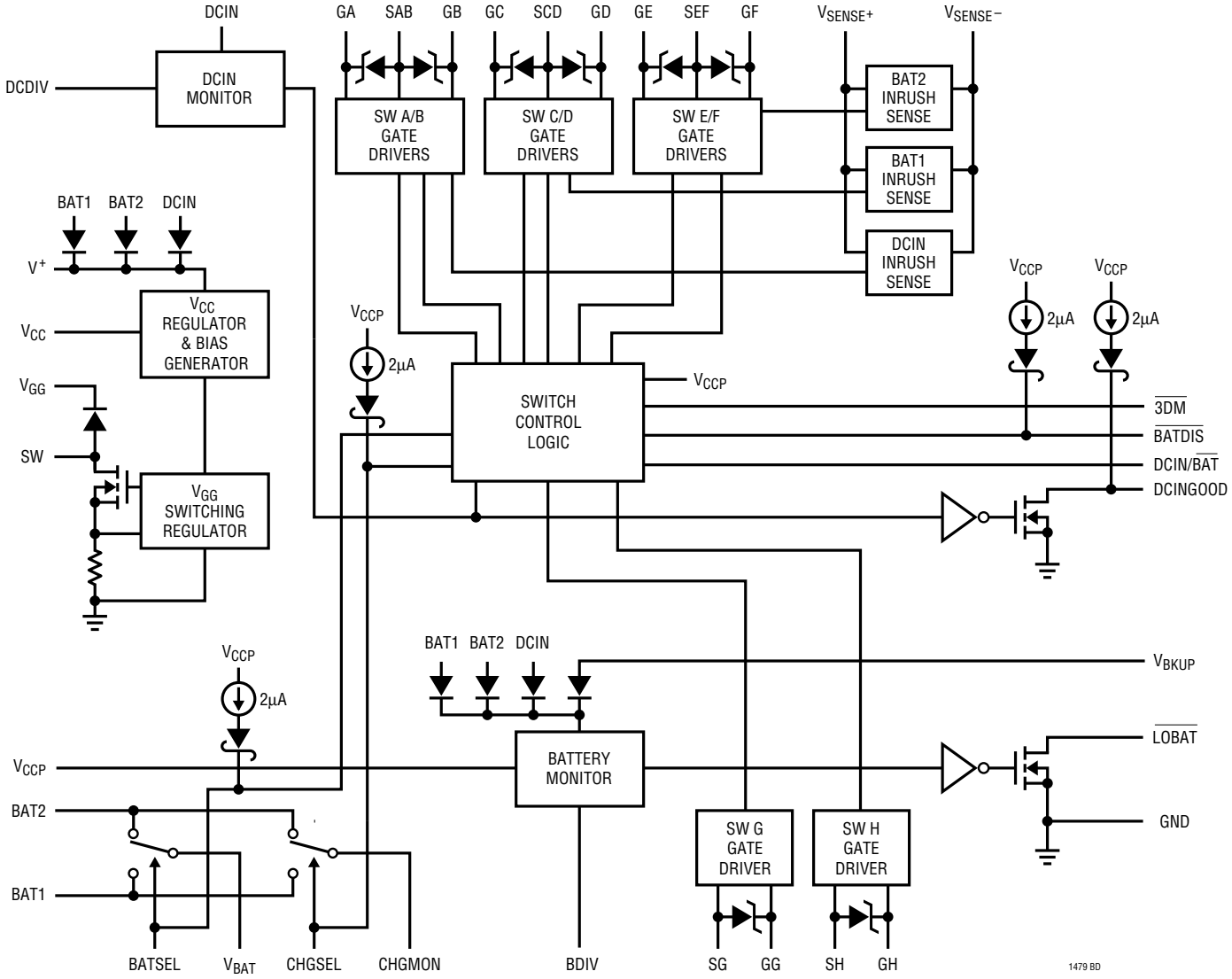
BLOCK DIAGRAM



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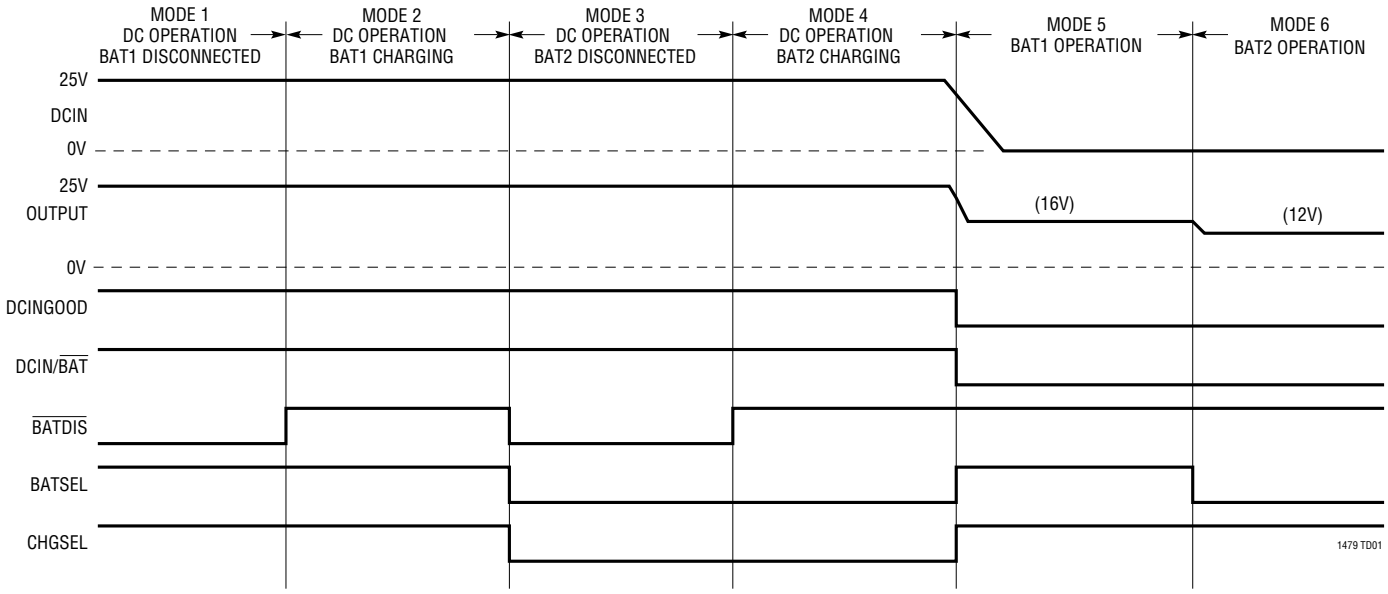
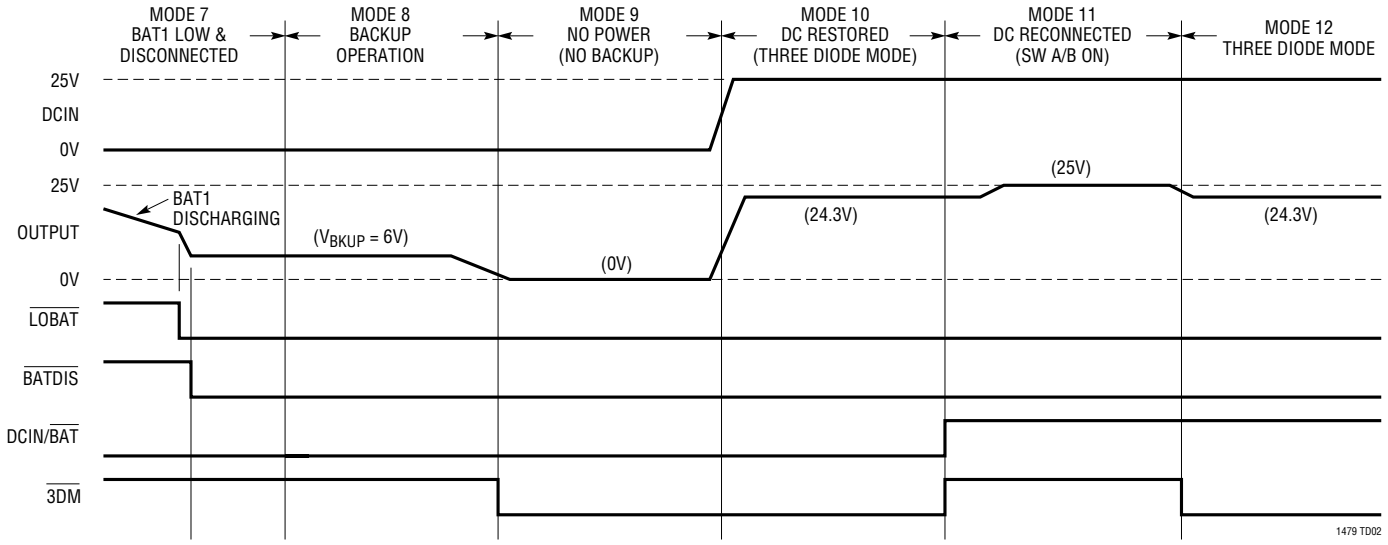
TIMING DIAGRAMS

DC and Battery Operation Timing



NOTE: FOR MODES 1 TO 6, $\overline{3DM}$ = H, BAT1 = 16V, BAT2 = 12V

Backup and DC Restoration Timing



NOTE: FOR MODES 7 TO 12, BATSEL = H, BAT1 = 16V AND DISCHARGING, BAT2 = 0V

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OPERATION

The LTC1479 is responsible for low-loss switching at the "front end" of the power management system, where up to two battery packs and a DC power source can be indiscriminately connected and disconnected. Smooth switching between input power sources is accomplished with the help of low-loss N-channel switches driven by special gate drive circuitry which limits the inrush current in and out of the battery packs and the system power supply capacitors.

All N-Channel Switching

The LTC1479 drives external back-to-back N-channel MOSFET switches to direct power from the three main power sources: the external DC power source, the primary battery and the secondary battery connected to the main supply pins—DCIN, BAT1 and BAT2 respectively. (N-channel MOSFET switches are more cost effective and provide lower voltage drops than their P-channel counterparts.)

Gate Drive (V_{GG}) Power Supply

The gate drive for the low-loss N-channel switches is supplied by a micropower boost regulator which is regulated at approximately 36.5V. The V_{GG} supply provides sufficient headroom above the maximum 28V operating voltage of the three main power sources to ensure that the MOSFET switches are fully enhanced.

The power for this inductor based regulator is taken from three internal diodes as shown in Figure 1. The three diodes are connected to each of the three main power sources, DCIN, BAT1 and BAT2. The highest voltage potential is directed to the top of the boost regulator inductor to maximize regulator efficiency. C1 provides filtering at the top of the 1mH switched inductor, L1, which is housed in a small surface mount package.

A fourth internal diode directs the current from the 1mH inductor to the V_{GG} output capacitor, C2, further reducing the external parts count. In fact, as demonstrated in Figure 1, only three external components are required by the V_{GG} regulator, L1, C1 and C2.

Inrush Current Limiting

The LTC1479 uses an adaptive inrush current limiting scheme to reduce current flowing in and out of the three main power sources and the DC/DC converter input capacitor during switch-over transitions. The voltage across a single small-valued resistor, R_{SENSE}, is measured to ascertain the instantaneous current flowing through the three main switch pairs, SW A/B, SW C/D, and SW E/F during the transitions.

Figure 2 is a block diagram showing only the DCIN switch pair, SW A/B. (The gate drive circuits for switch pairs SW C/D and SW E/F are identical). A bidirectional current sensing and limiting circuit determines when the voltage drop across R_{SENSE} reaches plus or minus 200mV. The gate-to-source voltage, V_{GS}, of the appropriate switch is limited during the transition period until the inrush current subsides, generally within a few milliseconds, depending upon the value of the DC/DC converter input capacitor.

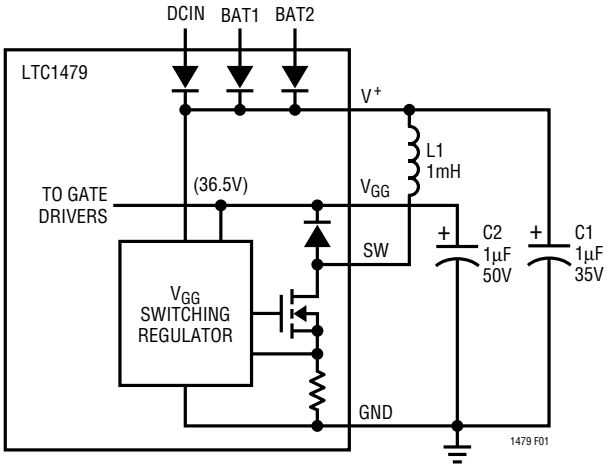

Figure 1. V_{GG} Switching Regulator

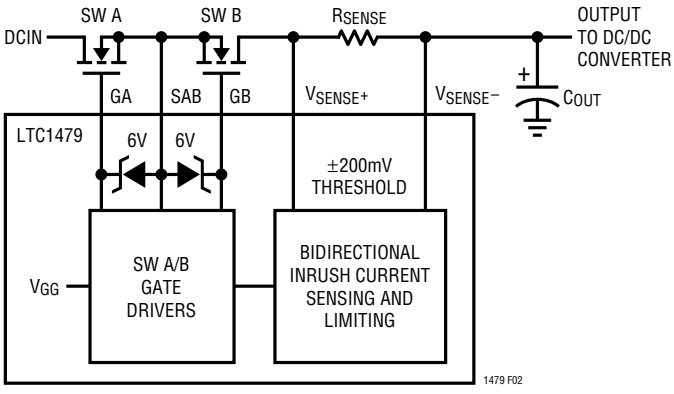

Figure 2. SW A/B Inrush Current Limiting

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OPERATION

This scheme allows capacitors and MOSFET switches of differing sizes and current ratings to be used in the same system without circuit modifications.

After the transition period has passed, the V_{GS} of both MOSFETs in the selected switch pair rises to approximately 6V. The gate drive is set at 6V to provide ample overdrive for logic level MOSFET switches without exceeding their maximum V_{GS} rating.

Internal Power Supplies

Two internal supplies provide power for the control logic and power source monitoring functions. The V_{CCP} logic supply is approximately 5V and provides power for the majority of the internal logic circuitry. The V_{CC} supply is approximately 3.60V and provides power for the V_{GG} switching regulator control circuitry and the gate drivers.

The V_{CC} supply has an undervoltage lockout circuit which minimizes power consumption in the event of a total loss of system power; i.e., when all available power sources fall below approximately 4.5V.

DCIN Voltage Monitoring

The DCIN input is continuously monitored via a two resistor ladder connected between the DCIN pin and the DCDIV input. The input threshold is 1.215V (rising edge) with approximately –35mV hysteresis. The use of a definitive voltage threshold ensures that the DC supply is not only connected but "healthy" before being attached to the DC/DC converter input.

Battery Voltage Monitoring

The LTC1479 has the ability to independently monitor both battery packs. (Because of this, one battery pack may be discharged as the other is being charged.)

A low-battery detector signals when the selected battery pack has dropped to the level where a shutdown sequence should be initiated or the other battery pack engaged.

Battery Charging Management Functions

The LTC1479 directly interfaces with LT1510/LT1511 battery charger circuits. Two gate drive circuits control the two back-to-back N-channel switch pairs, SW G and SW H, under logic (CHGSEL) control to connect the output of the charger to the selected battery pack. Break-before-make action ensures that current does not pass from one battery pack to the other during switch-over of the charger output. The CHGSEL input also simultaneously switches the positive terminal of the selected battery pack to the top of the voltage feedback resistor ladder in the charger system through the CHGMON pin.

Backup Supply Interface

Power for the LTC1479 is obtained from the backup supply when power is unavailable from the three main sources of power.

Interface to Companion Microprocessor

A companion µP must be used in conjunction with the LTC1479 to provide overall control of the power management system. The LTC1479 communicates with the µP by means of five logic inputs and two logic outputs as described in Table 1.

Table 1. LTC1479 µP Interface Inputs and Outputs

INPUT	ACTION
DCIN/$\overline{BAT}$	Logic High Required to Connect a Good DC Supply
$\overline{BATDIS}$	Logic Low Disconnects the Battery from the System
BATSEL	Selects Which Battery is Connected to the System (Logic High Selects BAT1; Logic Low Selects BAT2)
CHGSEL	Selects Which Battery is Charged and Monitored (Logic High Selects BAT1; Logic Low Selects BAT2)
$\overline{3DM}$	Forces the Main Three Power Path Switches Into "3-Diode Mode." See Applications Information Section
OUTPUT	**ACTION**
DCINGOOD	Logic High When a Good DC Supply is Present
$\overline{LOBAT}$	Logic Low When Selected Battery Voltage is Low

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APPLICATIONS INFORMATION

POWER PATH SWITCHING CONCEPTS

Power Source Selection

The LTC1479 drives low-loss switches to direct power in the main power path of a dual rechargeable battery system — the type found in most notebook computers and other portable equipment.

Figure 3 is a conceptual block diagram which illustrates the main features of an LTC1479 dual battery power management system, starting with the three main power sources and ending at the system DC/DC regulator.

Switches SW A/B, SW C/D and SW E/F direct power from either the AC adapter (DCIN) or one of the two battery packs (BAT1 and BAT2) to the input of the DC/DC switching regulator. Switches SW G and SW H connect the desired battery pack to the battery charger.

Each of the five switches is intelligently controlled by the LTC1479 which interfaces directly with a power management system µP.

Using Tantalum Capacitors

The inrush and "outrush" current of the system DC/DC regulator input capacitor is limited by the LTC1479. i.e., the current flowing both in and out of the capacitor during transitions from one input power source to another is limited. In many applications, this inrush current limiting makes it feasible to use lower cost/size tantalum surface mount capacitors in place of more expensive/larger aluminum electrolytics at the input of the DC/DC converter.

Note: The capacitor manufacturer should be consulted for specific inrush current specifications and limitations and some experimentation may be required to ensure compliance with these limitations under all possible operating conditions.

Back-to-Back Switch Topology

The simple SPST switches shown in Figure 3 actually consist of two back-to-back N-channel switches. These low-loss, N-channel switch pairs are housed in 8-pin SO and SSOP packaging and are available from a number of manufacturers. The back-to-back topology eliminates the problems associated with the inherent body diodes in power MOSFET switches and allows each switch pair to block current flow in either direction when the two switches are turned off.

The back-to-back topology also allows for independent control of each half of the switch pair which facilitates bidirectional inrush current limiting and the so called "3-diode" mode described in the following section.

The "3-Diode" Mode

Under normal operating conditions, both halves of each switch pair are turned on and off simultaneously. For example, when the input power source is switched from a good DC input (AC adapter) to a good battery pack, BAT1, both gates of switch pair SW A/B are turned off and both gates of switch pair SW C/D are turned on. The back-to-back body diodes in switch pair, SW A/B, block current flow in or out of the DC input connector.

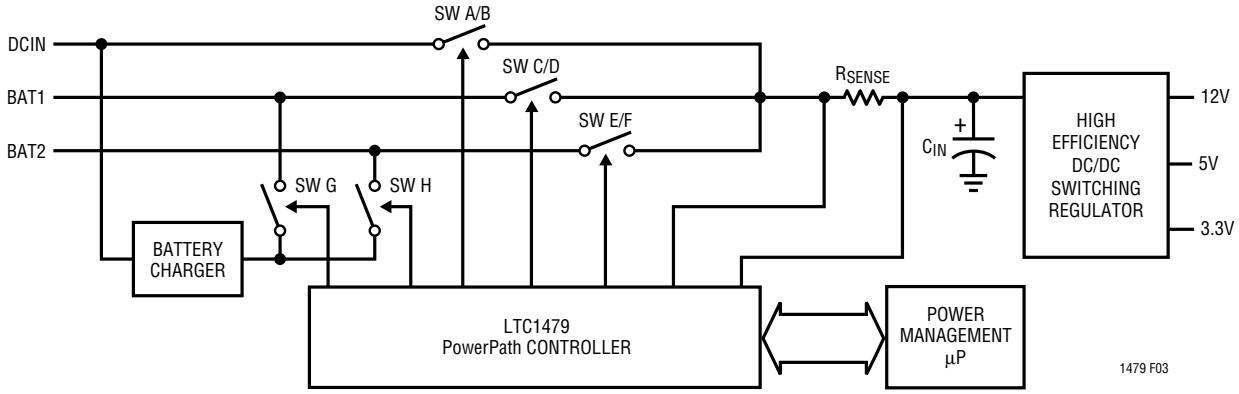

Figure 3. LTC1479 PowerPath Conceptual Diagram

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In the "3-diode" mode, only the first half of each power path switch pair, i.e., SW A, SW C and SW E, is turned on; and the second half, i.e., SW B, SW D and SW F, is turned off. These three switch pairs now act simply as three diodes connected to the three main input power sources as illustrated in Figure 4. The power 'diode' with the highest input voltage passes current through to the input of the DC/DC converter to ensure that the power management μP is powered at start-up or under abnormal operating conditions. (An undervoltage lockout circuit defeats this mode when the V^+ pin drops below approximately 4.5V).

"Cold Start" Initial Condition

The LTC1479 is designed to start in the "3- diode" mode when all five logic inputs are low—when no power is available (including the backup system). A 100k resistor from the $\overline{3DM}$ input to ground ensures that this input is low during a "cold start." This will cause the main PowerPath switches to pass the highest voltage available to the input of the DC/DC converter. Normal operation will then resume after a good power source is identified.

Recovery from Uncertain Power Conditions

The "3-diode" mode can also be asserted (by applying an active low to the $\overline{3DM}$ input) when abnormal conditions exist in the system, i.e., when all power sources are deemed not "good" or are depleted, or the management system μP is being reset or not functioning properly. (See the Power Management μP Interface section for additional information on when to invoke "3-diode" mode.)

COMPONENT SELECTION

N-Channel Switches

The LTC1479 adaptive inrush limiting circuitry permits the use of a wide range of logic-level N-channel MOSFET switches. A number of dual low $R_{DS(ON)}$ N-channel switches in 8-lead surface mount packages are available that are well suited for LTC1479 applications.

The maximum allowable drain source voltage, $V_{DS(MAX)}$, of the three main switch pairs, SW A/B, SW C/D and SW E/F, must be high enough to withstand the maximum DC supply voltage. If the DC supply is in the 20V to 28V range, use 30V MOSFET switches. If the DC supply is in the 10V to 18V range, and is well regulated, then use 20V MOSFET switches.

As a general rule, select the switch with the lowest $R_{DS(ON)}$ at the maximum allowable V_{DS}. This will minimize the heat dissipated in the switches while increasing the overall system efficiency. Higher switch resistances can be tolerated in some systems with lower current requirements, but care should be taken to ensure that the power dissipated in the switches is never allowed to rise above the manufacturer's recommended levels.

The maximum allowable drain-source voltage, $V_{DS(MAX)}$, of the two charger switch pairs, SW G and SW H, need only

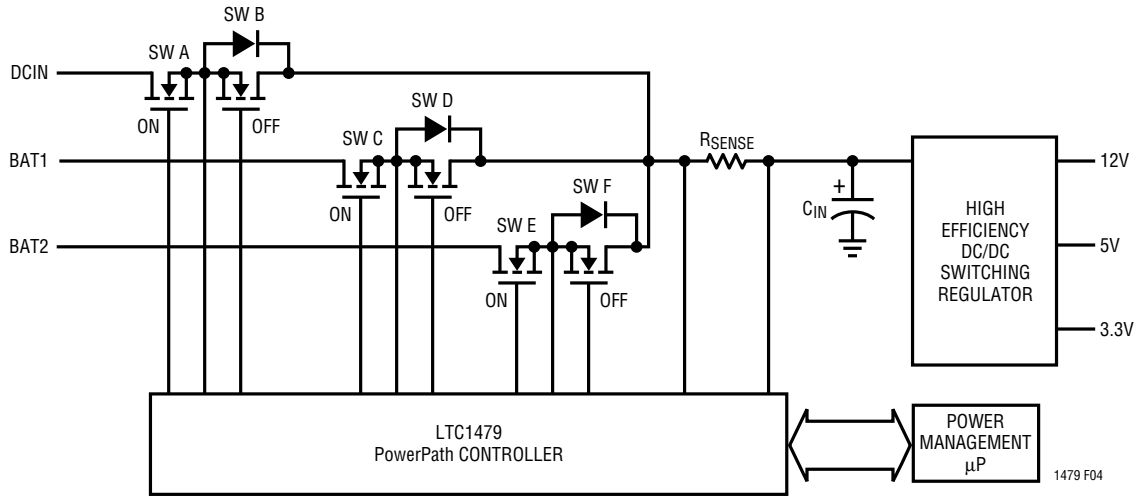

Figure 4. LTC1479 PowerPath Switches in "3-Diode" Mode

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APPLICATIONS INFORMATION

be high enough to withstand the maximum battery or charger output voltage. In most cases, this will allow the use of 20V MOSFET switches in the charger path, while 30V switches are used in the main power path.

Inrush Current Sense Resistor, R_{SENSE}

A small valued sense resistor (current shunt) is used by the three main switch pair drivers to measure and limit the inrush current flowing through the conducting switch pair.

It should be noted that the inrush limiting circuit is not intended to provide short-circuit protection; but rather, is designed to limit the large peak currents which flow into or out of the large power supply capacitors and the battery packs during power supply switch-over transitions. The inrush current limit should be set at approximately 2× or 3× the maximum required DC/DC input current.

For example, if the maximum current required by the DC/DC converter is 2A, an inrush current limit of 6A is set by selecting a 0.033Ω sense resistor, R_{SENSE}, using the following formula:

$$R_{SENSE} = (200mV)/I_{INRUSH}$$

Note that the voltage drop across the resistor in this example is only 66mV under normal operating conditions. Therefore, the power dissipated in the resistor is extremely small (132mW), and a small 1/4W surface mount resistor can be used in this application. A number of small valued, surface mount resistors are available that have been specifically designed for high efficiency current sensing applications.

DC Input Monitor Resistor Divider

The DCDIV input continuously monitors the DC power supply voltage via a two resistor divider network, R_{DC1} and R_{DC2}, as shown in Figure 5. The threshold voltage of the DC good comparator is 1.215V when the power supply input voltage is rising. Approximately –35mV of hysteresis is provided to ensure clean switching of the comparator when the DC supply voltage is falling.

To minimize errors due to the input bias current of the DC good comparator, set R_{DC1} = 12.1k so that approximately 100μA flows through the resistor divider when the desired threshold is reached. R_{DC2} is then selected according to the following formula:

$$R_{DC2} = 12.1k\left(\frac{V_{GOOD}}{1.215V} - 1\right)$$

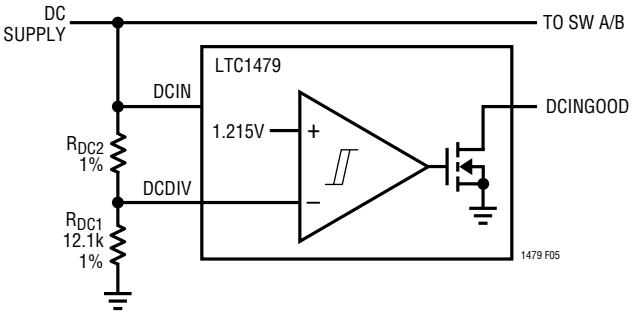

Figure 5. DC Monitor Resistor Divider

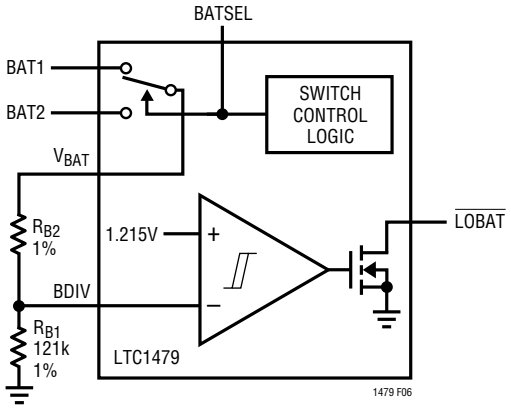

Figure 6. Battery Monitor Resistor Divider

Battery Monitor Resistor Divider

A switch controlled by the BATSEL input connects one of the two batteries to the V_{BAT} pin and therefore to the top of the battery resistor divider as shown in Figure 6. The threshold voltage of the low-battery comparator is 1.215V when the battery voltage is falling. Approximately +35mV of hysteresis is provided to ensure clean switching of the comparator when the battery voltage rises again.

To minimize errors due to the input bias current of the low battery comparator, assume R_{B1} = 121k so that approximately 10μA flows through the resistor divider when the threshold is reached. R_{B2} is selected according to the following formula:

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$$R_{B2} = 121k\left(\frac{V_{LOBAT}}{1.215V} - 1\right)$$

V_{GG} Regulator Inductor and Capacitors

The V_{GG} regulator provides a power supply voltage significantly higher than any of the three main power source voltages to allow the control of N-channel MOSFET switches. This 36.5V micropower, step-up voltage regulator is powered by the highest potential available from the three main power sources for maximum regulator efficiency.

Because the three input supply diodes and regulator output diode are built into the LTC1479, only three external components are required by the V_{GG} regulator: L1, C1 and C2 as shown in Figure 7.

L1 is a small, low current 1mH surface mount inductor. C1 provides filtering at the top of the 1mH switched inductor and should be 1µF to filter switching transients. The V_{GG} output capacitor, C2, provides storage and filtering for the V_{GG} output and should be 1µF and rated for 50V operation. C1 and C2 can be either tantalum or ceramic capacitors.

V_{CC} and V_{CCP} Regulator Capacitors

The V_{CCP} logic supply is approximately 5V and provides power for the majority of the internal logic circuitry. Bypass this output with a 0.1µF capacitor.

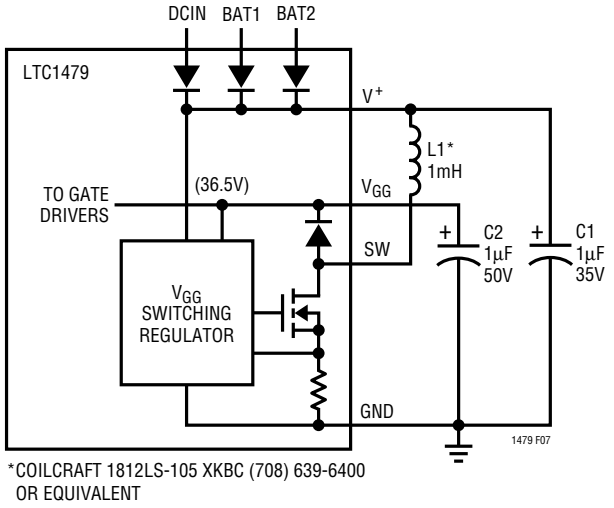

Figure 7. V_{GG} Step-Up Switch Regulator

The V_{CC} supply is approximately 3.60V and provides power for the V_{GG} switching regulator control circuitry and the gate drivers. Bypass this output with a 2.2µF tantalum capacitor. *This capacitor is required for stability of the V_{CC} regulator output.*

SYSTEM LEVEL CONSIDERATIONS

The Complete Power Management System

The LTC1479 is the "heart" of a complete power management system and is responsible for the main power path and charger switching. A companion power management µP provides overall control of the power management system in concert with the LTC1479 and the auxiliary power management systems.

A typical dual Li-Ion battery power management system is illustrated in Figure 8. If "good" power is available at the DCIN input (from the AC adapter), switch pair SW A/B are turned on—providing a low-loss path for current flow to the input of the LTC1538-AUX DC/DC converter. Switch pairs, SW C/D and SW E/F are turned off to block current from flowing back into the two battery packs from the DC input.

In this case, an LT1510 constant-voltage/constant-current (CC/CV) battery charger circuit is used to alternately charge the two Li-Ion battery packs. The µP "decides" which battery is in need of recharging by either querying the "smart" battery directly or by more indirect means. After the determination is made, either switch pair, SW G or SW H, is turned on to pass charger output current to one of the batteries. Simultaneously, the selected battery voltage is returned to the voltage feedback input of the LT1510 CV/CC battery charger via the CHGMON output of the LTC1479. After the first battery has been charged, it is disconnected from the charger circuit and the second battery is connected through the other switch pair and the second battery charged.

Backup power is provided by the LT1304 circuit which ensures that the DC/DC input voltage does not drop below 6V.

Backup System Interface

The LTC1479 is designed to work in concert with related power management products including the LT1304 mi-

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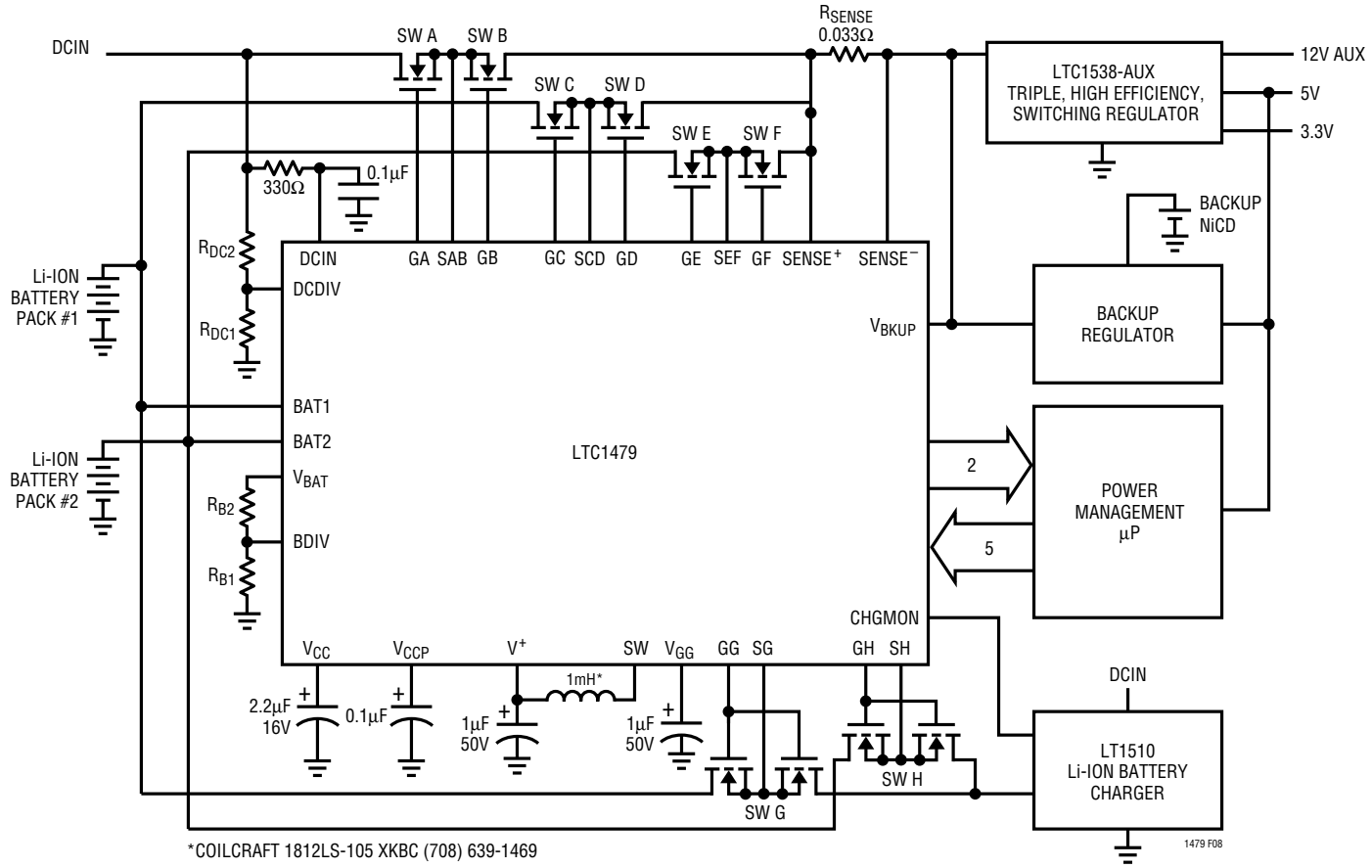

Figure 8. Simplified Dual Li-Ion Battery Power Management System

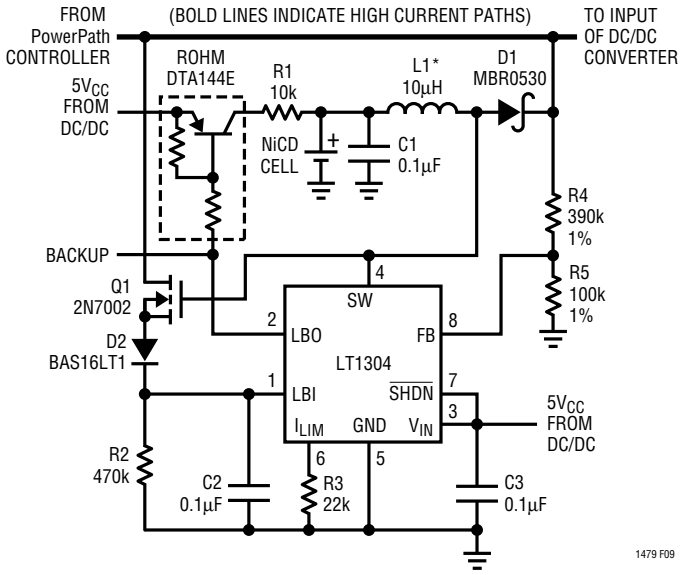

Figure 9. LT1304 Micropower Backup Converter Circuit

cropower DC/DC converter. As shown in Figure 9, the LT1304 monitors the input supply voltage and activates when it drops below 6V.

Power for the DCIN and battery monitors and the logic supply in the LTC1479 is then obtained from the output of the LT1304 step-up regulator.

Charger System Interface

The LTC1479 is designed to work directly with constant-voltage (CV), constant-current (CC) battery chargers such as the LT1510 and LT1511.

LT1510 Battery Charger Interface

As illustrated in Figure 10, the LT1510 CV/CC battery charger, takes power from the DC adapter input through Schottky diode D1. The output of the charger is directed to

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the charging battery through one of the N-channel switch pairs, SW G or SW H. The charging battery voltage is simultaneously connected through the CHGMON switch in the LTC1479 to the top of the charger voltage resistor divider, R4 and R5, for constant voltage charging. (See the LT1510 data sheet for further detail.)

LT1511 Battery Charger Interface

The LT1511, 3A CC/CV battery charger with input current limiting, is connected in a slightly different manner than the LT1510 as illustrated in Figure 11.

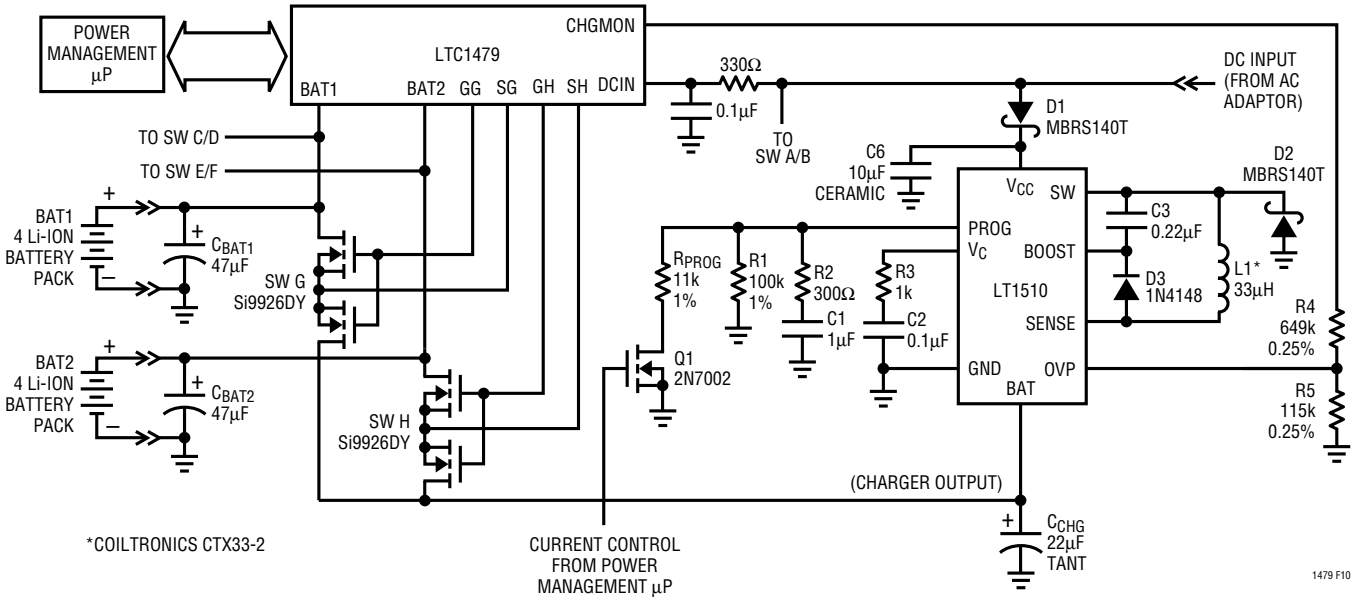

Figure 10. Interfacing to the LT1510 Constant-Voltage/Constant-Current Battery Charger

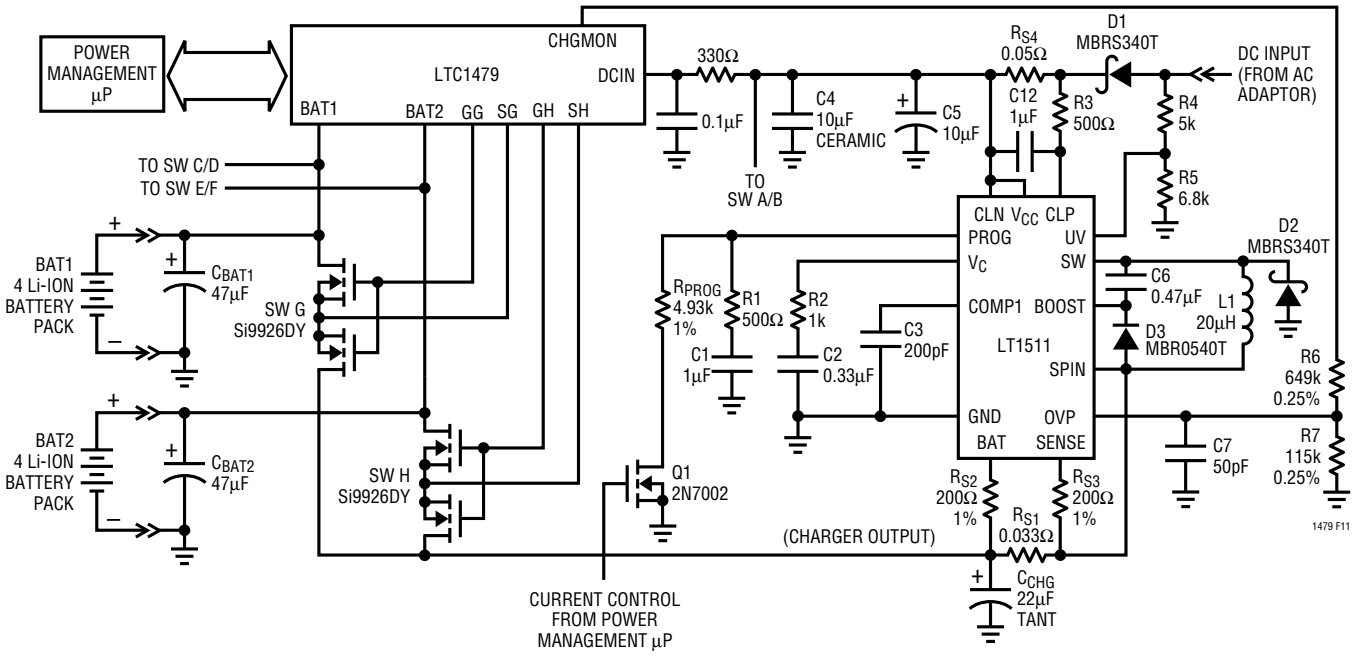

Figure 11. Interfacing to the LT1511 Constant-Voltage/Constant-Current Battery Charger with Input Current Limiting

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The LT1511 has a third control loop that regulates the current drawn from the AC adapter. Therefore, the DC input to the LTC1479 and the input to the host system through SW A/B, is obtained from the "output" of the LT1511 adapter sense resistor, R_{S4}, and not directly from the DC input connector as with the LT1510. This allows simultaneous operation of the host system while charging a battery without overloading the AC adapter. Charging current is reduced to keep the adapter current within specified levels.

However, as with the LT1510 , the output of the LT1511 is directed to the charging battery through either SW G or SW H, and the charging battery voltage is connected to the top of the voltage resistor divider, R6 and R7, for constant voltage charging. (See the LT1511 data sheet for further detail on battery charging techniques and applications hints.)

LT1620/LTC1435 Battery Charger Interface

The LTC1479 also interfaces with the LT1620/LTC1435 synchronous high efficiency low dropout battery charger. The circuit shown in Figure 12 is a constant-current/ constant-voltage battery charger specifically designed for lithium-ion applications having thermal, output current, or input voltage headroom constraints which preclude the use of other high performance chargers such as the LT1510 or LT1511.

This circuit can charge batteries at up to 4A. The precision current sensing of the LT1620 combined with the high efficiency and low dropout characteristics of the LTC1435 provide a battery charger with over 96% efficiency requiring only 0.5V input-to-output differential at 3A charging current.

Charge current programming is achieved by applying a 0μA to 100μA current from the LT1620 PROG pin to ground, which can be derived from a resistor or DAC output controlled by the power management μP. (See the LT1620 data sheet for further details on this circuit.)

Capacitive Loading on the CHGMON Output

In most applications, there is virtually no capacitive loading on the CHGMON output—just a simple resistor divider. Care should be taken to restrict the amount of capacitance to ground on the CHGMON output to less than 100pF. If more capacitance is required, it may become necessary to "mask" the $\overline{\text{LOBAT}}$ output when the charge monitor is switched between batteries. (Internal resistance between the BAT1 and BAT2 inputs and the charge monitor switch may create a transient voltage drop at the V_{BAT} output during transitions which could be falsely interpreted by the μP as a low battery condition.)

THE POWER MANAGEMENT MICROPROCESSOR

Interfacing to the LTC1479

The LTC1479 can be thought as a "real world" interface to the power management μP. It takes logic level commands directly from the μP, and makes changes at high current and high voltage levels in the power path. Further, it provides information directly to the μP on the status of the AC adapter, the batteries and the charging system.

The LTC1479 logic inputs are TTL level compatible and therefore interface directly with standard power management μPs. Further, because of the direct interface via the five logic inputs and the two logic outputs, there is virtually no latency (i.e. time delay) between the μP and the LTC1479. In this way, time critical decisions can be made by the μP without the inherent delays associated with bus protocols, etc. These delays are acceptable in certain portions of the power management system, but it is vital that the power path switching control be made through a direct connection to the power management μP. The remainder of the power management system can be easily interfaced to the μP through a serial interface.

Selecting a Power Management Microprocessor

The power management μP provides intelligence for the entire power system, is programmed to accommodate the custom requirements of each individual system and allow performance updates without resorting to costly hardware changes.

The power management μP must meet the requirements of the total power management system, including the LTC1479 controller, the batteries (and interface), the backup system, the charging system and the host processor. A number of inexpensive processors are available which can easily fulfill these requirements.

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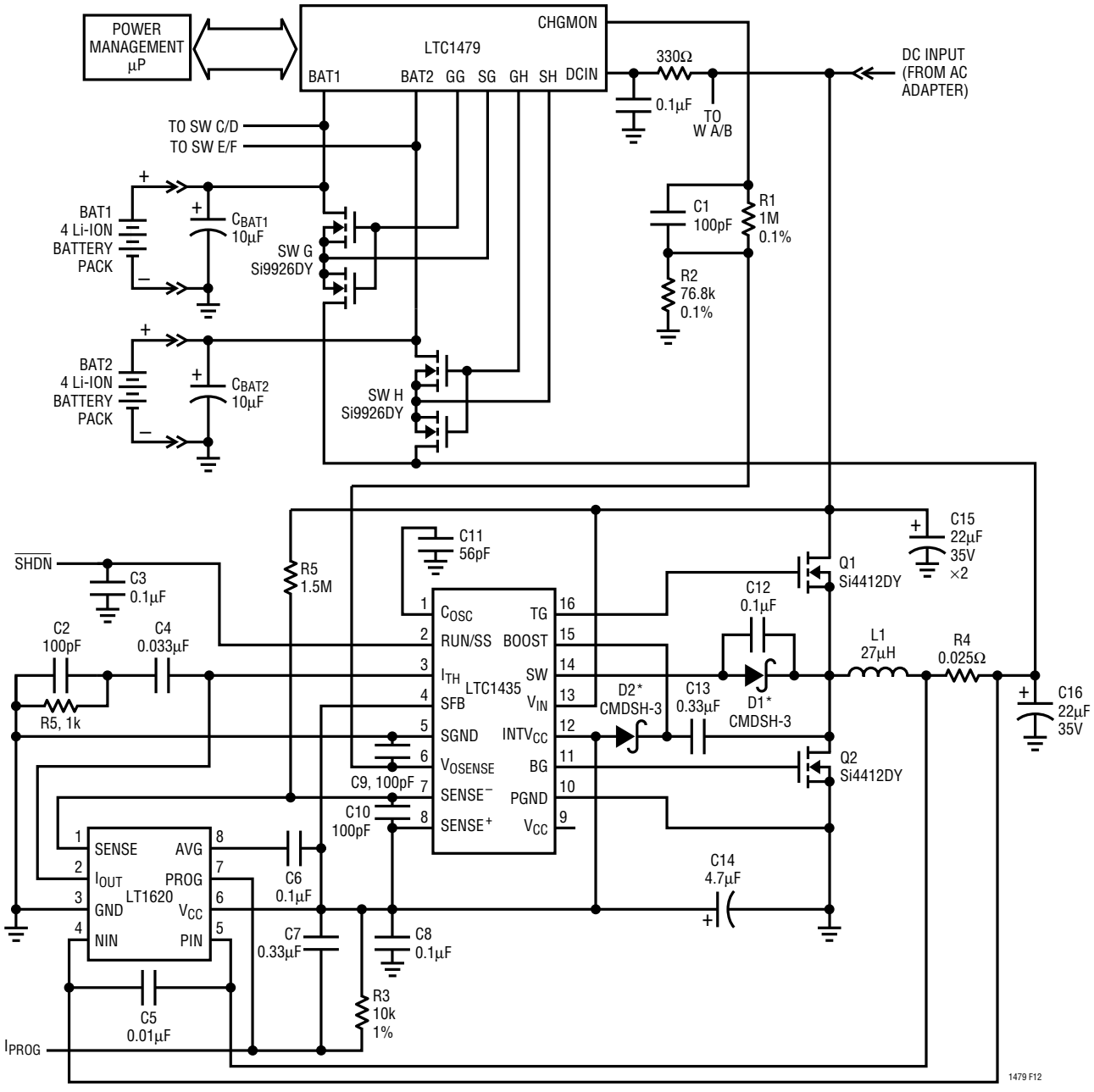

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Figure 12. Interfacing to an LT1620/LTC1435 High Efficiency Constant-Voltage/Constant-Current Battery Charger

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APPLICATIONS INFORMATION

Interfacing to the Battery Pack

The LTC1479 is designed to work with virtually any battery pack chemistry or cell count, as long as the battery pack operating voltage range is somewhere between 6V and 28V. This permits great flexibility in system design. The low-battery threshold is adjustable and can be set anywhere between 6V and 28V.

Conventional Battery Packs

Conventional battery packs do not include a "smart" battery interface between the battery pack and the host system. Thus, these battery packs generally have only three terminals to connect the battery and a temperature sensor (thermistor) to the host system. The NTC thermistor typically has a nominal resistance of 10k at room temperature and is used to monitor the battery pack temperature.

$\overline{\text{LOBAT}}$ and DCINGOOD Blanking/Filtering

It is good practice to include some delay in accepting low battery and DCIN good information during transitional periods, e.g., when switching the charger from one battery to another or when switching from batteries to DC power. This technique will eliminate false triggering at the associated µP I/O. (Remember that the "3-diode" mode may be used during periods of uncertainty to eliminate the need for "instantaneous" DCIN and battery status information.)

Smart Battery Packs

Smart battery packs, compliant with the Smart Battery System specification, have a five-terminal connector. Two of the terminals are the minus and plus connections to the battery. A third terminal is connected to the top of a thermistor in NiCd and NiMH battery packs and to a resistor in Li-Ion battery packs. A fourth and fifth terminal are connected to the Smart Management Bus (SMBus) SMBDATA and SMBCLK lines from an integrated circuit inside the battery pack.

Applications Assistance

Linear Technology applications engineers have developed a smart battery charger around the LT1511 charger IC. Contact the factory for applications assistance in developing a complete smart battery system with intelligent PowerPath control using the LTC1479.

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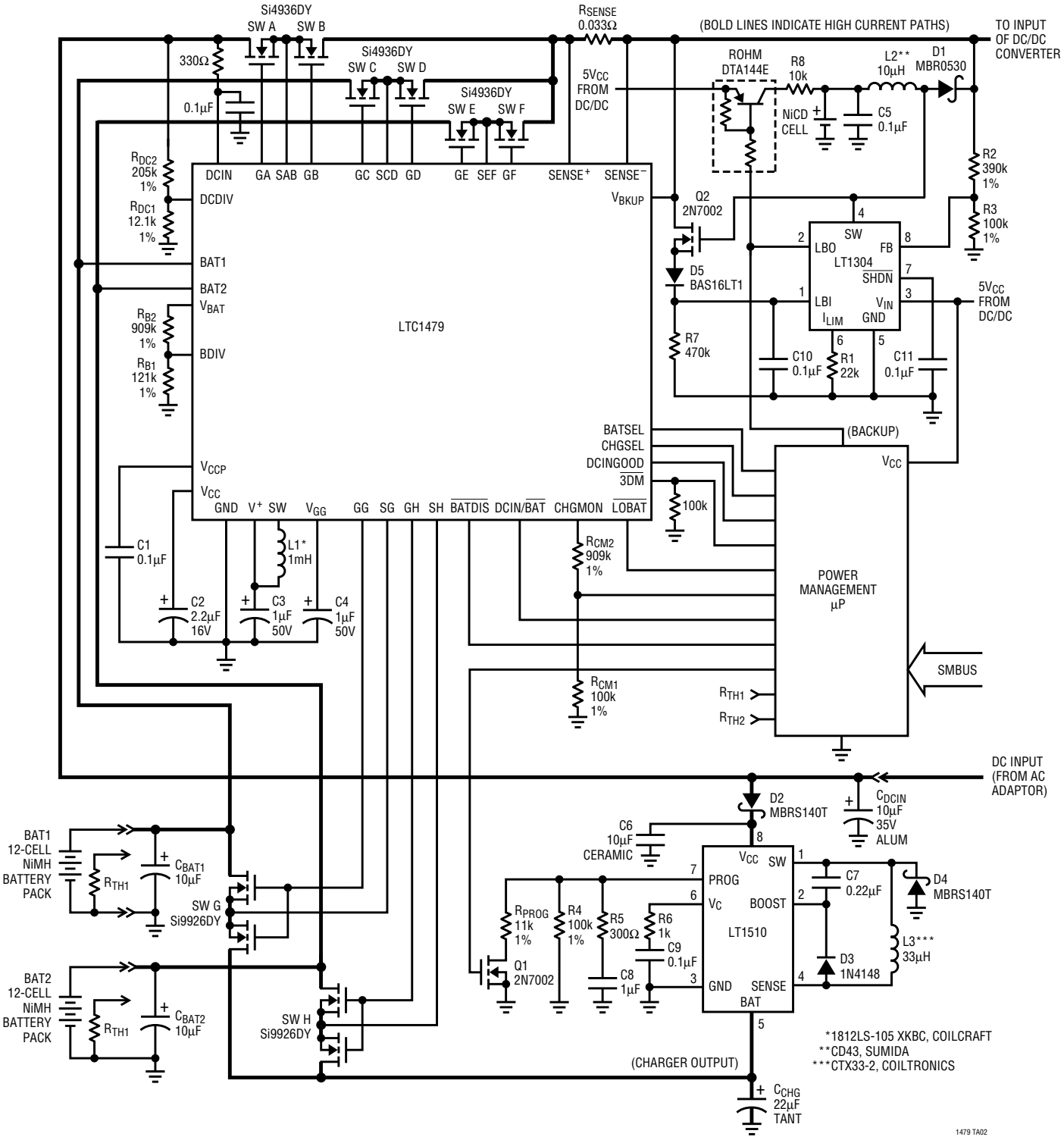
TYPICAL APPLICATIONS

Dual NiMH Battery Power Management System (Using an LT1510, 1A Charger)



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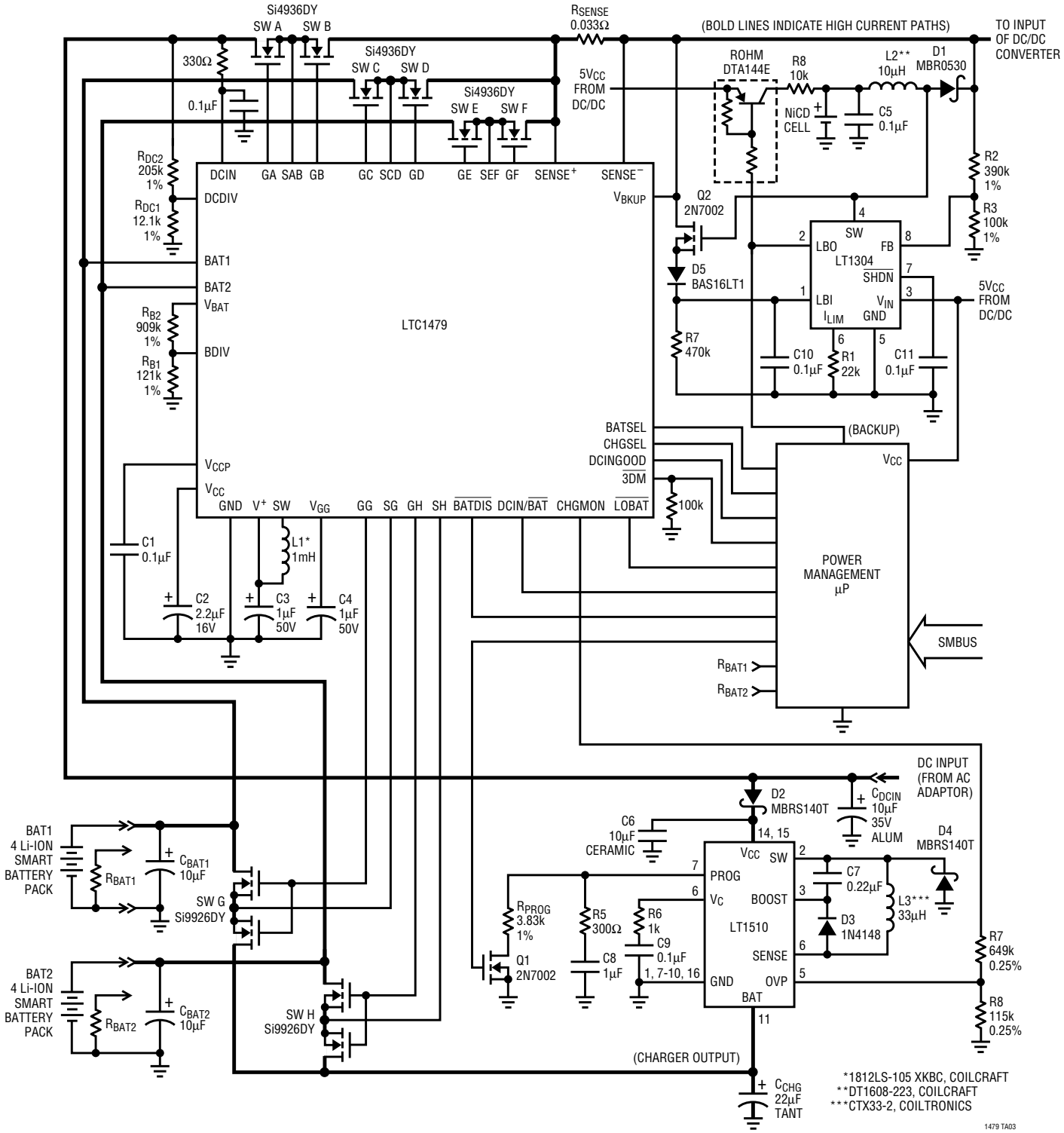
TYPICAL APPLICATIONS

Dual Li-Ion Battery Power Management System



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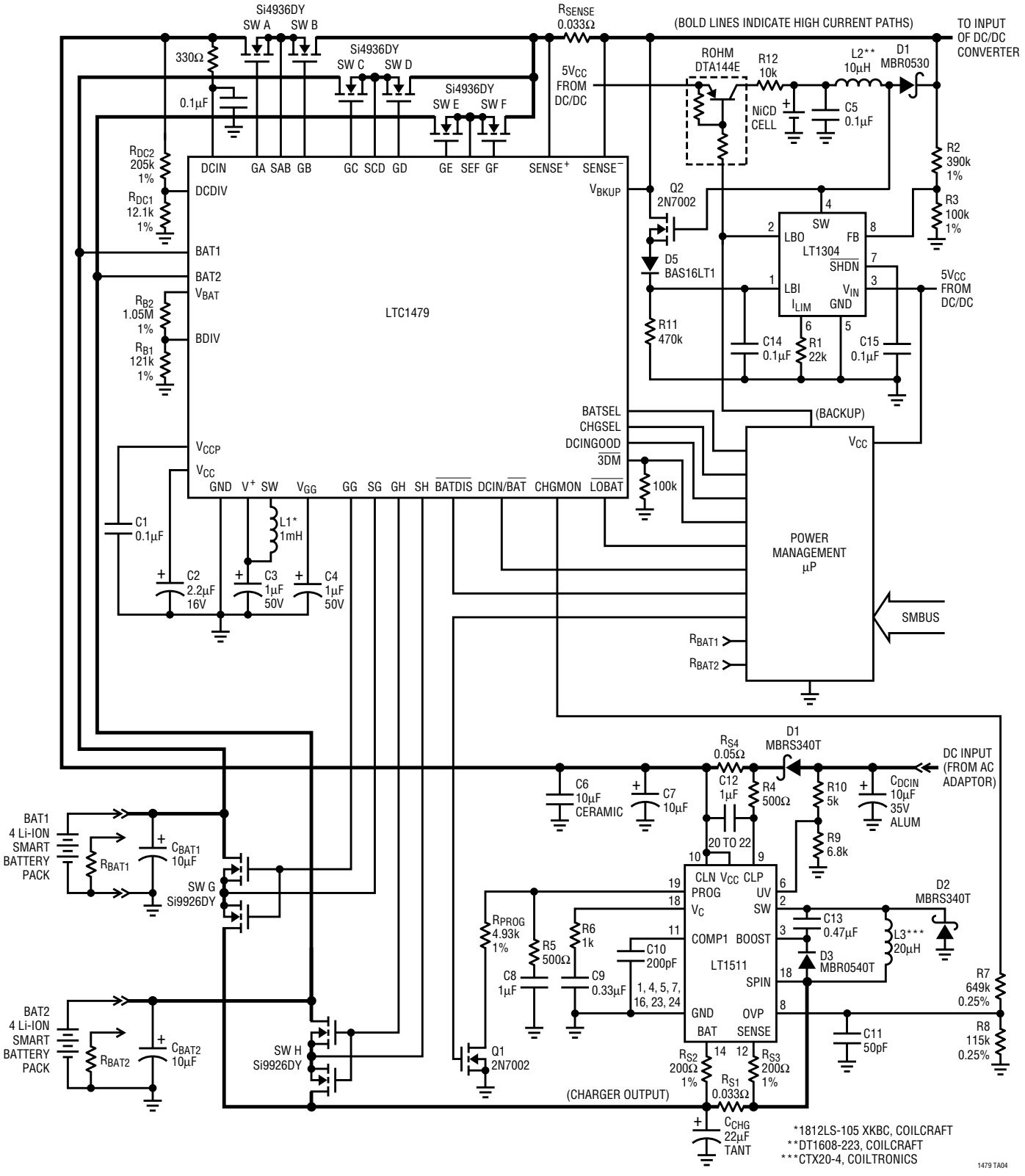
TYPICAL APPLICATIONS

Dual Li-Ion Battery Power Management System (Using an LT1511, 3A Charger)



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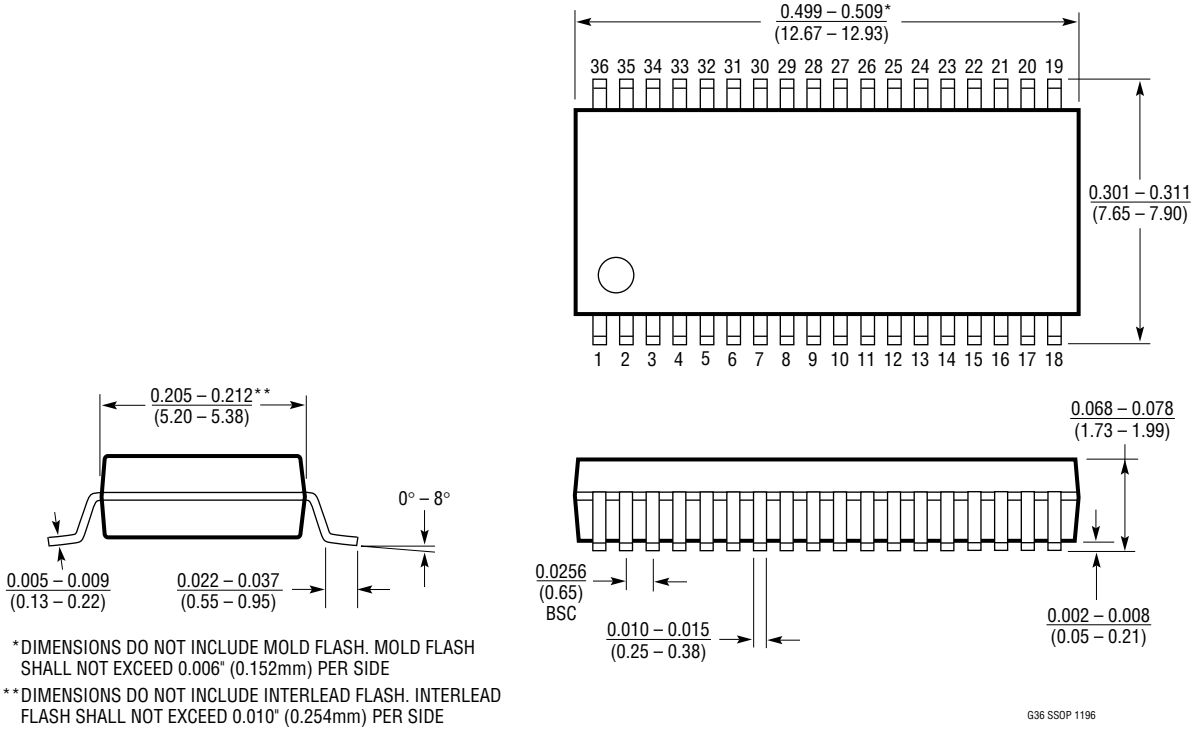
PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

G Package
36-Lead Plastic SSOP (0.209)
(LTC DWG # 05-08-1640)



*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSIONS DO NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1304	Micropower DC/DC Step-Up Converter	5V at 200mA from 2 Cells, I_Q = 10μA in Shutdown
LTC1435	High Efficiency Synchronous Step-Down Converter	Fixed Frequency, Ultrahigh Efficiency
LTC1438	Dual High Efficiency Synchronous Step-Down Converter	Fixed Frequency, PLL Lockable, Ultrahigh Efficiency
LTC1473	Dual PowerPath Switch Driver	Protected Power Management Building Block
LT1510	Constant-Voltage/Constant-Current Battery Charger	1.5A Internal Switch, Precision 0.5% Reference
LT1511	Constant-Voltage/Constant-Current 3A Battery Charger	Adapter Current Limit Loop
LTC1538-AUX	Dual, Synchronous Controller with Aux Regulator	5V Standby in Shutdown
LT1620	Battery Charger Current Controller	96% Efficiency When Used with LTC1435
LT1621	Dual Battery Charger Current Controller	For Dual Loop Applications

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