

### FEATURES

- Charges Single-Cell Li-Ion Batteries Directly from USB Port
- Load Dependent Charging Guarantees USB Input Current Compliance
- Automatic Battery Switchover When Input Supply is Removed
- Constant-Current/Constant-Voltage Operation with Thermal Feedback to Maximize Charging Rate Without Risk of Overheating\*
- Selectable 500mA/100mA Current Limit
- Low Loss Full PowerPath™ Control with Ideal Diode Operation (Reverse Current Blocking)
- Preset 4.2V Charge Voltage with 0.8% Accuracy (4.1V for LTC4055-1)
- 4.1V Float Voltage (LTC4055-1) Improves Battery Life and High Temperature Safety Margin
- USB-Compliant Suspend Mode
- Programmable Charge Current and Termination Timer
- Soft-Start Limits Inrush Current
- NTC Thermistor Input for Temperature Qualified Charging
- Tiny (4mm × 4mm × 0.75mm) QFN Package

### APPLICATIONS

- Portable USB Devices: Cameras, MP3 Players, PDAs

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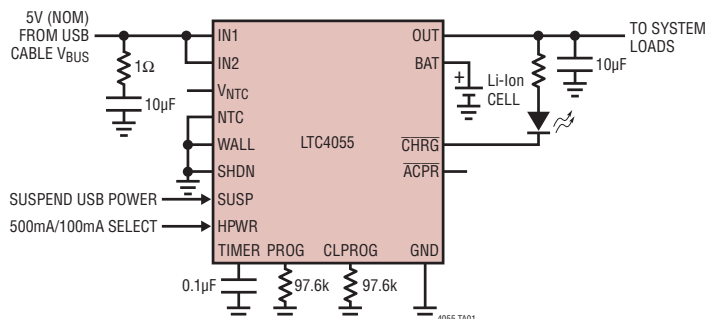
### DESCRIPTION

The LTC®4055/LTC4055-1 are USB power manager and Li-Ion battery chargers designed to work in portable battery-powered applications. The parts manage and limit the total current used by the USB peripheral for operation and battery charging. Depending on the state of the current select pin (HPWR), total input current can be limited to either 100mA or 500mA. The voltage drop from the USB supply or battery to the USB peripheral is typically less than 100mV at 400mA and 20mV at 80mA. Other management features include: automatic switchover to battery when input is removed, inrush current limiting, reverse current blocking, undervoltage lockout and thermal shutdown.

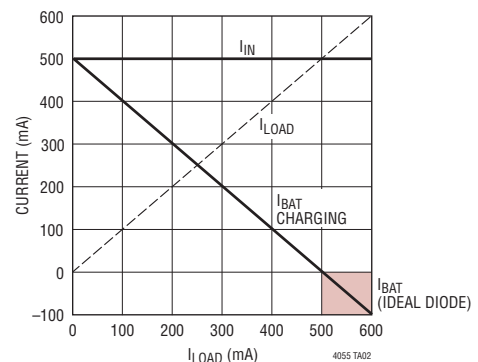
The LTC4055/LTC4055-1 include a complete constant-current/constant-voltage linear charger for single-cell Li-ion batteries. The float voltage applied to the battery is held to a tight 0.8% tolerance, and charge current is programmable using an external resistor to ground. Fully discharged cells are automatically trickle charged at 10% of the programmed current until the cell voltage exceeds 2.8V. Total charge time is programmable by an external capacitor to ground. When the battery drops 100mV below the float voltage, automatic recharging of the battery occurs. Also featured is an NTC thermistor input used to monitor battery temperature while charging.

The LTC4055/LTC4055-1 are available in a 16-pin low profile (4mm × 4mm) QFN package.

### TYPICAL APPLICATION



Input and Battery Current vs Load Current  
 $R_{PROG} = R_{CLPROG} = 97.6k$



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# LTC4055/LTC4055-1

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2, 3, 4, 5)

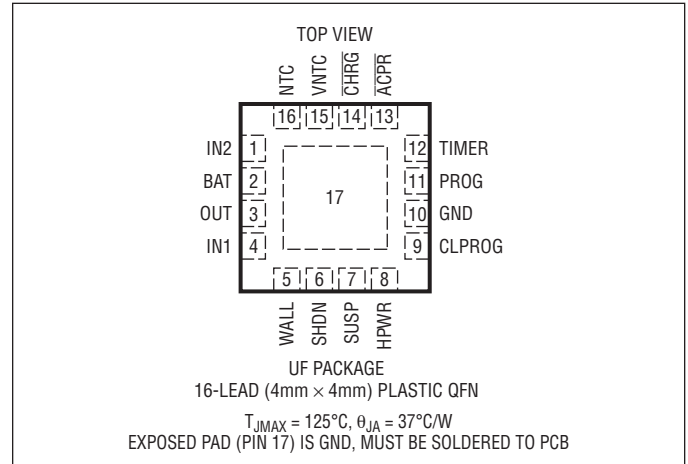
Terminal Voltage

IN1, IN2, OUT, BAT .....	-0.3V to 6V
NTC, $V_{NTC}$ , TIMER, PROG, CLPROG .....	-0.3V to (VCC + 0.3V)
CHRG, HPWR, SUSP, SHDN, WALL, ACPR .....	-0.3V to 6V
IN2 .....	$V_{IN1} + 0.1V$

Pin Current (DC)

IN1, IN2, OUT, BAT (Note 7) .....	1.6A
Operating Temperature Range .....	-40°C to 85°C
Maximum Operating Junction Temperature .....	125°C
Storage Temperature Range .....	-65°C to 125°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4055EUF#PBF	LTC4055EUF#TRPBF	4055	16-Lead (4mm × 4mm) Plastic QFN	-40°C to 85°C
LTC4055EUF-1#PBF	LTC4055EUF-1#TRPBF	40551	16-Lead (4mm × 4mm) Plastic QFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ .  $V_{IN1} = V_{IN2} = 5V$ ,  $V_{BAT} = 3.5V$ ,  $HPWR = 5V$ ,  $WALL = 0V$ ,  $R_{PROG} = R_{CLPROG} = 100k$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN}$	Input Supply Voltage	IN1, IN2 and OUT	● 4.35		5.5	V
$V_{BAT}$	Input Voltage	BAT	●		4.3	V
$I_{IN}$	Input Supply Current	$V_{BAT} = 4.2V$	●	0.8	1.6	mA
		Suspend Mode	●	50	100	$\mu A$
		Suspend Mode, Wall = 2V, $V_{OUT} = 4.8V$	●	0.1	0.2	mA
		Shutdown	●	10	20	$\mu A$
$I_{OUT}$	Output Supply Current	$V_{OUT} = 5V$ , $V_{IN1} = V_{IN2} = 0V$ , $V_{BAT} = 4.2V$	●	450	900	$\mu A$
$I_{BAT}$	Battery Drain Current	$V_{BAT} = 4.2V$ , Charging Stopped	●	15	30	$\mu A$
		Suspend Mode	●	15	30	$\mu A$
		Shutdown	●	2.5	5	$\mu A$
		$V_{IN1} = V_{IN2} = 0V$ , BAT Powers OUT, No Load	●	50	100	$\mu A$
$I_{LIM(MAX)}$	Maximum Current Limit	(Note 8)		1		A
$V_{UVLO}$	Input or Output Undervoltage Lockout	$V_{IN}$ Powers Part, Rising Threshold	● 3.5	3.8	4	V
		$V_{OUT}$ Powers Part, Rising Threshold	● 3.5	3.8	4	V
$\Delta V_{UVLO}$	Input or Output Undervoltage Lockout Hysteresis	$V_{IN}$ Rising – $V_{IN}$ Falling or $V_{OUT}$ Rising – $V_{OUT}$ Falling		125		mV

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SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Current Limit</b>						
$I_{\text{LIM}}$	Current Limit	$R_{\text{CLPROG}} = 100\text{k}$ , $\text{HPWR} = 5\text{V}$	● 465	490	515	mA
		$R_{\text{CLPROG}} = 100\text{k}$ , $\text{HPWR} = 0\text{V}$	● 89	97	105	mA
$R_{\text{ON}}$	ON Resistance $V_{\text{IN}}$ to $V_{\text{OUT}}$	$\text{HPWR} = 5\text{V}$ , 400mA Load		0.2		$\Omega$
		$\text{HPWR} = 0\text{V}$ , 80mA Load		0.2		$\Omega$
$V_{\text{PROG}}$	Programming Pin Voltage (PROG, CLPROG)	$R_{\text{CLPROG}} = R_{\text{PROG}} = 100\text{k}$	● 0.98	1.000	1.02	V
		$R_{\text{CLPROG}} = R_{\text{PROG}} = 50\text{k}$	● 0.98	1.000	1.02	V
$I_{\text{SS}}$	Soft-Start Inrush Current	IN or OUT		5		mA/ $\mu\text{s}$
$V_{\text{CLEN}}$	Input Current Limit Enable Threshold	$V_{\text{IN}}$ Rising	● 3.5	3.8	4	V
$\Delta V_{\text{CLEN}}$	Input Current Limit Enable Threshold	$V_{\text{IN}}$ Rising – $V_{\text{IN}}$ Falling		125		mV
$V_{\text{ALEN}}$	Automatic Limit Enable Threshold Voltage	$(V_{\text{IN}} - V_{\text{OUT}})$ $V_{\text{IN}}$ Rising	25	50	75	mV
		$(V_{\text{IN}} - V_{\text{OUT}})$ $V_{\text{IN}}$ Falling	-75	-50	-25	mV
<b>Battery Charger</b>						
$V_{\text{FLOAT}}$	Regulated BAT Voltage	$(0^\circ\text{C to } 85^\circ\text{C})$ $I_{\text{BAT}} = 2\text{mA}$ (LTC4055)	● 4.165	4.200	4.235	V
		$I_{\text{BAT}} = 2\text{mA}$ (LTC4055)	● 4.158	4.200	4.242	V
		$(0^\circ\text{C to } 85^\circ\text{C})$ , $I_{\text{BAT}} = 2\text{mA}$ (LTC4055-1)	● 4.066	4.100	4.134	V
$I_{\text{BAT}}$	Current Mode Charge Current	$R_{\text{PROG}} = 100\text{k}$ , $\text{HPWR} = 5\text{V}$ , No Load	● 445	485	525	mA
		$R_{\text{PROG}} = 100\text{k}$ , $\text{HPWR} = 0\text{V}$ , No Load	● 45	80	110	mA
$I_{\text{BAT}}$	Current Mode Charge Current	$R_{\text{PROG}} = 100\text{k}$ , $V_{\text{OUT}} = 5\text{V}$ , $V_{\text{IN}} = 0\text{V}$ , $V_{\text{WALL}} = 2\text{V}$	● 445	485	525	mA
		$R_{\text{PROG}} = 50\text{k}$ , $\text{HPWR} = 5\text{V}$ , No Load	● 900	980	1060	mA
		$R_{\text{PROG}} = 50\text{k}$ , $V_{\text{OUT}} = 5\text{V}$ , $V_{\text{IN}} = 0\text{V}$ , $V_{\text{WALL}} = 2\text{V}$	● 900	980	1060	mA
$I_{\text{BAT(MAX)}}$	Maximum Charge Current	(Note 8)		1		A
$\Delta I_{\text{B}}/\Delta I_{\text{O}}$	Charge Current Load Dependency	$\Delta I_{\text{BAT}}/\Delta I_{\text{OUT}}$ , $I_{\text{OUT}} = 100\text{mA}$	● 0.95	1	1.05	mA/mA
$I_{\text{TRKL}}$	Trickle-Charge Current	$V_{\text{BAT}} = 2\text{V}$ , $R_{\text{PROG}} = 100\text{k}$	30	45	60	mA
$V_{\text{TRKL}}$	Trickle-Charge Threshold Voltage	$V_{\text{BAT}}$ Rising	● 2.7	2.85	3	V
$V_{\text{CENI}}$	Input Charger Enable Threshold Voltage	$(V_{\text{IN}} - V_{\text{BAT}})$ High to Low		70		mV
		$(V_{\text{IN}} - V_{\text{BAT}})$ Low to High		80		mV
$V_{\text{CENO}}$	Output Charger Enable Threshold Voltage	$(V_{\text{OUT}} - V_{\text{BAT}})$ High to Low		70		mV
		$(V_{\text{OUT}} - V_{\text{BAT}})$ Low to High		80		mV
$V_{\text{UVCL}}$	Input/Output Undervoltage Current Limit	$I_{\text{BAT}} = I_{\text{CHG}}/2$	● 4.23	4.3	4.37	V
$V_{\text{RECHRG}}$	Recharge Battery Threshold Voltage	$V_{\text{FLOAT}} - V_{\text{RECHRG}}$	● 65	100	135	mV
$t_{\text{TIMER}}$	TIMER Accuracy	$C_{\text{TIMER}} = 0.1\mu\text{F}$		$\pm 10$		%
	Recharge Time	Percent of Total Charge Time		50		%
	Low Battery Trickle-Charge Time	Percent of Total Charge Time, $V_{\text{BAT}} < 2.8\text{V}$		25		%
$T_{\text{LIM}}$	Junction Temperature in Constant Temperature Mode			105		$^\circ\text{C}$
<b>Ideal Diode</b>						
$R_{\text{FWD}}$	On Resistance, $V_{\text{ON}}$ Regulation	$V_{\text{BAT}} = 3.5\text{V}$ , 100mA Load		0.1		$\Omega$
$R_{\text{DIO,ON}}$	On Resistance $V_{\text{BAT}}$ to $V_{\text{OUT}}$	$V_{\text{BAT}} = 3.5\text{V}$ , 600mA Load		0.2		$\Omega$
$V_{\text{FWD}}$	Voltage Forward Drop ( $V_{\text{BAT}} - V_{\text{OUT}}$ )	$V_{\text{BAT}} = 3.5\text{V}$ , 5mA Load	● 10	30	50	mV
		$V_{\text{BAT}} = 3.5\text{V}$ , 100mA Load		55		mV
		$V_{\text{BAT}} = 3.5\text{V}$ , 600mA		120		mV
$V_{\text{OFF}}$	Diode Disable Battery Voltage	$V_{\text{BAT}}$ Falling		2.8		V
$I_{\text{FWD}}$	Load Current Limit for $V_{\text{ON}}$ Regulation	$V_{\text{IN}} = 3.5\text{V}$		550		mA
$I_{\text{MAX}}$	Diode Current Limit	$V_{\text{BAT}} = 3.5\text{V}$ , $V_{\text{OUT}} = 2.8\text{V}$ , Pulsed with 10% Duty Cycle	1.4	1.8	2.2	A

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN1} = V_{IN2} = 5\text{V}$ ,  $V_{BAT} = 3.5\text{V}$ ,  $\text{HPWR} = 5\text{V}$ ,  $\text{WALL} = 0\text{V}$ ,  $R_{\text{PROG}} = R_{\text{CLPROG}} = 100\text{k}$ , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Logic</b>							
$V_{OL}$	Output Low Voltage ( $\overline{\text{CHRG}}$ , $\overline{\text{ACPR}}$ )	$I_{\text{SINK}} = 5\text{mA}$	●	0.2	0.4	V	
$V_{IH}$	Enable Input High Voltage	SUSP, SHDN, HPWR Pin Low to High	●		1.2	V	
$V_{IL}$	Enable Input Low Voltage	SUSP, SHDN, HPWR Pin High to Low	●	0.4		V	
$I_{\text{PULLDN}}$	Logic Input Pull-Down Current	SUSP, SHDN, HPWR		2		$\mu\text{A}$	
$V_{\text{CHG,SD}}$	Charger Shutdown Threshold Voltage on TIMER	TIMER Falling	●	0.15	0.4	V	
$I_{\text{CHG,SD}}$	Charger Shutdown Pull-Up Current on TIMER	$V_{\text{TIMER}} = 0\text{V}$	●	2	4	$\mu\text{A}$	
$V_{\text{WALL}}$	Wall Input Threshold Voltage	$V_{\text{WALL}}$ Rising Threshold	●	0.98	1.000	1.02	V
$V_{\text{WALL,HYS}}$	Wall Input Hysteresis	$V_{\text{WALL}}$ Rising – $V_{\text{WALL}}$ Falling Threshold		35		mV	
$I_{\text{WALL}}$	Wall Input Leakage Current	$V_{\text{WALL}} = 1\text{V}$		0	$\pm 50$	nA	
<b>NTC</b>							
$I_{\text{VNTC}}$	$V_{\text{NTC}}$ Pin Current	$V_{\text{VNTC}} = 2.5\text{V}$	●	1.5	2.5	3.5	mA
$V_{\text{VNTC}}$	$V_{\text{NTC}}$ Bias Voltage	$I_{\text{VNTC}} = 500\mu\text{A}$	●	3.4	3.8		V
$V_{\text{COLD}}$	Cold Temperature Fault Threshold Voltage	Rising Threshold		$0.74 \cdot V_{\text{VNTC}}$		V	
		Falling Threshold		$0.72 \cdot V_{\text{VNTC}}$		V	
$V_{\text{HOT}}$	Hot Temperature Fault Threshold Voltage	Falling Threshold		$0.29 \cdot V_{\text{VNTC}}$		V	
		Rising Threshold		$0.30 \cdot V_{\text{VNTC}}$		V	
$V_{\text{DIS}}$	NTC Disable Voltage	NTC Input Voltage to GND (Falling) Hysteresis	●	75	100 50	125	mV mV

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:**  $V_{\text{CC}}$  is the greater of  $V_{\text{IN1}}$ ,  $V_{\text{OUT}}$  or  $V_{\text{BAT}}$ .

**Note 3:** IN1 and IN2 should be tied together with a low impedance to ensure that the difference between the two pins does not exceed 100mV.

**Note 4:** All voltage values are with respect to GND.

**Note 5:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed  $125^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

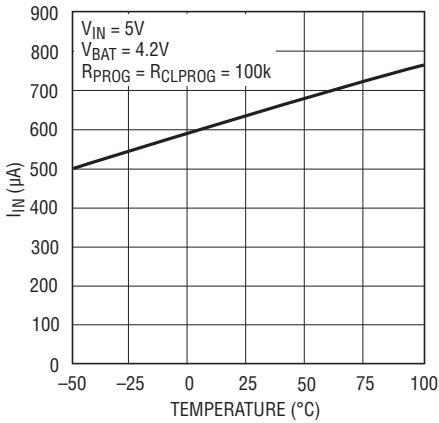
**Note 6:** The LTC4055EUF/LTC4055EUF-1 are guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $85^\circ\text{C}$ . Specifications over the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operating temperature range are assured by design, characterization and correlation with statistical process controls.

**Note 7:** Guaranteed by long-term current density limitations.

**Note 8:** Accuracy of programmed current may degrade for currents greater than 1A.

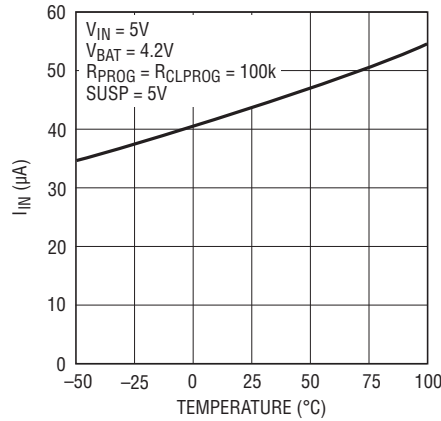
# TYPICAL PERFORMANCE CHARACTERISTICS

**Input Supply Current vs Temperature**



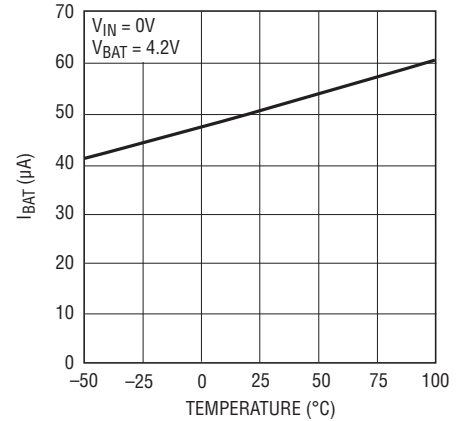
4055 G01

**Input Supply Current vs Temperature (Suspend Mode)**



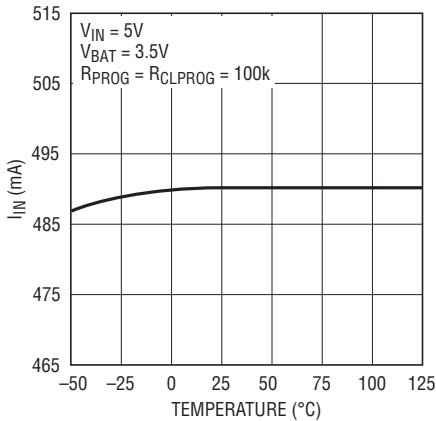
4055 G02

**Battery Drain Current vs Temperature (BAT Powers OUT, No Load)**



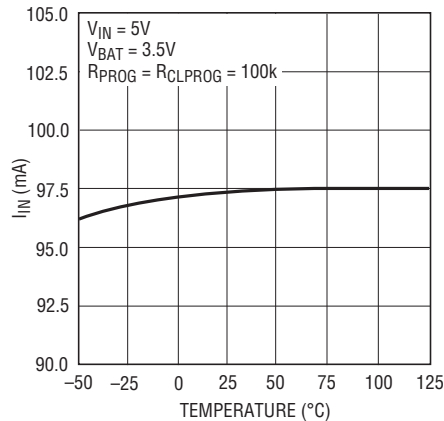
4055 G03

**Input Current Limit vs Temperature, HPWR = 5V**



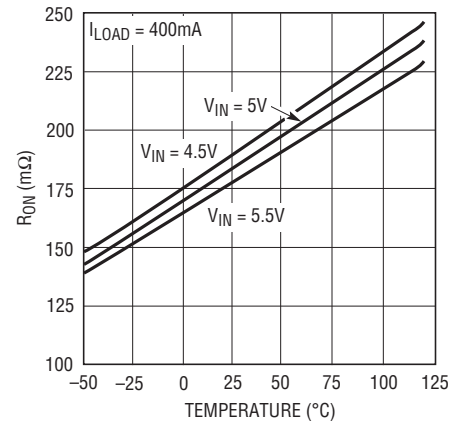
4055 G04

**Input Current Limit vs Temperature, HPWR = 0V**



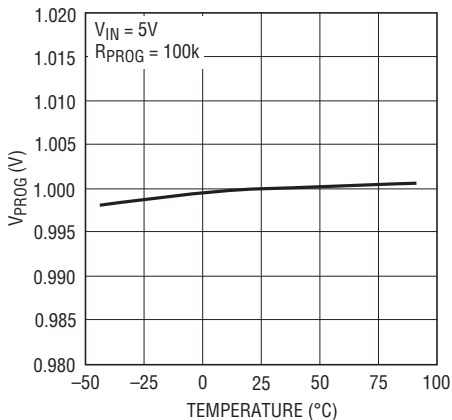
4055 G05

**R\_ON vs Temperature**



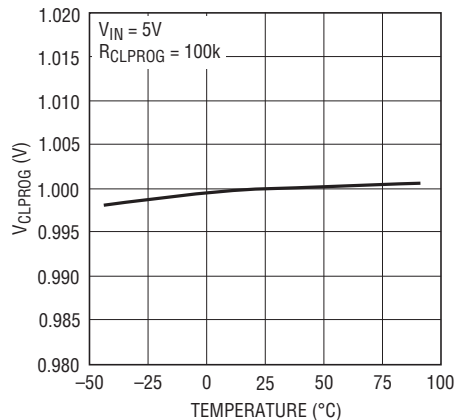
4055 G06

**PROG Pin Voltage vs Temperature**



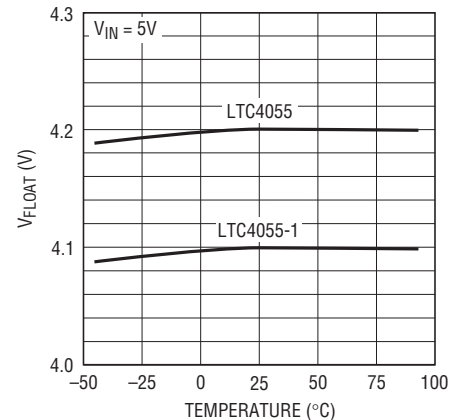
4055 G07

**CLPROG Pin Voltage vs Temperature**



4055 G08

**Battery Regulated Output (Float) Voltage vs Temperature**

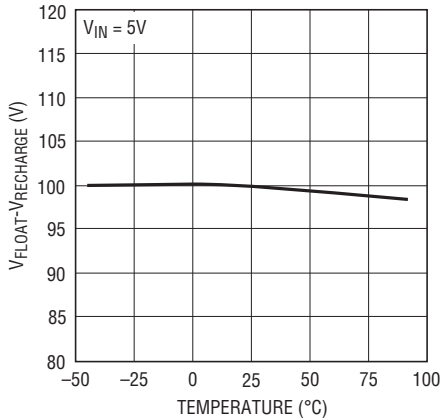


4055 G09

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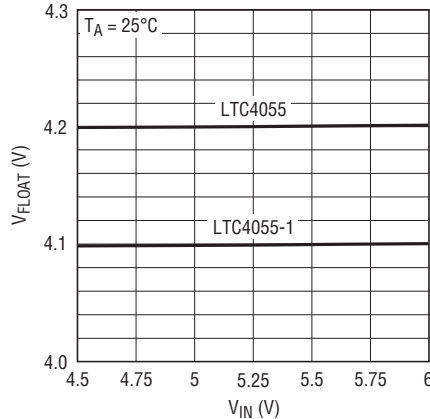
## TYPICAL PERFORMANCE CHARACTERISTICS

**Regulated Output Voltage-Recharge Threshold Voltage vs Temperature**



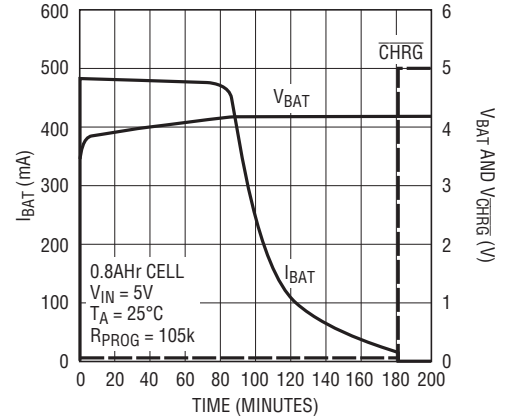
4055 G10

**Battery Regulated Output (Float) Voltage vs Supply Voltage**



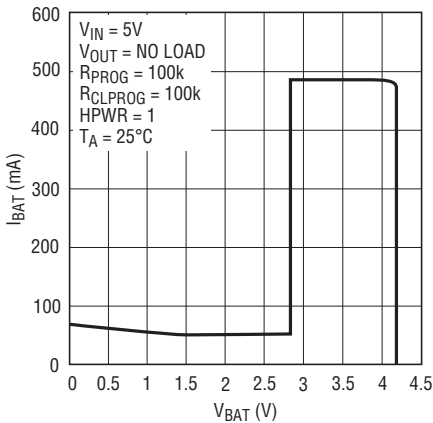
4055 G11

**Battery Current and Voltage vs Time (LTC4055)**



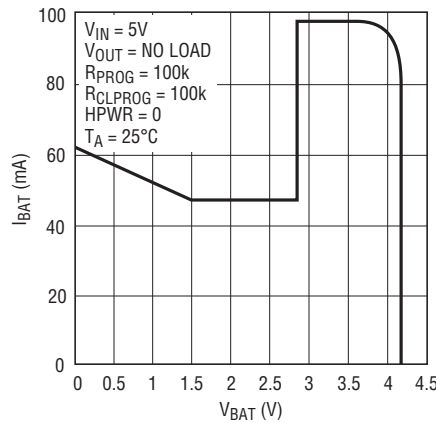
4055 G12

**Charging from USB,  $I_{BAT}$  vs  $V_{BAT}$  (LTC4055)**



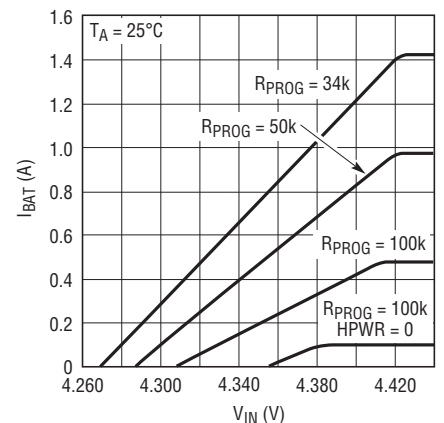
4055 G13

**Charging from USB, Low Power,  $I_{BAT}$  vs  $V_{BAT}$  (LTC4055)**



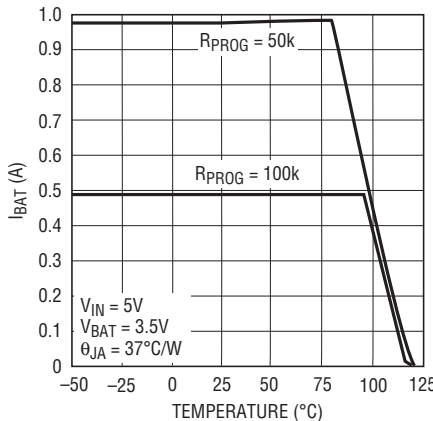
4055 G14

**Undervoltage Current Limit, Charging from  $V_{IN}$ ,  $I_{BAT}$  vs  $V_{IN}$**



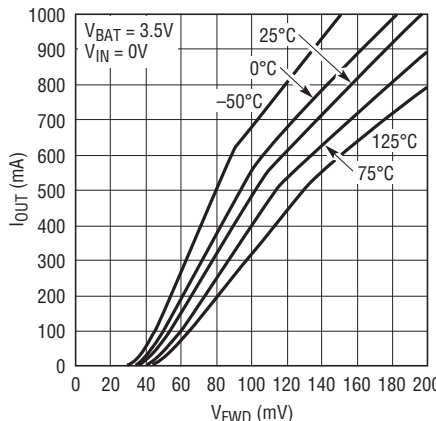
4055 G15

**Charge Current vs Temperature (Thermal Regulation)**



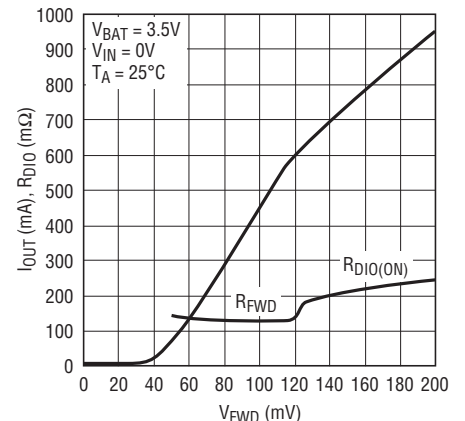
4055 G16

**Ideal Diode Forward Voltage vs Current and Temperature**



4055 G17

**Ideal Diode Forward Voltage and Resistance vs Current**

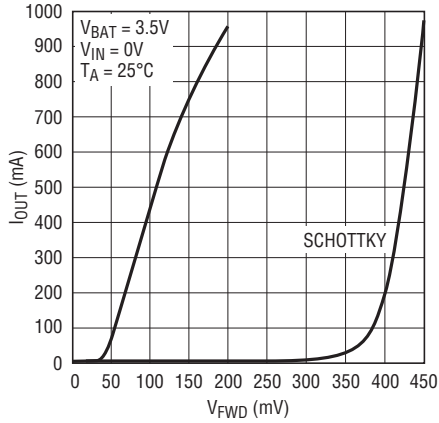


4055 G18

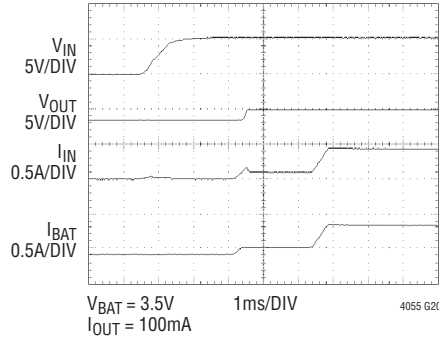
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# TYPICAL PERFORMANCE CHARACTERISTICS

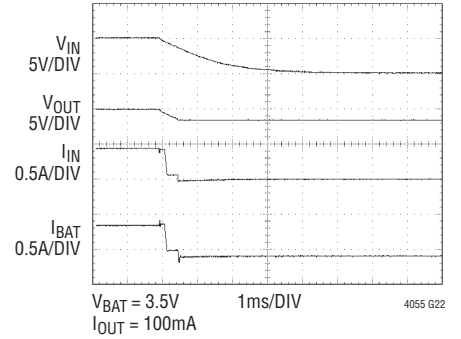
**Ideal Diode and Schottky Diode Forward Voltage vs Current**



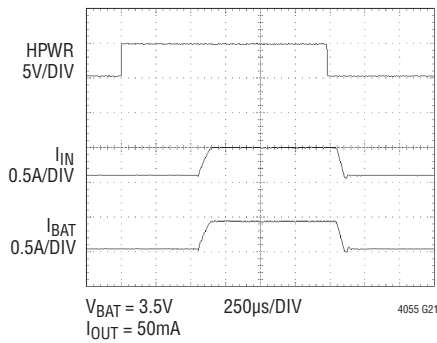
**Input Connect Waveforms**



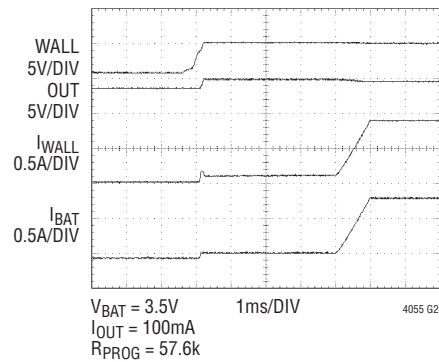
**Input Disconnect Waveforms**



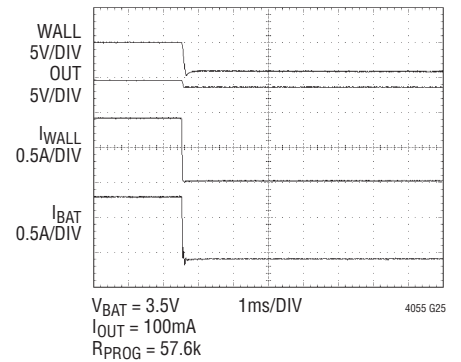
**Response to HPWR**



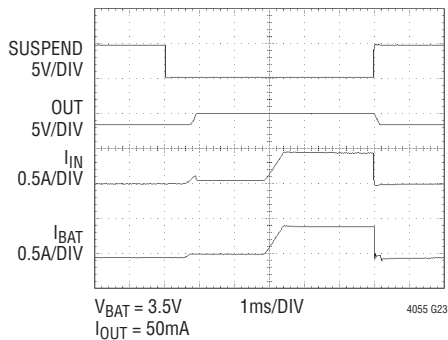
**WALL Connect Waveforms ( $V_{IN} = 0V$ )**



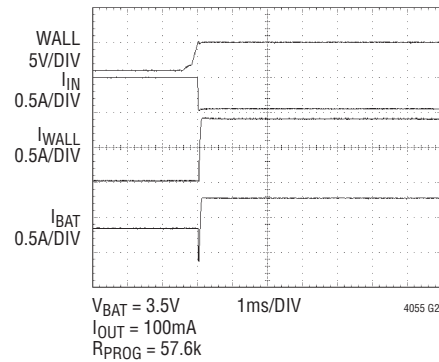
**WALL Disconnect Waveforms ( $V_{IN} = 0V$ )**



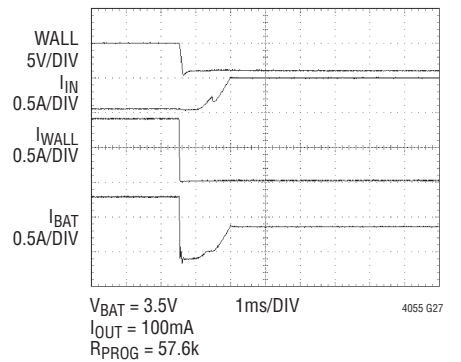
**Response to Suspend**



**WALL Connect Waveforms ( $V_{IN} = 5V$ )**



**WALL Disconnect Waveforms ( $V_{IN} = 5V$ )**





## PIN FUNCTIONS

**BAT (Pin 2):** Connect to a single-cell Li-Ion battery. Used as an output when charging the battery and as an input when supplying power to OUT. When the OUT pin potential drops below the BAT pin potential, an ideal diode function connects BAT to OUT and prevents  $V_{OUT}$  from dropping more than 100mV below  $V_{BAT}$ . A precision internal resistor divider sets the final float potential on this pin. The internal resistor divider is disconnected when IN1/IN2 and OUT are in UVLO.

**OUT (Pin 3):** Voltage Output. Used to provide controlled power to a USB device from either USB  $V_{BUS}$  (IN1/IN2) or the battery (BAT) when the USB is not present. Can also be used as an input for battery charging when the USB is not present and a wall adaptor is applied to this pin. Should be bypassed with at least 10 $\mu$ F to GND.

**IN1/IN2 (Pin 4/Pin 1):** Input Supply. Connect to USB supply,  $V_{BUS}$ . Used as main supply while connected to USB  $V_{BUS}$  for power control to a USB device. Input current is limited to either 20% or 100% of the current programmed by the CLPROG pin as determined by the state of the HPWR pin. Charge current (to BAT pin) supplied through the inputs is set to the current programmed by the PROG pin but will be limited by the input current limit if set greater than the input current limit.

Connect IN2 to IN1 with a resistance no greater than 0.05 $\Omega$ .

**WALL (Pin 5):** Wall Adapter Present Input. Pulling this pin above 1V will disable charging from IN1/IN2 and disconnect the power path from IN1/IN2 to OUT. The  $\overline{ACPR}$  pin will also be pulled low to indicate that a wall adapter has been detected. Requires the voltage on IN1/IN2 or OUT to be 100mV greater than  $V_{BAT}$  and greater than  $V_{UVLO}$  to activate this function.

**SHDN (Pin 6):** Shutdown Input. Pulling this pin greater than 1.2V will disable the entire part and place it in a low supply current mode of operation. All power paths will be disabled. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the input is not being driven externally.

**SUSP (Pin 7):** Suspend Mode Input. Pulling this pin above 1.2V will disable charging from IN1/IN2 and disconnect the power path from IN1/IN2 to OUT. The supply current will be reduced to comply with the USB specification for Suspend mode. The BAT to OUT ideal diode function will remain active as well as the ability to charge the battery from OUT. Suspend mode will reset the charge timer if  $V_{OUT}$  is less than  $V_{BAT}$  while in suspend mode. If  $V_{OUT}$  is kept greater than  $V_{BAT}$ , such as when a wall adapter is present, the charge timer will not be reset when the part is put in suspend. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the input is not being driven externally.

**HPWR (Pin 8):** High Power Select. Used to control the amount of current drawn from the USB port. A voltage greater than 1.2V on the pin will set the current limit to 100% of the current programmed by the CLPROG pin and 100% of the charge current programmed by the PROG pin. A voltage less than 0.4V on the pin will set the current limit to 20% of the current programmed by the CLPROG pin and decrease battery charge current to 16% of the current programmed by the CLPROG pin. A weak pull-down current is internally applied to this pin to ensure it is low at power-up when the input is not being driven externally.

**CLPROG (Pin 9):** Current Limit Program. Connecting a resistor,  $R_{CLPROG}$  to ground, programs the input to output current limit. The current limit is programmed as follows:

$$I_{CL}(A) = \frac{V_{CLPROG}}{R_{CLPROG}} \cdot 49,000 = \frac{49,000V}{R_{CLPROG}}$$

In USB applications the resistor  $R_{CLPROG}$  should be set to no less than 105k.

**GND (Pin 10):** Ground.

**PROG (Pin 11):** Charge Current Program. Connecting a resistor,  $R_{PROG}$ , to ground programs the battery charge current. The battery charge current is programmed as follows:

$$I_{CHG}(A) = \frac{V_{PROG}}{R_{PROG}} \cdot 48,500 = \frac{48,500V}{R_{PROG}}$$



## PIN FUNCTIONS

**TIMER (Pin 12):** Timer Capacitor. Placing a capacitor  $C_{\text{TIMER}}$  to GND sets the timer period. The timer period is:

$$t_{\text{TIMER}}(\text{Hours}) = \frac{C_{\text{TIMER}} \cdot R_{\text{PROG}} \cdot 3 \text{ Hours}}{0.1\mu\text{F} \cdot 100\text{k}}$$

Charge time is increased as charge current is reduced due to input voltage regulation, load current and current limit selection (HPWR).

Shorting the TIMER pin to GND disables the battery charging functions.

**ACPR (Pin 13):** Wall Adapter Present Output. Active low open-drain output pin. A low on this pin indicates that the wall adapter input comparator has had its input pulled above the input threshold and power is present on IN1/IN2 or OUT (i.e., above UVLO threshold).

**CHRG (Pin 14):** Open-Drain Charge Status Output. When the battery is being charged, the CHRG pin is pulled low by an internal N-channel MOSFET. When the timer runs out or the input supply or output supply is removed, the CHRG pin is forced to a high impedance state.

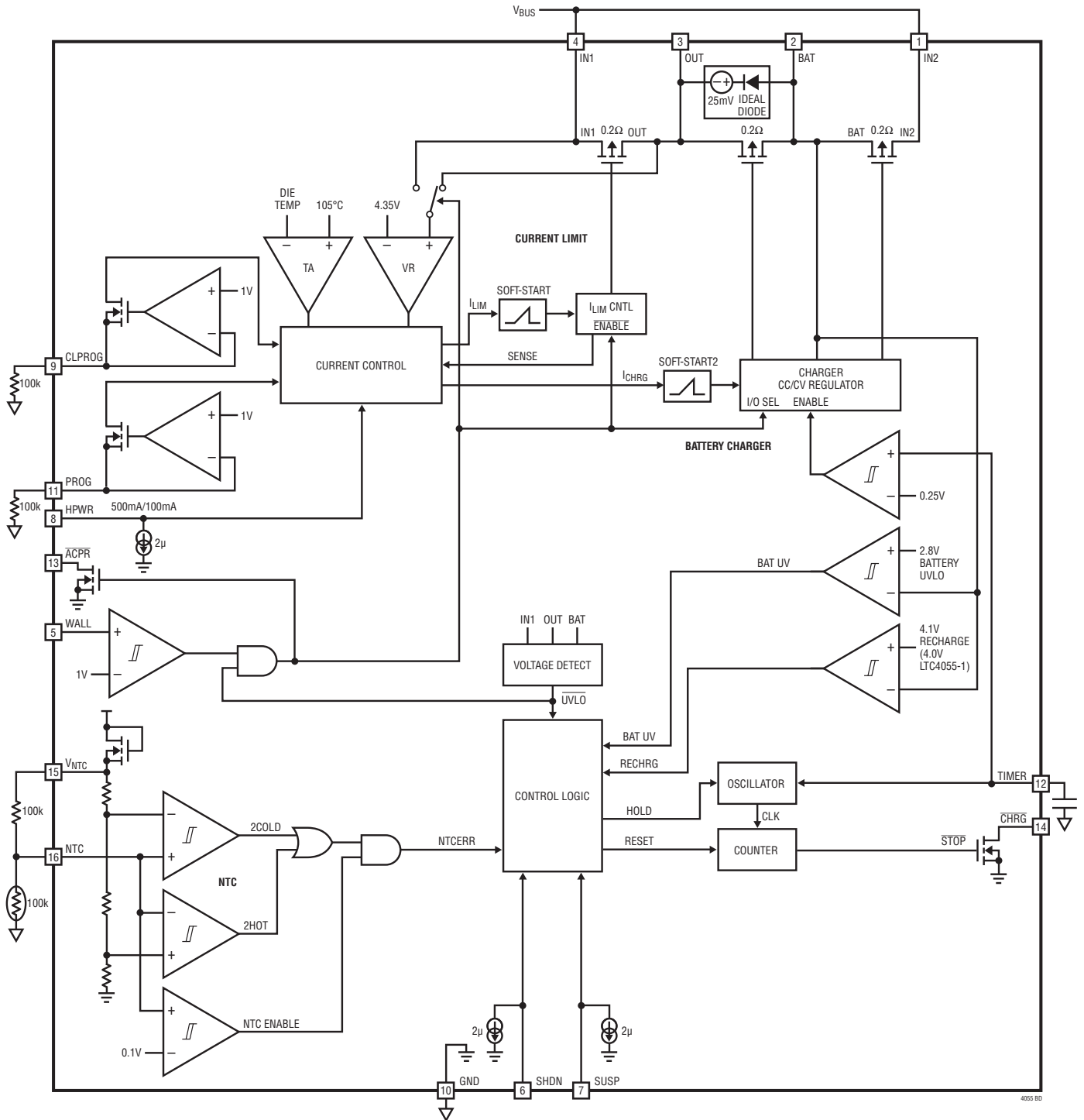
**V<sub>NTC</sub> (Pin 15):** Output Bias Voltage for NTC. A resistor from this pin to the NTC pin will set up the bias for an NTC thermistor.

**NTC (Pin 16):** Input to the NTC Thermistor Monitoring Circuits. Under normal operation, tie a thermistor from the NTC pin to ground and a resistor of equal value from NTC to  $V_{\text{NTC}}$ . When the voltage on this pin is above  $0.74 \cdot V_{\text{NTC}}$  (Cold, 0°C) or below  $0.29 \cdot V_{\text{NTC}}$  (Hot, 50°C) the timer is suspended, but not cleared, the charging is disabled and the CHRG pin remains in its former state. When the voltage on NTC comes back between  $0.74 \cdot V_{\text{NTC}}$  and  $0.29 \cdot V_{\text{NTC}}$ , the timer continues where it left off and charging is re-enabled if the battery voltage is below the recharge threshold. There is approximately 3°C of temperature hysteresis associated with each of the input comparators.

If the NTC function is not to be used, connect the NTC to ground. This will disable all of the LTC4055/LTC4055-1 NTC functions.

**Exposed Pad (Pin 17):** Ground. The Exposed Pad must be soldered to a good thermally conductive PCB ground.

## BLOCK DIAGRAM



4055 BD

## OPERATION

The LTC4055/LTC4055-1 are complete PowerPath controllers for battery-powered USB applications. The LTC4055/LTC4055-1 are designed to provide device power and Li-ion battery charging from the USB  $V_{BUS}$  while maintaining the current limits as specified in the USB specification. This is accomplished by reducing battery charge current as output/load current is increased. In this scenario, the available bus current is maximized in an effort to minimize battery charge time.

An ideal diode function provides power from the battery when output/load current exceeds the input current limit set for the part or when input power is removed. The advantage to powering the load through the ideal diode (rather than connecting the load directly to the battery) is that when the bus is connected and the battery is fully charged, the battery remains fully charged until bus power is removed. Once bus power is removed the output drops until the ideal diode is forward biased. The forward biased ideal diode will then provide the output power to the load from the battery.

Another advantage to powering the load from the bus when the bus is available is in cases where the load is a switching regulator. The input power to a switching regulator can be thought of as constant. A higher voltage across a constant power load will require less current. Less load current in USB applications means more available charge current. More charge current translates to shorter charge times.

The LTC4055/LTC4055-1 also have the ability to accommodate power from a wall adapter. Wall adapter power can be connected to the output (load side) of the LTC4055/LTC4055-1 through an external device such as a power Schottky or FET, as shown in Figure 1. The LTC4055/LTC4055-1 have the unique ability to use the output, which is powered by the wall adapter, as an alternate path to charge the battery while providing power to the load. A wall adapter comparator on the LTC4055/LTC4055-1 can be configured to detect the presence of the wall adapter and shut off the connection to the USB to prevent reverse conduction out to the bus.

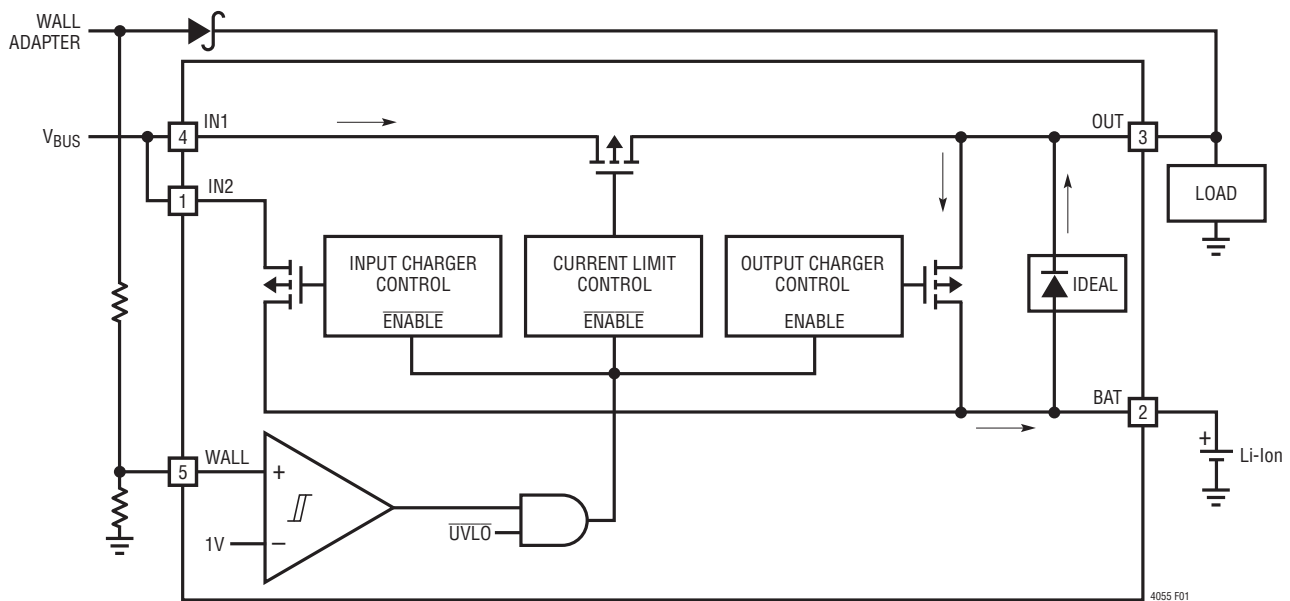


Figure 1. Simplified Block Diagram—PowerPath

## OPERATION

**Table 1. Operating Modes—PowerPath States Current Limited Input Power (IN1/IN2 to OUT)**

WALL PRESENT	SHUTDOWN	SUSPEND	$V_{IN} > 3.8V$	$V_{IN} > (V_{OUT} + 100mV)$	$V_{IN} > (V_{BAT} + 100mV)$	CURRENT LIMIT ENABLED
Y	X	X	X	X	X	N
X	Y	X	X	X	X	N
X	X	Y	X	X	X	N
X	X	X	N	X	X	N
X	X	X	X	N	X	N
X	X	X	X	X	N	N
N	N	N	Y	Y	Y	Y

**Input Powered Charger (IN1/IN2 to BAT)**

WALL PRESENT	SHUTDOWN	SUSPEND	$V_{IN} > 4.35V$	$V_{IN} > (V_{OUT} + 100mV)$	$V_{IN} > (V_{BAT} + 100mV)$	INPUT CHARGER ENABLED
Y	X	X	X	X	X	N
X	Y	X	X	X	X	N
X	X	Y	X	X	X	N
X	X	X	N	X	X	N
X	X	X	X	N	X	N
X	X	X	X	X	N	N
N	N	N	Y	Y	Y	Y

**Output Powered Charger (OUT to BAT)**

WALL PRESENT	SHUTDOWN	SUSPEND	$V_{IN} > 4.35V$	$V_{OUT} > (V_{IN} + 100mV)$	$V_{OUT} > (V_{BAT} + 100mV)$	OUTPUT CHARGER ENABLED
N	X	X	X	X	X	N
X	Y	X	X	X	X	N
X	X	X	N	X	X	N
X	X	X	X	N	X	N
X	X	X	X	X	N	N
Y	N	X	Y	Y	Y	Y

**Ideal Diode (BAT to OUT)**

WALL PRESENT	SHUTDOWN	SUSPEND	$V_{BAT} > 2.8V$	$V_{BAT} > V_{OUT}$	$V_{IN}$	DIODE ENABLED
X	Y	X	X	X	X	N
X	X	X	N	X	X	N
X	X	X	X	N	X	N
X	N	X	Y	Y	X	Y

**Table 2. Operating Modes—Pin Currents vs Programmed Currents (Charging from IN1/IN2)**

PROGRAMMING	OUTPUT CURRENT	BATTERY CURRENT	INPUT CURRENT
$I_{CL} = I_{CHG}$	$I_{OUT} < I_{CL}$ $I_{OUT} = I_{CL} = I_{CHG}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CHG} - I_{OUT}$ $I_{BAT} = 0$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$
$I_{CHG} < I_{CL}$	$I_{OUT} < (I_{CL} - I_{CHG})$ $I_{OUT} > (I_{CL} - I_{CHG})$ $I_{OUT} = I_{CL}$ $I_{OUT} > I_{CL}$	$I_{BAT} = I_{CHG}$ $I_{BAT} = I_{CL} - I_{OUT}$ $I_{BAT} = 0$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CHG} + I_{OUT}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$
$I_{CL} < I_{CHG}$	$I_{OUT} < I_{CL}$ $I_{OUT} > I_{CL}^*$	$I_{BAT} = I_{CL} - I_{OUT}$ $I_{BAT} = I_{CL} - I_{OUT}$	$I_{IN} = I_Q + I_{CL}$ $I_{IN} = I_Q + I_{CL}$

\*Charge current shuts off when  $V_{OUT}$  drops below  $V_{BAT}$ , i.e., when  $I_{OUT}$  exceeds  $I_{CL}$ .

# OPERATION

Operational State Diagram



## OPERATION

### USB CURRENT LIMIT AND CHARGE CURRENT CONTROL

The current limit and charger control circuits of the LTC4055/LTC4055-1 are designed to limit input current as well as control battery charge current as a function of  $I_{OUT}$ . The programmed current limit,  $I_{CL}$  is defined as:

$$I_{CL} = \left( \frac{49,000}{R_{CLPROG}} \cdot V_{CLPROG} \right) = \frac{49,000V}{R_{CLPROG}}$$

The programmed battery charge current,  $I_{CHG}$ , is defined as:

$$I_{CHG} = \left( \frac{48,500}{R_{PROG}} \cdot V_{PROG} \right) = \frac{48,500V}{R_{PROG}}$$

Input current,  $I_{IN}$ , is equal to the sum of the BAT pin output current and the OUT pin output current.

$$I_{IN} = I_{OUT} + I_{BAT}$$

The current limiting circuitry in the LTC4055/LTC4055-1 can and should be configured to limit current to 500mA for USB applications (selectable using the HPWR pin and programmed using the CLPROG pin).

When programmed for 500mA current limit and 500mA or more of charging current, powered from IN1/IN2 and battery charging is active, control circuitry within

the LTC4055/LTC4055-1 reduces the battery charging current such that the sum of the battery charge current and the load current does not exceed 500mA (100mA when HPWR is low, see Figure 2) The battery charging current goes to zero when load current exceeds 500mA (80mA when HPWR is low). If the load current is greater than the current limit, the output voltage will drop to just under the battery voltage where the ideal diode circuit will take over and the excess load current will be drawn from the battery (shaded region in Figure 2).

### PROGRAMMING CURRENT LIMIT

The formula for programming current limit is:

$$I_{CL} = I_{CLPROG} \cdot 49,000 = \frac{V_{CLPROG}}{R_{CLPROG}} \cdot 49,000$$

where  $V_{CLPROG}$  is the CLPROG pin voltage and  $R_{CLPROG}$  is the total resistance from the CLPROG pin to ground.

For example, if typical 490mA current limit is required, calculate:

$$R_{CLPROG} = \frac{1V}{490mA} \cdot 49,000 = 100k$$

In USB applications, the minimum value for  $R_{CLPROG}$  should be 105k. This will prevent the application current from

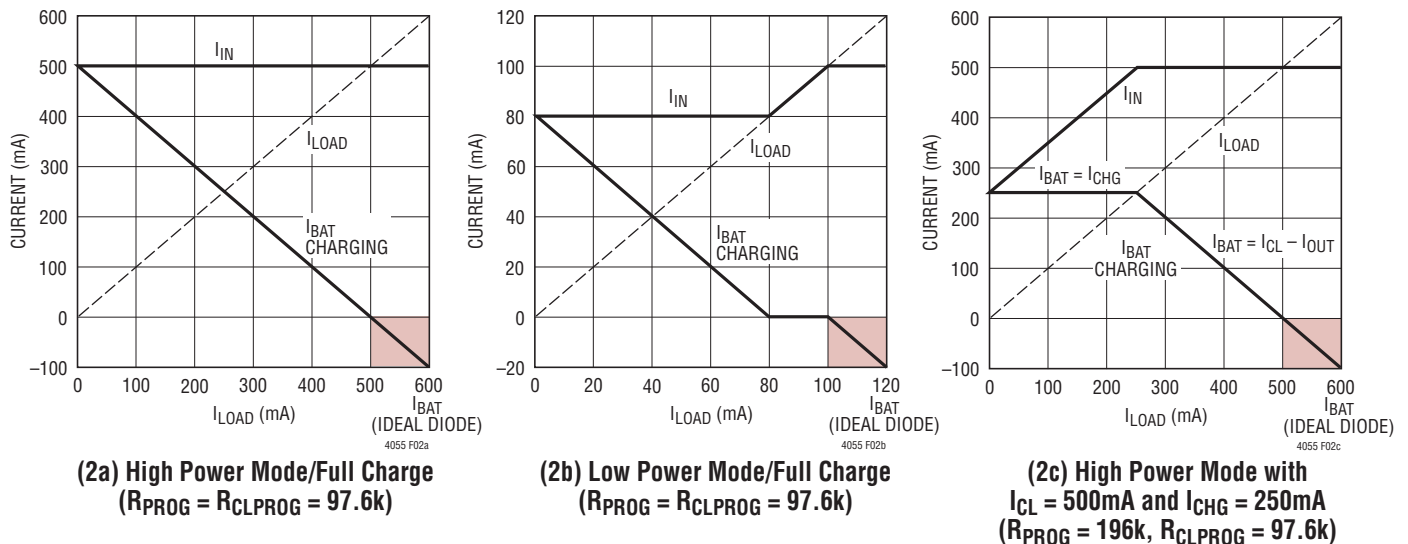


Figure 2. Input and Battery Currents as a Function of Load Current

## OPERATION

exceeding 500mA due to LTC4055/LTC4055-1 tolerances and quiescent currents. This will give a typical current limit of approximately 467mA in high power mode (HPWR = 1) or 92mA in low power mode (HPWR = 0).

For best stability over temperature and time, 1% metal film resistors are recommended.

### Battery Charger

The battery charger circuits of the LTC4055/LTC4055-1 are designed for charging single-cell lithium-ion batteries. Featuring an internal P-channel power MOSFET, the charger uses a constant-current/constant-voltage charge algorithm with programmable current and a programmable timer for charge termination. Charge current can be programmed up to 1A. The final float voltage accuracy is  $\pm 0.8\%$  typical. No blocking diode or sense resistor is required when charging through IN1/IN2. The  $\overline{\text{CHRG}}$  open-drain status output provides information regarding the charging status of the LTC4055/LTC4055-1 at all times. An NTC input provides the option of charge qualification using battery temperature.

An internal thermal limit reduces the programmed charge current if the die temperature attempts to rise above a preset value of approximately 105°C. This feature protects the LTC4055/LTC4055-1 from excessive temperature, and allows the user to push the limits of the power handling capability of a given circuit board without risk of damaging the LTC4055/LTC4055-1. Another benefit of the LTC4055/LTC4055-1 thermal limit is that charge current can be set according to typical, not worst-case, ambient temperatures for a given application with the assurance that the charger will automatically reduce the current in worst-case conditions.

An internal voltage regulation circuit, called undervoltage current limit, UVCL, reduces the programmed charge current to keep the voltage on  $V_{\text{IN}}$  or  $V_{\text{OUT}}$  at least 4.4V. This feature prevents the charger from cycling in and out of undervoltage lockout due to resistive drops in the USB or wall adapter cabling.

The charge cycle begins when the voltage at the input (IN1/IN2) rises above the input UVLO level and the battery voltage is below the recharge threshold. No charge current actually flows until the input voltage is greater than the  $V_{\text{UVCL}}$  level. At the beginning of the charge cycle, if the

battery voltage is below 2.8V, the charger goes into trickle-charge mode to bring the cell voltage up to a safe level for charging. The charger goes into the fast charge constant-current mode once the voltage on the BAT pin rises above 2.8V. In constant current mode, the charge current is set by  $R_{\text{PROG}}$ . When the battery approaches the final float voltage, the charge current begins to decrease as the LTC4055/LTC4055-1 switches to constant-voltage mode.

An external capacitor on the TIMER pin sets the total minimum charge time. When this time elapses the charge cycle terminates and the  $\overline{\text{CHRG}}$  pin assumes a high impedance state. While charging in constant-current mode, if the charge current is decreased due to load current, undervoltage charge current limiting or thermal regulation the charging time is automatically increased. In other words, the charge time is extended inversely proportional to charge current delivered to the battery. For lithium-ion and similar batteries that require accurate final float potential, the internal bandgap reference, voltage amplifier and the resistor divider provide regulation with  $\pm 1\%$  maximum accuracy.

### TRICKLE CHARGE AND DEFECTIVE BATTERY DETECTION

At the beginning of a charge cycle, if the battery voltage is low (below 2.8V) the charger goes into trickle-charge reducing the charge current to 10% of the full-scale current. If the low battery voltage persists for one quarter of the total charge time, the battery is assumed to be defective, the charge cycle is terminated and the  $\overline{\text{CHRG}}$  pin output assumes a high impedance state. If for any reason the battery voltage rises above  $\sim 2.8\text{V}$ , the charge cycle will be restarted. To restart the charge cycle (i.e., when the dead battery is replaced with a discharged battery), simply remove the input voltage and reapply it, cycle the TIMER pin to 0V or cycle the SHDN pin to 0V.

### PROGRAMMING CHARGE CURRENT

The formula for programming the battery charge current, when not being limited, is:

$$I_{\text{CHG}} = I_{\text{PROG}} \cdot 48,500 = \frac{V_{\text{PROG}}}{R_{\text{PROG}}} \cdot 48,500$$



## OPERATION

where  $V_{\text{PROG}}$  is the PROG pin voltage and  $R_{\text{PROG}}$  is the total resistance from the PROG pin to ground.

For example, if typical 485mA charge current is required, calculate:

$$R_{\text{PROG}} = \frac{1\text{V}}{485\text{mA}} \cdot 48,500 = 100\text{k}$$

For best stability over temperature and time, 1% metal film resistors are recommended. Under trickle-charge conditions, this current is reduced to 10% of the full-scale value.

### THE CHARGE TIMER

The programmable charge timer is used to terminate the charge cycle. The timer duration is programmed by an external capacitor at the TIMER pin and is also a function of the resistance on PROG. Typically the charge time is:

$$t_{\text{TIMER}}(\text{Hours}) = \frac{C_{\text{TIMER}} \cdot R_{\text{PROG}} \cdot 3 \text{ Hours}}{0.1\mu\text{F} \cdot 100\text{k}}$$

The timer starts when an input voltage greater than the undervoltage lockout threshold level is applied, or when leaving shutdown and the voltage on the battery is less than the recharge threshold. At power-up or exiting shutdown with the battery voltage less than the recharge threshold, the charge time is a full cycle. If the battery is greater than the recharge threshold, the timer will not start and charging is prevented. If after power-up the battery voltage drops below the recharge threshold, or if after a charge cycle the battery voltage is still below the recharge threshold, the charge time is set to one half of a full cycle.

The LTC4055/LTC4055-1 have a feature that extends charge time automatically. Charge time is extended if the charge current in constant-current mode is reduced due to load current, undervoltage charge current limiting or thermal regulation. This change in charge time is inversely proportional to the change in charge current. As the LTC4055/LTC4055-1 approach constant-voltage mode the charge current begins to drop. This change in charge current is part of the normal charging operation of the part and should not affect the timer duration. Therefore,

the LTC4055/LTC4055-1 detect that the change in charge current is due to voltage mode, and increase the timer period back to its programmed operating period.

Once a time-out occurs and the voltage on the battery is greater than the recharge threshold, the charge current stops, and the  $\overline{\text{CHRG}}$  output assumes a high impedance state to indicate that the charging has stopped.

Connecting the TIMER pin to ground disables the battery charger.

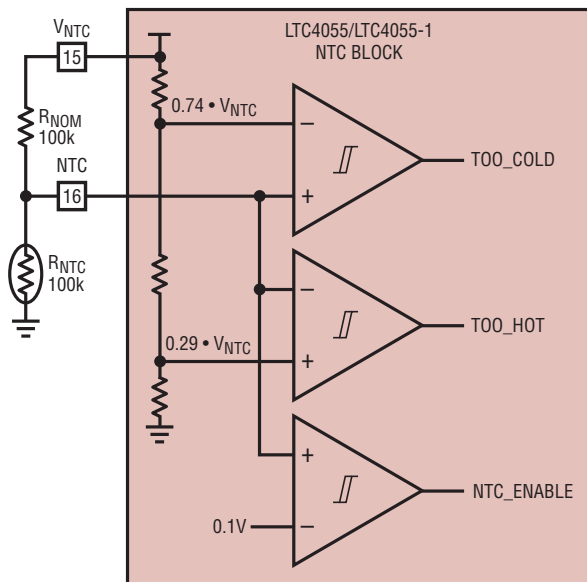
### $\overline{\text{CHRG}}$ STATUS OUTPUT PIN

When the charge cycle starts, the  $\overline{\text{CHRG}}$  pin is pulled to ground by an internal N-channel MOSFET capable of driving an LED. After a time-out occurs, the pin assumes a high impedance state.

### NTC Thermistor

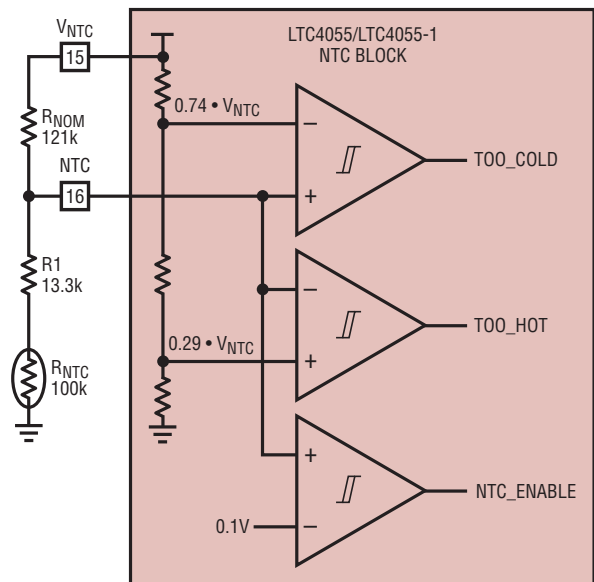
The battery temperature is measured by placing a negative temperature coefficient (NTC) thermistor close to the battery pack. The NTC circuitry is shown in Figure 3. To use this feature, connect the NTC thermistor,  $R_{\text{NTC}}$ , between the NTC pin and ground and a resistor,  $R_{\text{NOM}}$ , from the NTC pin to  $V_{\text{NTC}}$ .  $R_{\text{NOM}}$  should be a 1% resistor with a value equal to the value of the chosen NTC thermistor at 25°C (this value is 10k for a Vishay NTHS0603N02N1002J thermistor). The LTC4055/LTC4055-1 go into hold mode when the resistance,  $R_{\text{HOT}}$ , of the NTC thermistor drops to 0.41 times the value of  $R_{\text{NOM}}$  or approximately 4.1k, which should be at 50°C. The hold mode freezes the timer and stops the charge cycle until the thermistor indicates a return to a valid temperature. As the temperature drops, the resistance of the NTC thermistor rises. The LTC4055/LTC4055-1 are designed to go into hold mode when the value of the NTC thermistor increases to 2.82 times the value of  $R_{\text{NOM}}$ . This resistance is  $R_{\text{COLD}}$ . For a Vishay NTHS0603N02N1002J thermistor, this value is 28.2k which corresponds to approximately 0°C. The hot and cold comparators each have approximately 3°C of hysteresis to prevent oscillation about the trip point. Grounding the NTC pin disables the NTC function.

## OPERATION



(3a)

4055 F03a



(3b)

4055 F03b

Figure 3. NTC Circuits

## THERMISTORS

The LTC4055/LTC4055-1 NTC trip points were designed to work with thermistors whose resistance-temperature characteristics follow Vishay Dale's "R-T Curve 2." The Vishay NTHS0603N02N1002J is an example of such a thermistor. However, Vishay Dale has many thermistor products that follow the "R-T Curve 2" characteristic in a variety of sizes. Furthermore, any thermistor whose ratio of  $R_{COLD}$  to  $R_{HOT}$  is about 7.0 will also work (Vishay Dale R-T Curve 2 shows a ratio of  $R_{COLD}$  to  $R_{HOT}$  of  $2.815/0.4086 = 6.89$ ).

Power conscious designs may want to use thermistors whose room temperature value is greater than 10k. Vishay Dale has a number of values of thermistor from 10k to 100k that follow the "R-T Curve 1." Using these as indicated in the NTC Thermistor section will give temperature trip points of approximately 3°C and 47°C, a delta of 44°C. This delta in temperature can be moved in either direction by changing the value of  $R_{NOM}$  with respect to  $R_{NTC}$ . Increasing  $R_{NOM}$  will move both trip points to lower temperatures. Likewise a decrease in  $R_{NOM}$  with respect to  $R_{NTC}$  will move the trip points to higher temperatures. To calculate

$R_{NOM}$  for a shift to lower temperature for example, use the following equation:

$$R_{NOM} = \frac{R_{COLD}}{2.815} \cdot R_{NTC} \text{ at } 25^{\circ}\text{C}$$

where  $R_{COLD}$  is the resistance ratio of  $R_{NTC}$  at the desired cold temperature trip point. If you want to shift the trip points to higher temperatures use the following equation:

$$R_{NOM} = \frac{R_{HOT}}{0.4086} \cdot R_{NTC} \text{ at } 25^{\circ}\text{C}$$

where  $R_{HOT}$  is the resistance ratio of  $R_{NTC}$  at the desired hot temperature trip point.

Here is an example using a 100k R-T Curve 1 thermistor from Vishay Dale. The difference between the trip points is 44°C, from before, and we want the cold trip point to be 0°C, which would put the hot trip point at 44°C. The  $R_{NOM}$  needed is calculated as follows:

$$\begin{aligned} R_{NOM} &= \frac{R_{COLD}}{2.815} \cdot R_{NTC} \text{ at } 25^{\circ}\text{C} \\ &= \frac{3.266}{2.815} \cdot 100\text{k} = 116\text{k} \end{aligned}$$

## OPERATION

The nearest 1% value for  $R_{NOM}$  is 115k. This is the value used to bias the NTC thermistor to get cold and hot trip points of approximately 0°C and 44°C respectively. To extend the delta between the cold and hot trip points a resistor, R1, can be added in series with  $R_{NTC}$  (see Figure 3b). The values of the resistors are calculated as follows:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086}$$

$$R1 = \left( \frac{0.4086}{2.815 - 0.4086} \right) \cdot (R_{COLD} - R_{HOT}) - R_{HOT}$$

where  $R_{NOM}$  is the value of the bias resistor,  $R_{HOT}$  and  $R_{COLD}$  are the values of  $R_{NTC}$  at the desired temperature trip points. Continuing the example from before with a desired hot trip point of 50°C:

$$R_{NOM} = \frac{R_{COLD} - R_{HOT}}{2.815 - 0.4086} = \frac{100k \cdot (3.266 - 0.3602)}{2.815 - 0.4086}$$

= 120.8k, 121k is nearest 1%

$$R1 = 100k \cdot \left[ \left( \frac{0.4086}{2.815 - 0.4086} \right) \cdot (3.266 - 0.3602) - 0.3602 \right]$$

= 13.3k, 13.3k is nearest 1%

The final solution is as shown if Figure 3b where  $R_{NOM} = 121k$ ,  $R1 = 13.3k$  and  $R_{NTC} = 100k$  at 25°C.

## CURRENT LIMIT UNDERVOLTAGE LOCKOUT

An internal undervoltage lockout circuit monitors the input voltage and keeps the current limit circuits of the part in shutdown mode until  $V_{IN}$  rises above the undervoltage lockout threshold. The current limit UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the current limit UVLO circuit keeps the current limit shutdown if  $V_{OUT}$  exceeds  $V_{IN}$ . If the current limit UVLO comparator is tripped, the current limit circuits will not come out of shutdown until  $V_{OUT}$  falls 50mV below the  $V_{IN}$  voltage.

## CHARGER UNDERVOLTAGE LOCKOUT

Internal undervoltage lockout circuits monitor the  $V_{IN}$  and  $V_{OUT}$  voltages and keep the charger circuits of the part shut down until  $V_{IN}$  or  $V_{OUT}$  rises above the undervoltage lockout threshold. The charger UVLO circuit has a built-in hysteresis of 125mV. Furthermore, to protect against reverse current in the power MOSFET, the charger UVLO circuit keeps the charger shutdown if  $V_{BAT}$  exceeds  $V_{OUT}$ . If the charger UVLO comparator is tripped, the charger circuits will not come out of shutdown until  $V_{OUT}$  exceeds  $V_{BAT}$  by 50mV.

## SHUTDOWN

The LTC4055/LTC4055-1 can be shut down by forcing the SHDN pin greater than 1V. In shutdown, the currents on IN1/IN2, OUT and BAT are decreased to less than 2.5µA and the internal battery charge timer is reset. All power paths are put in a Hi-Z state.

## SUSPEND

The LTC4055/LTC4055-1 can be put in suspend mode by forcing the SUSP pin greater than 1V. In suspend mode the ideal diode function from BAT to OUT and the output charger are kept alive. The rest of the part is shut down to conserve current and the battery charge timer is reset if  $V_{OUT}$  becomes less than  $V_{BAT}$ .

## $V_{IN}$ and Wall Adapter Bypass Capacitor

Many types of capacitors can be used for input bypassing. However, caution must be exercised when using multilayer ceramic capacitors. Because of the self resonant and high Q characteristics of some types of ceramic capacitors, high voltage transients can be generated under some start-up conditions, such as connecting the charger input to a hot power source. For more information, refer to Application Note 88.

## OPERATION

### Selecting WALL Input Resistors

The WALL input pin identifies the presence of a wall adapter. This information is used to disconnect the inputs IN1/IN2 from the OUT pin in order to prevent back conduction to whatever may be connected to the inputs. It also forces the  $\overline{\text{ACPR}}$  pin low when the voltage at the WALL pin exceeds the input threshold. The WALL pin has a 1V rising threshold and approximately 30mV of hysteresis.

It needs to be noted that this function is disabled when the only power applied to the part is from the battery. Therefore the 1V threshold only applies when the voltage on either IN1/IN2 or OUT is 100mV greater than the voltage on BAT and the voltage on IN1/IN2 or OUT is greater than the  $V_{\text{UVLO}}$  (3.8V typ) threshold.

The wall adapter detection threshold is set by the following equation:

$$V_{\text{TH}}(\text{Adapter}) = V_{\text{WALL}} \cdot \left(1 + \frac{R1}{R2}\right)$$

$$V_{\text{HYST}}(\text{Adapter}) = V_{\text{WALL-HYST}} \cdot \left(1 + \frac{R1}{R2}\right)$$

where  $V_{\text{TH}}(\text{Adapter})$  is the wall adapter detection threshold,  $V_{\text{WALL}}$  is the WALL pin rising threshold (typically 1V),  $R1$  is the resistor from the wall adapter input to WALL and  $R2$  is the resistor from WALL to GND.

Consider an example where the  $V_{\text{TH}}(\text{Adapter})$  is to be set somewhere around 4.5V. Resistance on the WALL pin should be kept relatively low (~10k) in order to prevent false tripping of the wall comparator due to leakages associated with the switching element used to connect the adapter to OUT. Pick  $R2$  to be 10k and solve for  $R1$ .

$$R1 = R2 \cdot \left(\frac{V_{\text{TH}}(\text{Adapter})}{V_{\text{WALL}}} - 1\right)$$

$$R1 = 10\text{k} \cdot \left(\frac{4.5}{1} - 1\right) = 10\text{k} \cdot 3.5 = 35\text{k}$$

The nearest 1% resistor is 34.8k. Therefore  $R1 = 34.8\text{k}$  and the rising trip point should be 4.48V.

$$V_{\text{HYST}}(\text{Adapter}) \approx 30\text{mV} \cdot \left(1 + \frac{34.8}{10}\right) \approx 134\text{mV}$$

The hysteresis is going to be approximately 134mV for this example.

### Power Dissipation

The conditions that cause the LTC4055/LTC4055-1 to reduce charge current due to the thermal protection feedback can be approximated by considering the power dissipated in the part. For high charge currents and a wall adapter applied to  $V_{\text{OUT}}$ , the LTC4055/LTC4055-1 power dissipation is approximately:

$$P_D = (V_{\text{OUT}} - V_{\text{BAT}}) \cdot I_{\text{BAT}}$$

where  $P_D$  is the power dissipated,  $V_{\text{OUT}}$  is the supply voltage,  $V_{\text{BAT}}$  is the battery voltage and  $I_{\text{BAT}}$  is the battery charge current. It is not necessary to perform any worst-case power dissipation scenarios because the LTC4055/LTC4055-1 will automatically reduce the charge current to maintain the die temperature at approximately 105°C. However, the approximate ambient temperature at which the thermal feedback begins to protect the IC is:

$$T_A = 105^\circ\text{C} - P_D \cdot \theta_{\text{JA}}$$

$$T_A = 105^\circ\text{C} - (V_{\text{OUT}} - V_{\text{BAT}}) \cdot I_{\text{BAT}} \cdot \theta_{\text{JA}}$$

Example: An LTC4055/LTC4055-1 operating from a wall adapter with 5V at  $V_{\text{OUT}}$  providing 0.8A to a 3V Li-Ion battery. The ambient temperature above, which the LTC4055/LTC4055-1 will begin to reduce the 0.8A charge current, is approximately:

$$T_A = 105^\circ\text{C} - (5\text{V} - 3\text{V}) \cdot 0.8\text{A} \cdot 37^\circ\text{C/W}$$

$$T_A = 105^\circ\text{C} - 1.6\text{W} \cdot 37^\circ\text{C/W} = 105^\circ\text{C} - 59^\circ\text{C} = 46^\circ\text{C}$$

## OPERATION

The LTC4055/LTC4055-1 can be used above 46°C, but the charge current will be reduced below 0.8A. The charge current at a given ambient temperature can be approximated by:

$$I_{\text{BAT}} = \frac{105^{\circ}\text{C} - T_{\text{A}}}{(V_{\text{OUT}} - V_{\text{BAT}}) \cdot \theta_{\text{JA}}}$$

Consider the above example with an ambient temperature of 55°C. The charge current will be reduced to approximately:

$$I_{\text{BAT}} = \frac{105^{\circ}\text{C} - 55^{\circ}\text{C}}{(5\text{V} - 3\text{V}) \cdot 37^{\circ}\text{C}/\text{W}} = \frac{50^{\circ}\text{C}}{74^{\circ}\text{C}/\text{A}} = 0.675\text{A}$$

## Board Layout Considerations

In order to be able to deliver maximum charge current under all conditions, it is critical that the Exposed Pad on the backside of the LTC4055/LTC4055-1 package is soldered to the board. Correctly soldered to a 2500mm<sup>2</sup> double-sided 1oz. copper board, the LTC4055/LTC4055-1 has a thermal resistance of approximately 37°C/W. Failure to make thermal contact between the Exposed Pad on the backside of the package and the copper board will result in thermal resistances far greater than 37°C/W. As an example, a correctly soldered LTC4055/LTC4055-1 can deliver over 1A to a battery from a 5V supply at room

temperature. Without a backside thermal connection, this number could drop to less than 500mA.

## STABILITY

The constant-voltage mode feedback loop is stable without any compensation when a battery is connected. However, a 1µF capacitor with a 1Ω series resistor to GND is recommended at the BAT pin to keep ripple voltage low when the battery is disconnected.

## Ideal Diode from BAT to OUT

Forward regulation for the LTC4055/LTC4055-1 from BAT to OUT has three operational ranges, depending on the magnitude of the load current. For small load currents, the LTC4055/LTC4055-1 will provide a constant-voltage drop; this operating mode is referred to as “constant V<sub>ON</sub>” regulation. As the current exceeds I<sub>FWD</sub>, the voltage drop will increase linearly with the current with a slope of 1/R<sub>DIO,ON</sub>; this operating mode is referred to as “constant R<sub>ON</sub>” regulation. As the current increases further, exceeding I<sub>MAX</sub>, the forward voltage drop will increase rapidly; this operating mode is referred to as “constant I<sub>ON</sub>” regulation. The characteristics for the following parameters: R<sub>FWD</sub>, R<sub>ON</sub>, V<sub>FWD</sub>, and I<sub>FWD</sub> are specified with the aid of Figure 4.

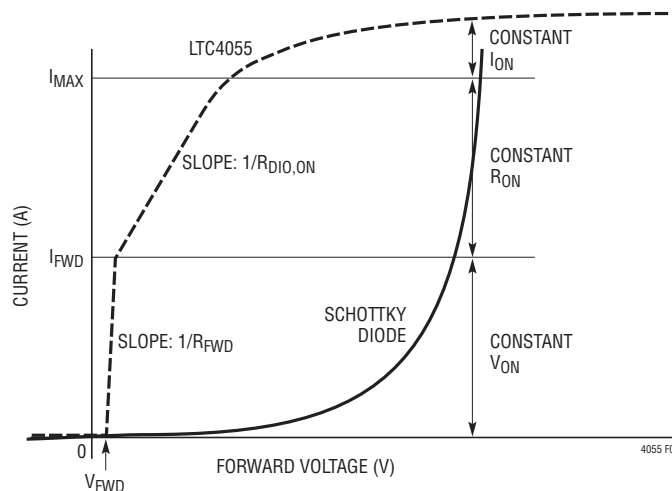


Figure 4. LTC4055/LTC4055-1 vs Schottky Diode Forward Voltage Drop

## TYPICAL APPLICATIONS

### LTC4055/LTC4055-1 Configured for USB Application with Wall Adapter

Figure 5 shows an LTC4055/LTC4055-1 configured for USB applications with the optional wall adapter input. The programming resistor ( $R_{CLPROG}$ ) is set to 105k which sets up a nominal current limit of 467mA in high power mode (92mA in low power). This is done to prevent the various tolerances in the part and programming resistors from

allowing the input current supplied by  $V_{BUS}$  to exceed the 500mA/100mA limits.

The programming resistor ( $R_{PROG}$ ) with a value of 60.4k sets up a nominal charge current of approximately 800mA. Note that this is the charge current when the wall adapter is present. When the wall adapter is absent, the current limit supersedes the charge current programming and charge current is limited to 467mA.

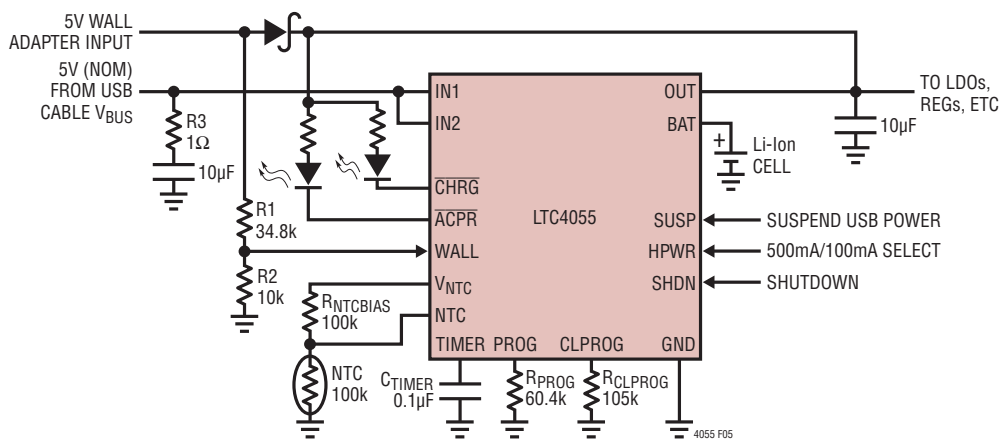


Figure 5. USB Power Control Application with Wall Adapter Input



## TYPICAL APPLICATIONS

### USB Hosting Application: The LTC4055/LTC4055-1's IN1 and IN2 are Set Hi-Z by Pulling the SUSP Pin Above 1.2V

In applications where the power is required to go back out on to the USB  $V_{BUS}$  the LTC4055/LTC4055-1 can be configured to turn off its input power path, IN1 and IN2.

Forcing the SUSP input pin above 1.2V does this. Figure 6 shows the application circuit. The wall adapter or the battery can still provide power to OUT, which in turn can provide power to  $V_{BUS}$  when commanded from the USB controller. The ability to charge the battery is enabled when the wall adapter is present.

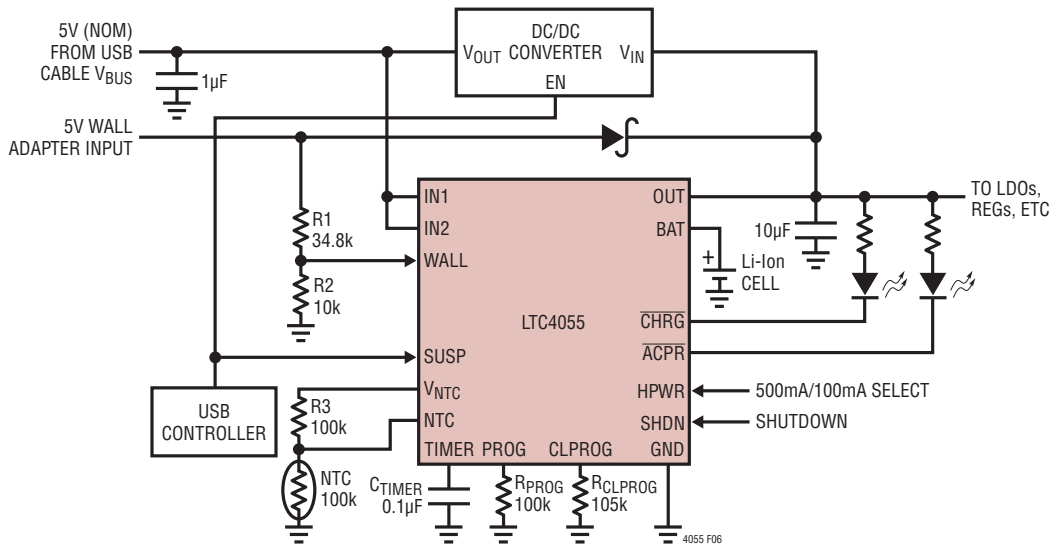


Figure 6. USB Hosting Application





