Datasheet, V2.0, 11 April 2000

CoolSET™-F1

TDA 16822

Off-Line Current Mode Controller with CoolMOS™ on board

Power Conversion

Never stop thinking.

TDA 16822

Revision History:	2000-04-11	Datasheet

Previous Version:

Page	Subjects (major changes since last revision)

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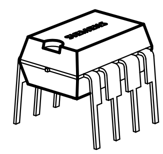
TDA 16822
CoolSET™

Off-Line SMPS Current Mode Controller with CoolMOS™ on board

Features

- PWM controller + CoolMOS™ within one compact package
- 650V (1) avalanche rugged CoolMOS™
- Typical R_{DSon}= 3 Ohm
- Standard DIP-8 package up to 20W
- Only few external components required
- Low start up current
- Improved current mode control for low load conditions
- Input Undervoltage Lockout
- Max duty cycle 72%
- **latched thermal shut down when T_j=140°C of PWM controller**
- **Overload and open loop protection by hiccup mode**
- **Overvoltage protection during hiccup mode**
- **Overall tolerance of current limiting < ±5%**
- **adjustable peak current limitation via external resistor**
- **current overshoot minimization dependent on dI/dt**

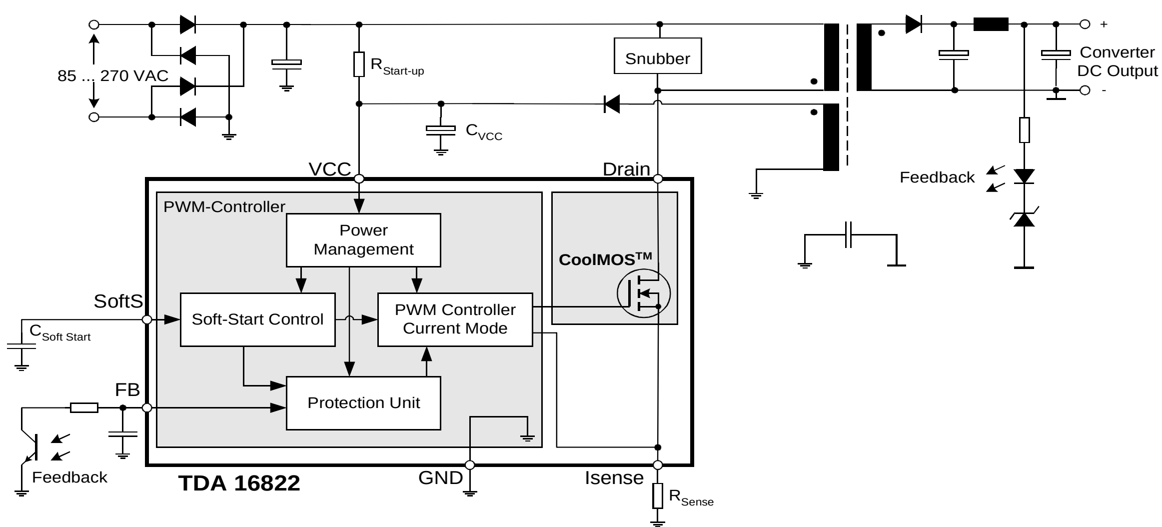


P-DIP-8-6

Description

The TDA 16822 is a current mode pulse width modulator with built in CoolMOS™ transistor. It fulfils the requirement of minimum external control circuitry for a flyback application.
Current mode control means that the current through the CoolMOS™ transistor is compared with a reference signal derived from the output voltage of the flyback application. The result of that comparision determines the on-time of the CoolMOS™ transistor. The accuracy of the switching frequency is highly sophisticated due to temperature compensation. Furthermore overload and open loop protection is implemented by sensing the feedback line. This means in case of overload or open loop the IC is working in protection mode.

Typical Application



Type	Ordering Code	Package
TDA 16822	Q67000-A9449	P-DIP-8-6

1 Pin Configuration and Outline Dimension

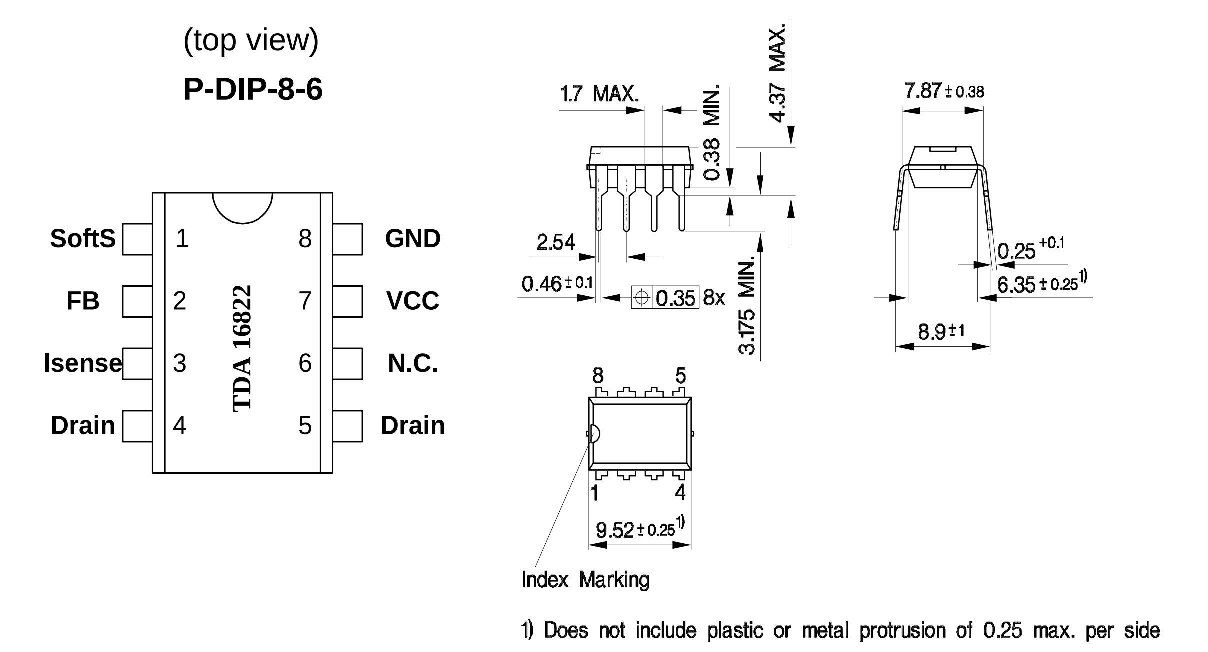


Figure 1

Pin	Symbol	Function
1	SoftS	Soft-Start
2	FB	Feedback
3	Isense	Controller Current Sense Input, CoolMOS™ Source Output
4	Drain	650V (1) CoolMOS™ Drain
5	Drain	650V (1) CoolMOS™ Drain
6	N.C.	Not connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

(1): at Tj = 110°C

2 Electrical Characteristics

2.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} supply voltage	V_{CC}	-0.3	17	V	
Drain Source Voltage	V_{DS}	-	650	V	T_j=110°C
Continous Drain Current	I_D	-	1.5	A	
Avalanche energy, repetitive tAR limited by T_{jmax}[1]	I_{AR}	-	2.5	A	
Avalanche current, repetitive t_{AR} limited by T_{jmax}	E_{AR}	-	0.1	mJ	I_{AR}=2.5A V_{DD}=50V
FB Voltage	V_{FB}	-0.3	6.5	V	
SoftS Voltage	V_{SoftS}	-0.3	6.5	V	
ISense	I_{Sense}	-0.3	3	V	
Junction temperature	T_j	-40	150	°C	
Storage temperature	T_S	-50	150	°C	
Thermal resistance	R_{thJA}	-	90	K/W	P-DIP-8-6

[1] Repetitive avalanche causes additional power losses that can be calculated as $P_{AV} = E_{AR}$*f

2.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
V_{CC} supply voltage	V_{CC}	V_{CCon}	17	V	
Junction temperature	T_J	-25	130	°C	Controller
Ambient temperature	T_A	-25	100	°C	

2.3 Characteristics

Supply Section

Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and ambient temperature range T_A from – 25 °C to 100 °C.Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 15 V is assumed.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start up current	I_{VCC1}	-	85	125	uA	V_{CC} < 8.5V
Supply current with inactiv CoolMOS™	I_{VCC2}	-	5	7	mA	V_{SoftS} = 0
Supply current with activ CoolMOS™	I_{VCC3}	-	6.5	8	mA	I_{FB} = 0
VCC Turn-On Threshold VCC Turn-Off Threshold VCC Turn-On/Off Hysteresis	V_{CCon} V_{CCoff} V_{CCHY}	13.5 8.5 4	14 9 5	14.5 9.5 6	V V V	

Internal Voltage Reference

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed reference voltage	V_{REF}	6.35	6.55	6.75	V	Measured at pin FB
Temperature coefficient V_{REF}	ΔV_{REF}	-	0.2	-	mV/°C	

Feedback & Soft-Start

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
V_{FB} operating range min level	V_{FB1}	-	0.8	-	V	
Feedback resistance	R_{FB}	3.0	3.7	4.9	kOhm	
Temperature coefficient R_{FB}	TK R_{FB}	-	600	-	ppm/°C	
Soft-Start resistance	$R_{Soft\text{-}Start}$	42	50	62	kOhm	
Temperature coefficient $R_{Soft\text{-}Start}$	TK $R_{Soft\text{-}Start}$	-	600	-	ppm/°C	

Oscillator

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Frequency	f_{switch}	93	100	107	kHz	
Temperature Coefficient	TK f_{switch}	-	1000	-	ppm/°C	

Protection Unit

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Over load & open loop detection limit	V_{FB2}	4.5	4.8	5.1	V	$V_{Soft\text{-}Start}$ > 5.3V
Activation limit of overload & open loop detection	$V_{Soft\text{-}Start1}$	5.0	5.3	5.6	V	V_{FB} > 4.8V
Deactivation limit of overvoltage detection	$V_{Soft\text{-}Start2}$	3.8	4	4.2	V	V_{FB} < 4.8V V_{CC} > 16V
Overvoltage detection limit	V_{VCC}	15.3	16	16.7	V	$V_{Soft\text{-}Start}$ < 4V V_{FB} > 4.8V
Thermal Shutdown	T_{jSD}	130	140	150	°C	guaranted by design

Current Limiting (Current Sense CS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CS threshold (incl. propagation delay time) (see Figure 4)	V_{csth}	0.97	1.02	1.07	V	R_{Sense}=2Ohm dI/dt<0.5A/us

CoolMOS™ Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Drain source breakdown voltage	$V_{(BR)DSS}$	600 650	- -	- -	V V	T_j=25°C T_j=110°C
Drain source avalanche breakdown voltage	$V_{(BR)DS}$	-	700	-	V	T_j=25°C
Drain source on-resistance	R_{DSon}	- -	3 -	3.8 7	Ohm Ohm	T_j=25°C T_j=120°C
Zero gate voltage drain current	I_{DSS}	-	0.1	-	uA	U_{GS}=0V
Output Capacitance	C_{OSS}	-	10	-	pF	U_{DS}0=V to 480V
Rise time	t_{rise}	-	40	-	ns	
Fall time	t_{fall}	-	20	-	ns	

PWM Section

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Max duty cycle	D_{max}	0.67	0.72	0.77		
Min duty cycle	D_{min}	0	-	-		V_{FB} = 0V
OP gain	A_v	3.45	3.65	3.95		
OP gain bandwidth	B_w	-	4	-	MHz	
OP phase margin	Φ_w	-	90	-	°	

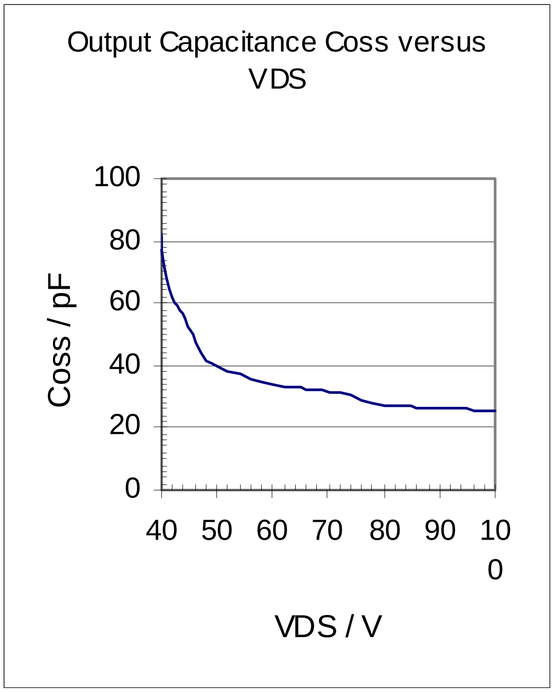


Figure 2

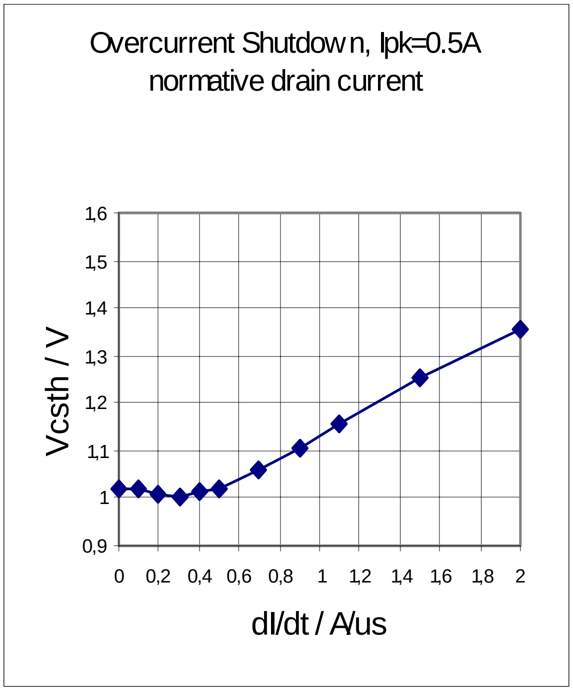


Figure 4

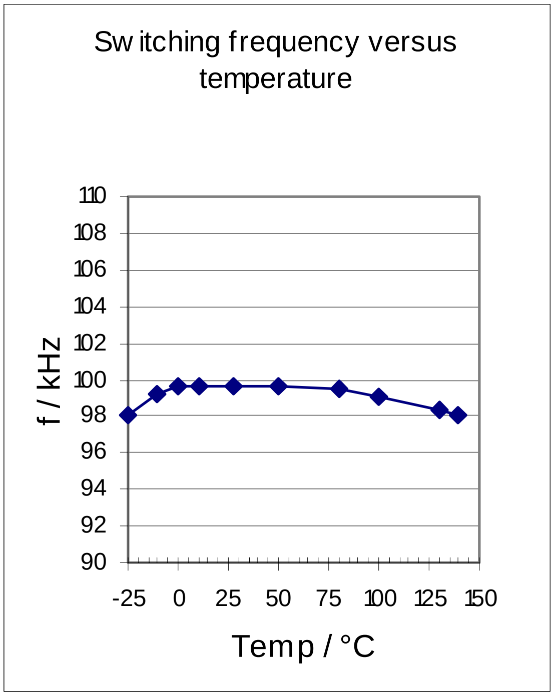


Figure 3

3 Representative Blockdiagramm

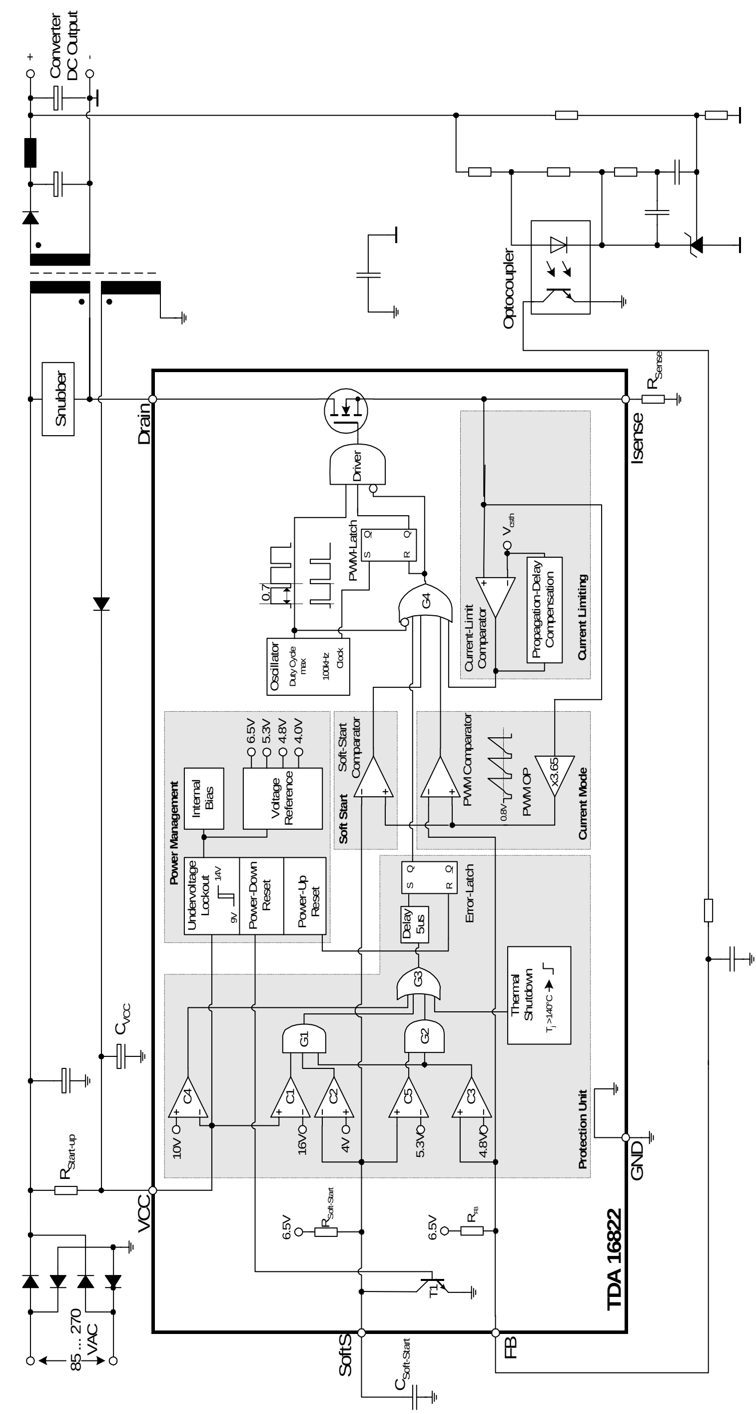


Figure 5

4 Operation Description

Power Management

The undervoltage lockout monitors the external supply voltage V_{CC}. When V_{CC} exceeds the on-threshold V_{CCon}=14V, the internal bias circuit and the voltage reference are switched on. Additionally the error-latch in the protection unit is reset. The internal bandgap generates a reference voltage V_{REF}=6.55V to supply the internal circuits. When V_{CC} falls below the off-threshold V_{CCoff}=9V the circuit is switched off. Then the power down reset discharges the soft-start capacitor $C_{Soft\text{-}Start}$ at pin SoftS by switching on T_1. During start up the current consumption is only about 100uA.

Improved Current Mode

- PWM-OP

The input of the PWM-OP is applied to the external sense resistor R_{Sense} connected to pin ISense. R_{Sense} allows an individual adjustment of maximum CoolMOS™ source current with very low tolerance of maximum current threshold. R_{Sense} converts the source current of the CoolMOS™ into a sense voltage. The sense voltage is amplified with a gain of 3.65. Then the amplified signal is superimposed on a virtual ramp of 0.8V. Under low load conditions the source current of the CoolMOS™ is insufficient to built a voltage ramp for the PWM-Comparator. To guaranted a proper operation at low load the virtual ramp is the reference signal for the PWM-Comparator. The output of the PWM-OP is connected to the positive inputs of the PWM-Comparator and the Soft-Start-Comparator.

- PWM-Comparator

The PWM-Comparator compares the sensed current signal of the CoolMOS™ with the feedback signal V_{FB} . V_{FB} is created by an external optocoupler or external transistor in combination with the internal pullup resistor R_{FB} and provides the information of the feedback circuitry. When the amplified current signal of the CoolMOS™ exceeds the signal V_{FB} the PWM-Comparator switches off the CoolMOS™.

Soft-Start

The Soft-Start is realized by the internal Soft-Start-Comparator and pullup resistor $R_{Soft\text{-}Start}$. The Soft-Start-Comparator compares the voltage at pin SoftS at the negative input with the ramp-signal of the PWM-OP at the positive input. When the Soft-Start voltage $V_{Soft\text{-}Start}$ is less than the Feedback voltage V_{FB} the Soft-Start-Comparator limits the pulse width by reseting the driver. The Soft-Start also controls the starting phase of the hiccup mode by the Comparators C2 and C5 in case of overload or open loop. The Soft-Start voltage is generated by an external capacitor $C_{Soft\text{-}Start}$ at pin SoftS and the internal pullup resistor $R_{Soft\text{-}Start}$ by charging the external capacitor $C_{Soft\text{-}Start}$.

Current Limiting

There is a cycle by cycle current limiting realised with the Current-Limiting Comparator. The CoolMOS™ source current is sensed via an external sense resistor R_{Sense}. When the voltage V_{Sense} at R_{Sense} exceeds the internal threshold voltage V_{csth} the Current-Limit-Comparator immediately turns off the gate drive.

- Propagation Delay Compensation

Concerning circuit delay there is an overshoot of the peak current I_{pk} which depends on the ratio of dI/dt of the peak current. A propagation delay compensation is integrated to bound the tolerance of the current limiting at +/-5% plus the tolerances of R_{Sense}.

This means the propagation delay time between exceeding the current sense threshold V_{csth} and CoolMOS™ switch off is compensated within a range of

$$0 \le \frac{dI}{dt} \le 0.5\,A/\mu s$$

E.g. I_{pk}=0.5A at f_{switch}=100kHz. Without propagation delay compensation the current sense threshold is set to V_{csth}=1V. A current ramp of dI/dt=0.4A/us and a propagation delay time of $t_{csth\text{-}delay}$=180ns leads to an I_{pk} overshoot of 12%. With the propagation delay compensation the overshoot is only about 2%. A current ramp of dI/dt=0.1A/us leads to an overshoot of 3% in both cases, with and without compensation. For further information see Figure 4 on page 8.

Oscillator

The oscillator generates a frequency f_{switch} = 100kHz. A resistor, a capacitor and a current source which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very high accuracy switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum PWM duty cycle D_{max}=0.72.

PWM-Latch

The oscillator clock output applies a set pulse to the PWM-Latch when initiating the CoolMOS™ conduction. After setting the PWM-Latch can be reset by the PWM-OP, the Soft-Start-Comparator, the Current-Limit-Comparator or the Error-Latch of the Protection Unit. In case of reseting the driver is shut down directly.

Driver

The driver-stage drives the gate of the CoolMOS™ and is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when reaching the CoolMOS™ threshold. Thus the leading switch on spike is minimized. When CoolMOS™ is switched off, the falling shape of the driver is slowed down when reaching 2V to prevent an overshoot below ground. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

Protection Unit (Hiccup Mode)

An overload and open loop protection is integrated within the Protection Unit. These two failure modes are latched by an Error-Latch. Additional thermal shutdown and undervoltage protection of V_{CC} is latched by the Error-Latch. In case of these failure modes the Error-Latch is set after a delay of 5us and CoolMOS™ is shut down. This delay prevents the Error-Latch from spikes during normal operation mode.

-Overload & Open loop with normal load

The detection of open loop or overload is provided by the Comparator C3, C5 and the AND-gate G2. The detection is activated by C5 when the voltage at pin SoftS exceeds 5.3V. Henceforth the comparator C3 can set the Error-Latch in case of open loop or overload which leads the feedback voltage V_{FB} to exceed the threshold of 4.8V. After latching VCC decreases till 9V. At this time the external Soft-Start capacitor is discharged by the internal transistor T1 due to Power Down Reset.

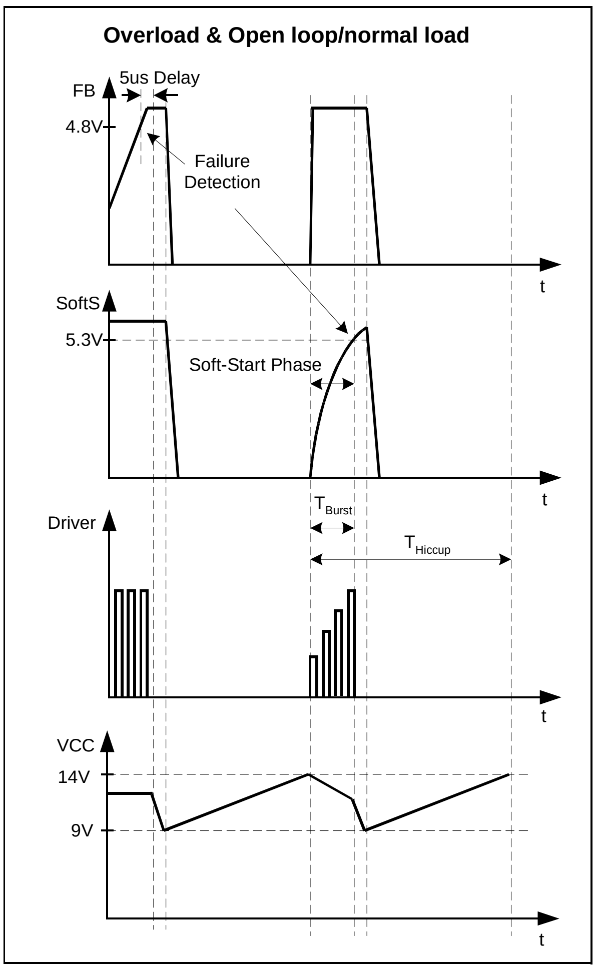


Figure 6

When the IC is inactive VCC increases till 14V. Now the Error-Latch is reset by Power Up Reset and the external Soft-Start capacitor $C_{Soft\text{-}Start}$ is charged by the internal pullup resistor $R_{Soft\text{-}Start}$. During the Soft-Start phase which ends when the voltage at pin SoftS exceeds 6V the detection of overload and open loop by C3 and G2 is inactive. In this way the start up phase is not detected as an overload. But after the Soft-Start phase the start up phase must be finished to force the voltage at FB under the failure detection threshold of 4.8V. Figure 6 shows the hiccup mode in case of overload or open loop with normal load.

-Open loop with no load

An additional protection by the comparators C1, C2 and the AND-gate G1 is implemented. In case of open loop and no load condition the burst phase during hiccup mode is finished early. In this situation the converter output voltage increases and also V_{CC}.

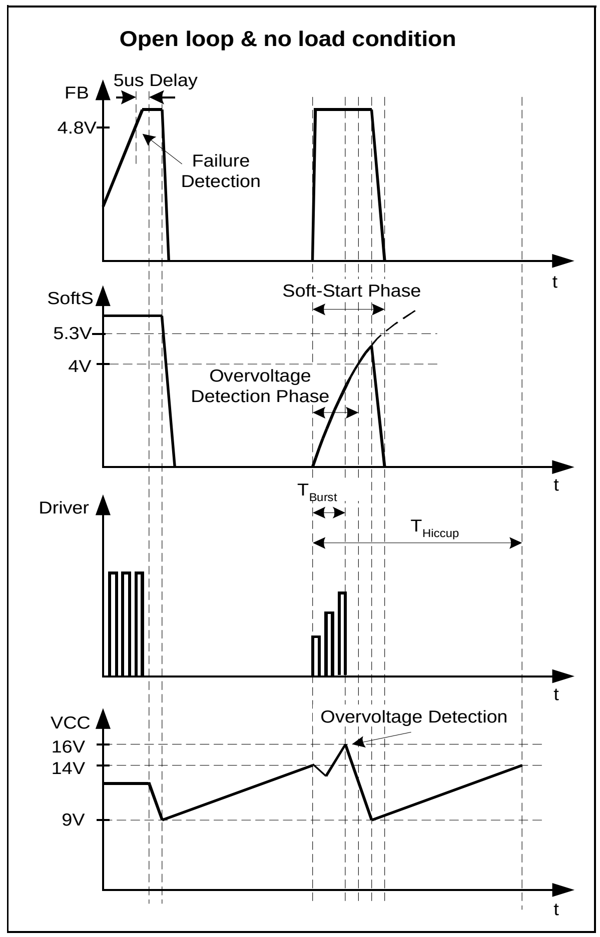


Figure 7

An overvoltage protection is provided by Comparator C1 in the first time till the Soft-Start voltage exceeds the threshold of the Comparator C2 at 4V and the voltage at FB is above 4.8V. This combination is to prevent the normal operation mode from overvoltage protection due to varying of VCC concerning the regulation of the converter output. Figure 7 shows the hiccup mode for open loop and no load condition.

-**Undervoltage Protection**

There is an undervoltage protection of V_{CC} realised by the Comparator C4. In case V_{CC} falls below 10V the Comparator C4 immediately turns off the gate drive by means of the Error-Latch. This is to provide only defined switching of the CoolMOS™.

-**Thermal shutdown**

Thermal shutdown is latched by the Error-Latch when junction temperature of the pwm controller is exceeding an internal threshold of 140°C.

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