Features

- **EE Programmable 524,288 x 1- and 1,048,576 x 1-bit Serial Memories Designed to Store Configuration Programs for Field Programmable Gate Arrays (FPGAs)**
- **In-System Programmable via 2-wire Bus**
- **Simple Interface to SRAM FPGAs**
- **Compatible with Atmel AT6000, AT40K and AT94K Devices, Altera FLEX®, APEX™ Devices, Lucent ORCA® FPGAs, Xilinx XC3000™, XC4000™, XC5200™, Spartan®, Virtex™ FPGAs**
- **Cascadable Read Back to Support Additional Configurations or Higher-density Arrays**
- **Low-power CMOS EEPROM Process**
- **Programmable Reset Polarity**
- **Available in 6 mm x 6 mm x 1 mm 8-lead LAP (Pin-compatible with 8-lead SOIC/VOIC Packages), 8-lead PDIP and 20-lead PLCC Packages (Pin Compatible Across Product Family)**
- **Emulation of Atmel's AT24CXXX Serial EEPROMs**
- **Available in 3.3V ± 10% LV and 5V ± 5% C Versions**
- **System-friendly READY Pin**
- **Low-power Standby Mode**

Description

The AT17C512/010 and AT17LV512/010 (high-density AT17 Series) FPGA Configuration EEPROMs (Configurators) provide an easy-to-use, cost-effective configuration memory for programming Field Programmable Gate Arrays. The AT17 Series is packaged in the 8-lead LAP, 8-lead PDIP and the popular 20-lead PLCC. The AT17 Series uses a simple serial-access procedure to configure one or more FPGA devices. The user can select the polarity of the reset function by programming four EEPROM bytes. These devices support a write protection mode and a system-friendly READY pin, which signifies a "good" power level to the FPGA and can be used to ensure reliable system power-up.

The AT17 Series Configurators can be programmed with industry-standard programmers, Atmel's ATDH2200E Programming Kit or Atmel's ATDH2225 ISP Cable.

FPGA Configuration EEPROM Memory

512-kilobit and

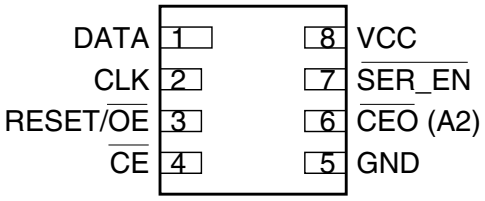
1-megabit

AT17C512
AT17LV512
AT17C010
AT17LV010

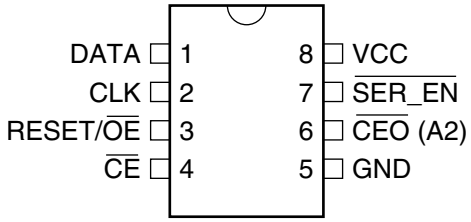
Rev. 0944E–12/01

Pin Configurations

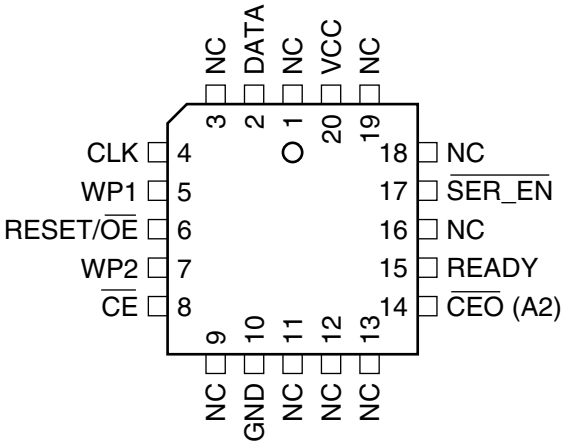
8-lead LAP



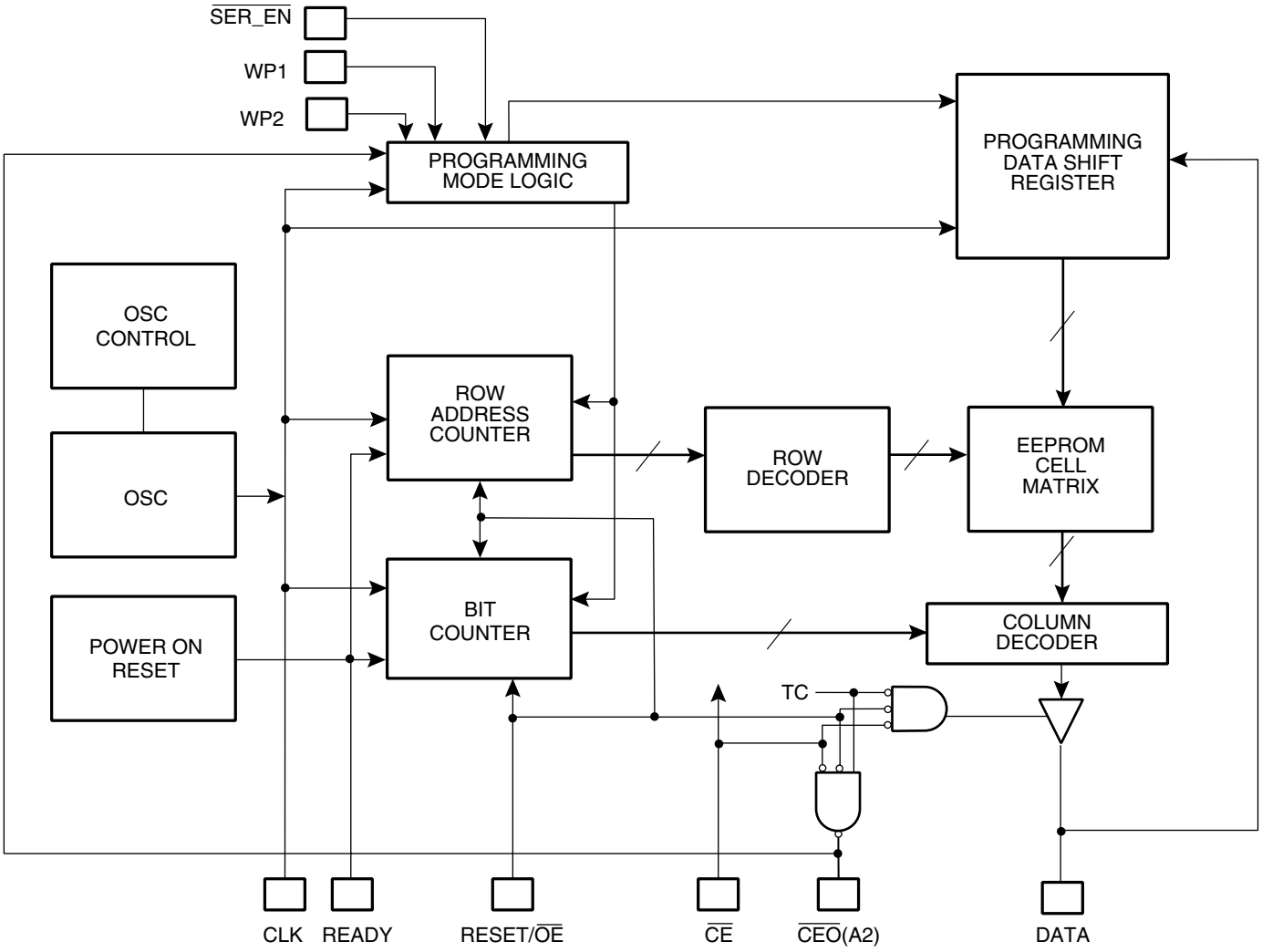
8-lead PDIP



20-lead PLCC



Block Diagram



Device Description

The control signals for the configuration EEPROM ($\overline{CE}$, RESET/$\overline{OE}$ and CCLK) interface directly with the FPGA device control signals. All FPGA devices can control the entire configuration process and retrieve data from the configuration EEPROM without requiring an external intelligent controller.

The configuration EEPROM RESET/$\overline{OE}$ and $\overline{CE}$ pins control the tri-state buffer on the DATA output pin and enable the address counter. When RESET/$\overline{OE}$ is driven High, the configuration EEPROM resets its address counter and tri-states its DATA pin. The $\overline{CE}$ pin also controls the output of the AT17 Series Configurator. If $\overline{CE}$ is held High after the RESET/$\overline{OE}$ reset pulse, the counter is disabled and the DATA output pin is tri-stated. When $\overline{OE}$ is subsequently driven Low, the counter and the DATA output pin are enabled. When RESET/$\overline{OE}$ is driven High again, the address counter is reset and the DATA output pin is tri-stated, regardless of the state of $\overline{CE}$.

When the configurator has driven out all of its data and $\overline{CEO}$ is driven Low, the device tri-states the DATA pin to avoid contention with other configurators. Upon power-up, the address counter is automatically reset.

This is the default setting for the device. Since almost all FPGAs use RESET Low and OE High, this document will describe $\overline{RESET}$/OE.

Pin Description

8 PDIP/ LAP Pin	20 PLCC Pin	Name	I/O	Description
1	2	DATA	I/O	Three-state DATA output for configuration. Open-collector bi-directional pin for programming.
2	4	CLK	I	Clock input. Used to increment the internal address and bit counter for reading and programming.
	5	WP1[1]	I	WRITE PROTECT (1). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations.
3	6	$\overline{\text{RESET}}$/OE	I	Output Enable (active High) and RESET (active Low) when $\overline{\text{SER\_EN}}$ is High. A Low level on $\overline{\text{RESET}}$/OE resets both the address and bit counters. A High level (with $\overline{\text{CE}}$ Low) enables the data output driver. The logic polarity of this input is programmable as either RESET/$\overline{\text{OE}}$ or $\overline{\text{RESET}}$/OE. For most applications, RESET should be programmed active Low. This document describes the pin as $\overline{\text{RESET}}$/OE.
	7	WP2[1]	I	WRITE PROTECT (2). Used to protect portions of memory during programming. Disabled by default due to internal pull-down resistor. This input pin is not used during FPGA loading operations.
4	8	$\overline{\text{CE}}$	I	Chip Enable input (active Low). A Low level (with OE High) allows DCLK to increment the address counter and enables the data output driver. A High level on $\overline{\text{CE}}$ disables both the address and bit counters and forces the device into a low-power standby mode. Note that this pin will *not* enable/disable the device in the 2-wire Serial Programming mode ($\overline{\text{SER\_EN}}$ Low).
5	10	GND		Ground pin. A 0.2 µF decoupling capacitor between V_{CC} and GND is recommended.
6	14	$\overline{\text{CEO}}$	O	Chip Enable Output (active Low). This output goes Low when the address counter has reached its maximum value. In a daisy chain of AT17 Series devices, the $\overline{\text{CEO}}$ pin of one device must be connected to the $\overline{\text{CE}}$ input of the next device in the chain. It will stay Low as long as $\overline{\text{CE}}$ is low and OE is High. It will then follow CE until OE goes Low; thereafter, $\overline{\text{CEO}}$ will stay High until the entire EEPROM is read again.
		A2	I	Device selection input, A2. This is used to enable (or select) the device during programming (i.e., when $\overline{\text{SER\_EN}}$ is Low). A2 has an internal pulldown resistor.
	15	READY[1]	O	Open collector reset state indicator. Driven Low during power-up reset, released (tri-stated) when power-up is complete. (Recommend a 4.7 kΩ pull-up on this pin if used).
7	17	$\overline{\text{SER\_EN}}$	I	Serial enable must be held High during FPGA loading operations. Bringing $\overline{\text{SER\_EN}}$ Low enables the 2-wire Serial Programming Mode. For non-ISP applications, $\overline{\text{SER\_EN}}$ should be tied to V_{CC}.
8	20	V_{CC}		+3.3V/+5V power supply pin.

Note: 1. This pin is not available on the 8-lead packages.

FPGA Master Serial Mode Summary

The I/O and logic functions of any SRAM-based FPGA are established by a configuration program. The program is loaded either automatically upon power-up, or on command, depending on the state of the FPGA mode pins. In Master Mode, the FPGA automatically loads the configuration program from an external memory. The AT17 Serial Configuration EEPROM has been designed for compatibility with the Master Serial Mode.

This document discusses the AT40K, AT40KAL and AT94KAL applications, as well as Xilinx applications.

Control of Configuration

Most connections between the FPGA device and the AT17 Serial EEPROM are simple and self-explanatory:

- The DATA output of the AT17 Series Configurator drives DIN of the FPGA devices.
- The master FPGA CCLK output drives the CLK input of the AT17 Series Configurator.
- The $\overline{CEO}$ output of any AT17 Series Configurator drives the $\overline{CE}$ input of the next Configurator in a cascade chain of EEPROMs.
- $\overline{SER\_EN}$ must be connected to V_{CC} (except during ISP).
- The READY pin is available as an open-collector indicator of the device's reset status; it is driven Low while the device is in its power-on reset cycle and released (tri-stated) when the cycle is complete.

Cascading Serial Configuration EEPROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded Configurators provide additional memory.

As the last bit from the first Configurator is read, the clock signal to the Configurator asserts its $\overline{CEO}$ output Low and disables its DATA line driver. The second Configurator recognizes the Low level on its $\overline{CE}$ input and enables its DATA output.

After configuration is complete, the address counters of all cascaded Configurators are reset if the $\overline{RESET}$/OE on each Configurator is driven to its active (Low) level.

If the address counters are not to be reset upon completion, then the $\overline{RESET}$/OE input can be tied to its inactive (High) level.

AT17 Series Reset Polarity

The AT17 Series Configurator allows the user to program the reset polarity as either RESET/$\overline{OE}$ or $\overline{RESET}$/OE. This feature is supported by industry-standard programmer algorithms.

Programming Mode

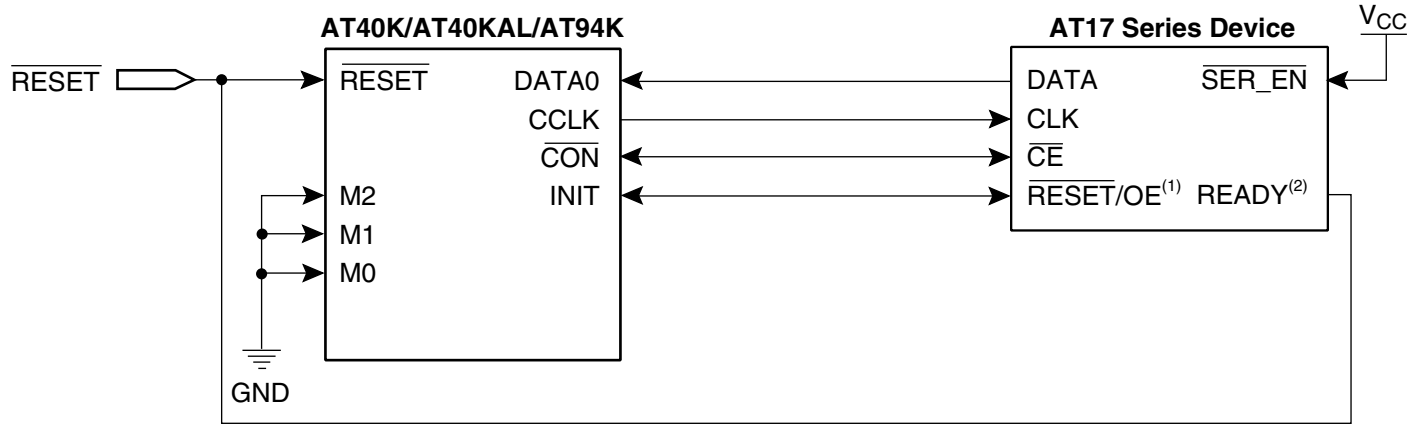
The programming mode is entered by bringing $\overline{SER\_EN}$ Low. In this mode the chip can be programmed by the 2-wire serial bus. The programming is done at V_{CC} supply only. Programming super voltages are generated inside the chip. The AT17C parts are read/write at 5V nominal. The AT17LV parts are read/write at 3.3V nominal.

Standby Mode

The AT17C/LV512/010 Series Configurator enters a low-power standby mode whenever $\overline{CE}$ is asserted High. In this mode, the Configurator consumes less than 0.5 mA of current at 5V. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Example Circuits

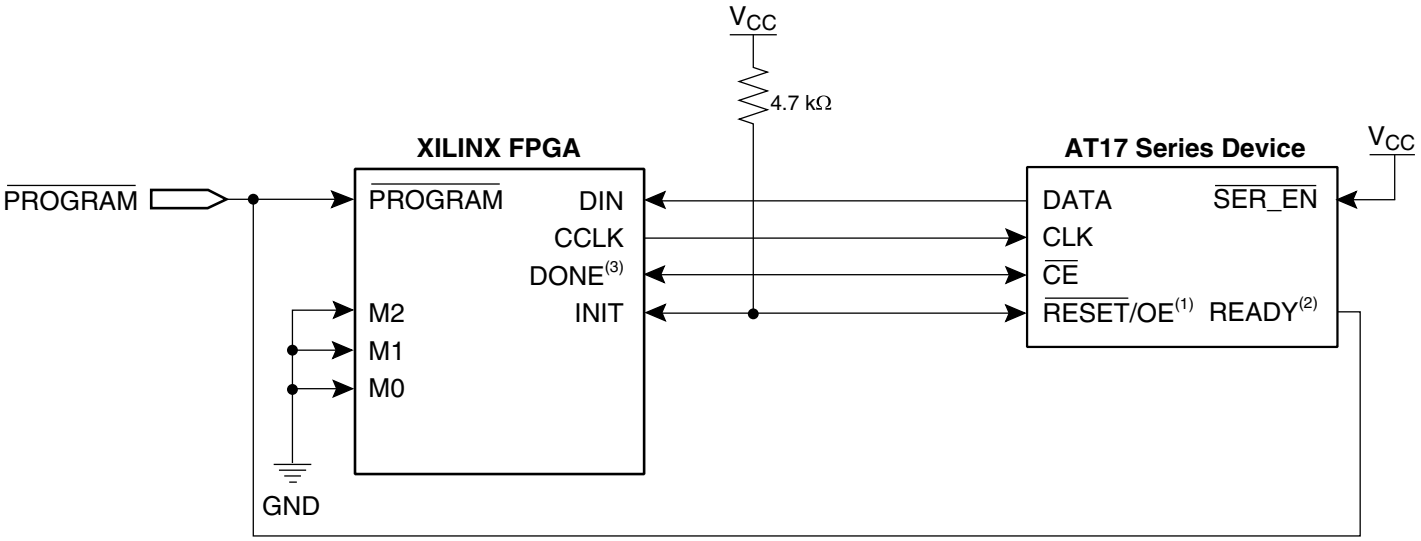
Figure 1. AT17 Series Device for Programming PSLI Devices



Notes: 1. Reset polarity must be set to active Low.
2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.

The FPGA CON/DONE output drives the CE input of the AT17 Series Configurator, while the RESET/OE input is driven by the FPGA INIT pin. This connection works under all normal circumstances, even when the user aborts the configuration before CON/DONE has gone High. A Low level on the RESET/OE input, during FPGA reset, clears the configurator's internal address pointer so that the reconfiguration starts at the beginning.

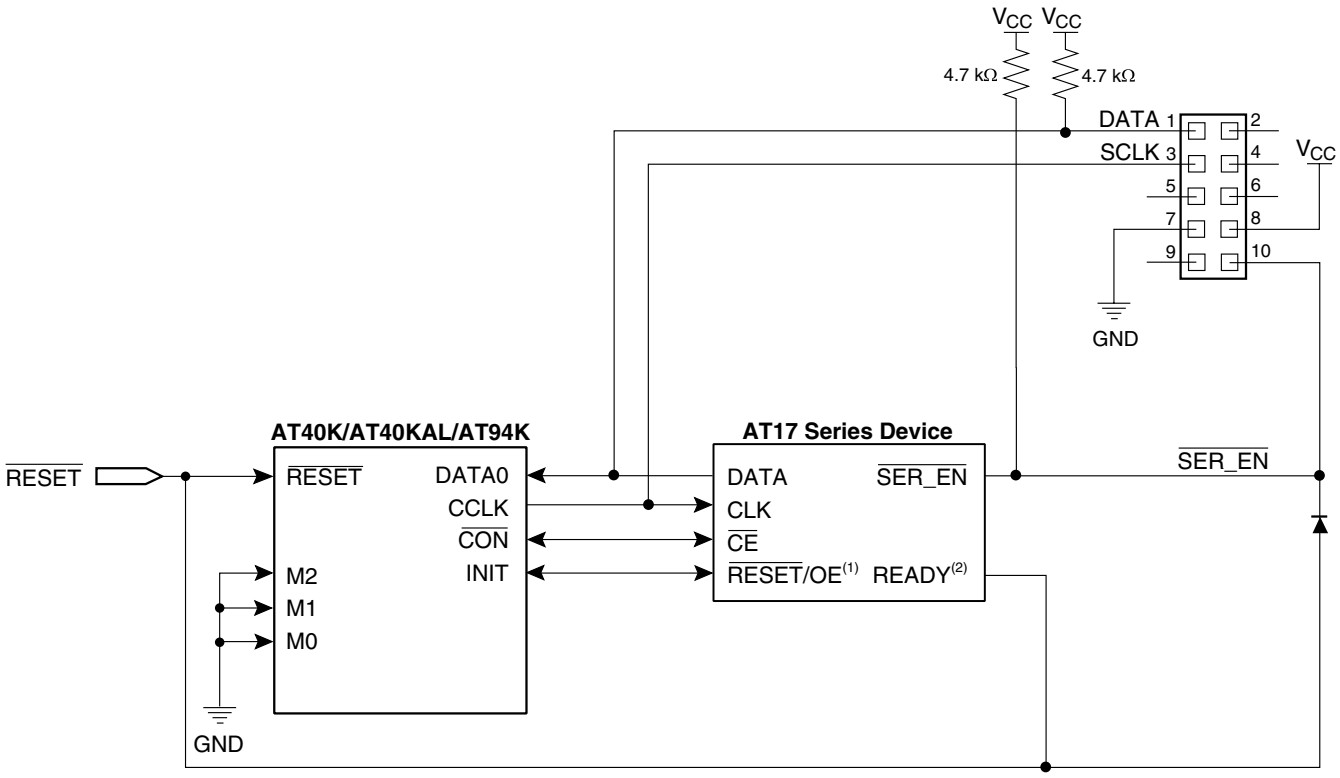
Figure 2. Drop-In Replacement of XC17/ATT17 PROMs for Xilinx/Lucent FPGA Applications



Notes: 1. Reset polarity must be set to active Low.
2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.
3. An internal pull-up resistor is enabled here for DONE.

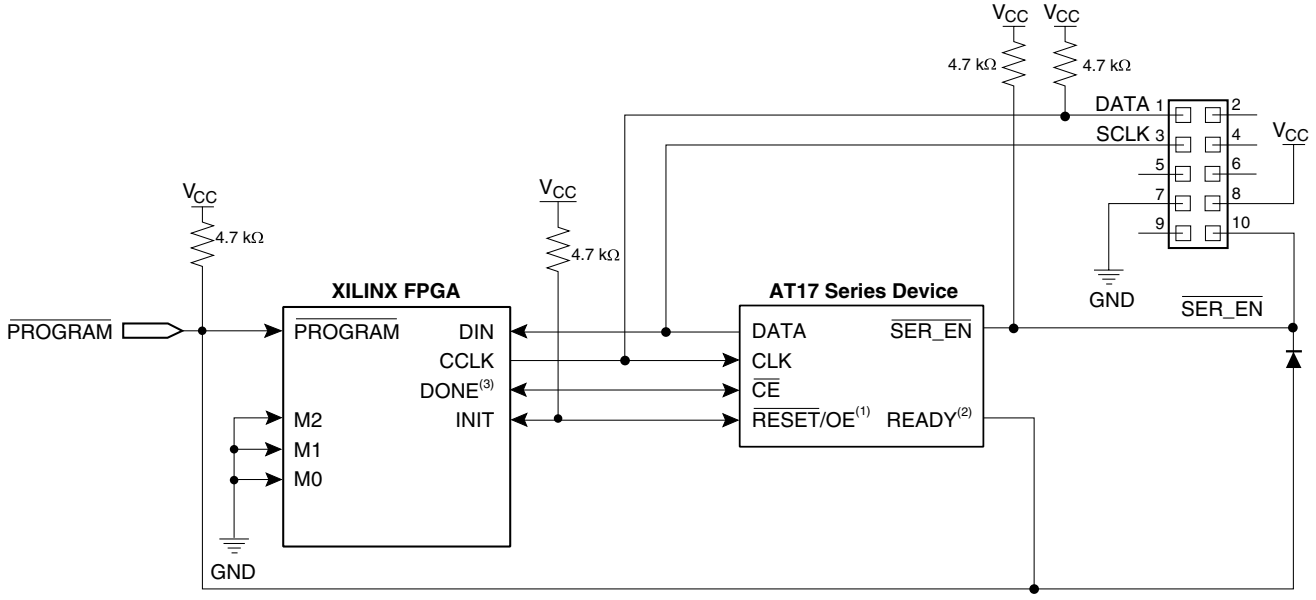
For details of ISP, please refer to the “Programming Specification for Atmel's AT17 and AT17A Series FPGA Configuration EEPROMs”, available on the Atmel web site, at http://www.atmel.com/atmel/acrobat/doc0437.pdf.

Figure 3. In-System Programming of AT17 Series for PSLI Applications



Notes: 1. Reset polarity must be set to active Low.
2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.

Figure 4. In-System Programming of AT17 Series for Xilinx/Lucent FPGA Applications



Notes: 1. Reset polarity must be set to active Low.
2. Use of the optional READY pin is not available on the AT17C/LV65/128/256 devices.
3. An internal pull-up resistor is enabled here for DONE.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to V_{CC} +0.5V
Supply Voltage (V_{CC})	-0.5V to +7.0V
Maximum Soldering Temp. (10 sec. @ 1/16 in.)	260°C
ESD (R_{ZAP} = 1.5K, C_{ZAP} = 100 pF)	2000V

*NOTICE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those listed under operating conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		AT17CXXX Min	AT17CXXX Max	AT17LVXXX Min	AT17LVXXX Max	Units
V_{CC}	Commercial	Supply voltage relative to GND -0°C to +70°C	4.75	5.25	3.0	3.6	V
	Industrial	Supply voltage relative to GND -40°C to +85°C	4.5	5.5	3.0	3.6	V
	Military	Supply voltage relative to GND -55°C to +125°C	4.5	5.5	3.0	3.6	V

DC Characteristics

V_{CC} = 5V ± 5% Commercial/5V ± 10% Industrial/Military

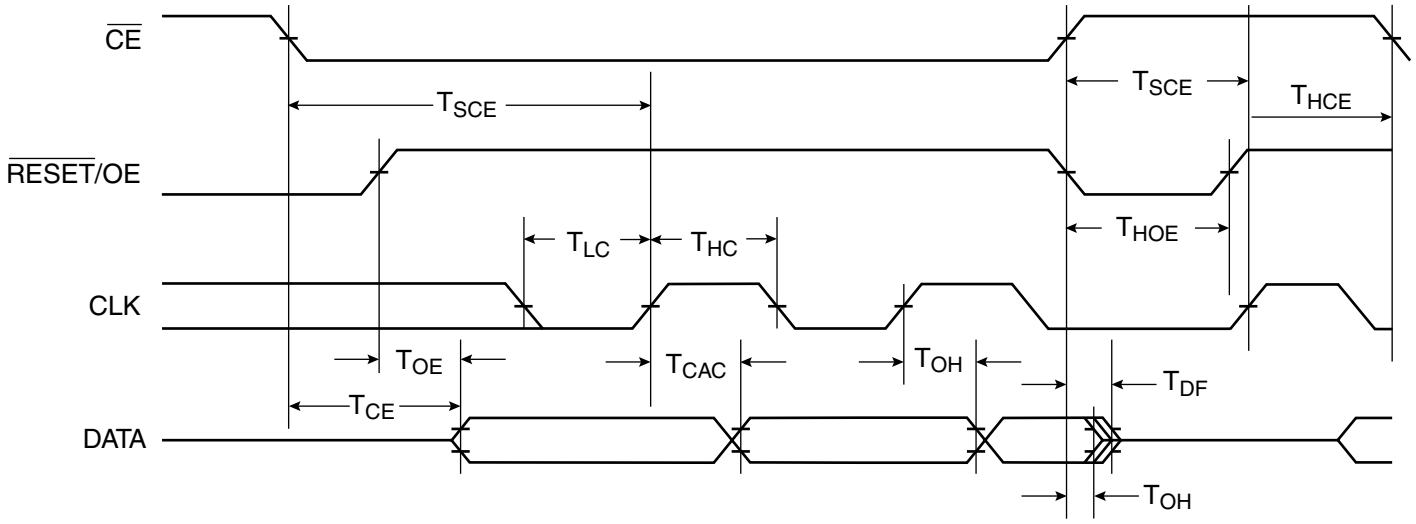
Symbol	Description		Min	Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0.0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Commercial	3.86		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Industrial	3.76		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.37	V
V_{OH}	High-level Output Voltage (I_{OH} = -4 mA)	Military	3.7		V
V_{OL}	Low-level Output Voltage (I_{OL} = +4 mA)			0.4	V
I_{CCA}	Supply Current, Active Mode			10	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		0.5	mA
		Industrial/Military		0.5	mA

DC Characteristics

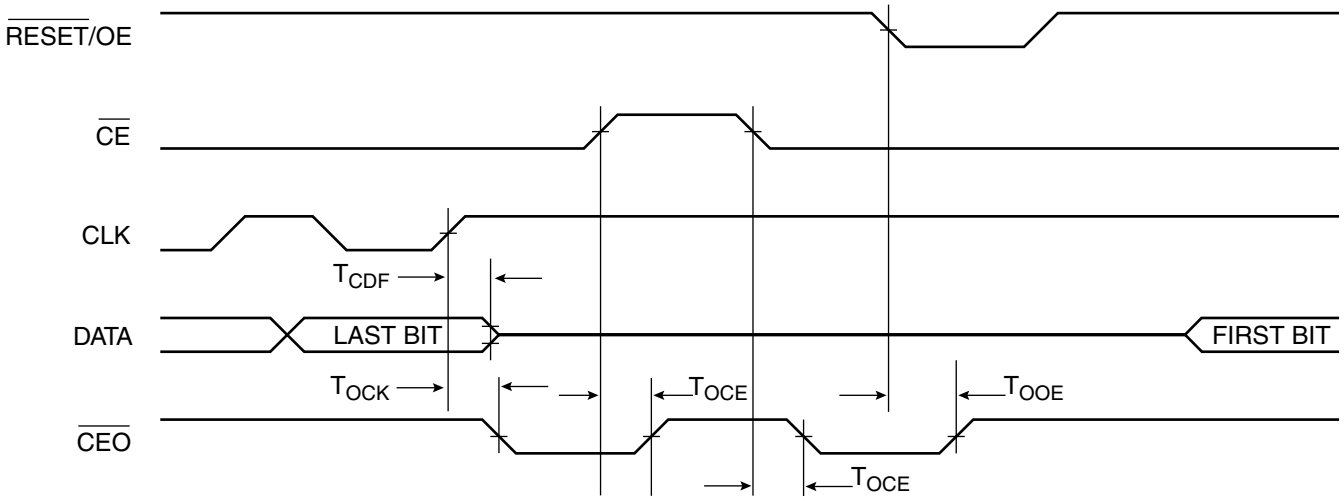
V_{CC} = 3.3V ± 10%

Symbol	Description		Min	Max	Units
V_{IH}	High-level Input Voltage		2.0	V_{CC}	V
V_{IL}	Low-level Input Voltage		0.0	0.8	V
V_{OH}	High-level Output Voltage (I_{OH} = -2.5 mA)	Commercial	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Industrial	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +3 mA)			0.4	V
V_{OH}	High-level Output Voltage (I_{OH} = -2 mA)	Military	2.4		V
V_{OL}	Low-level Output Voltage (I_{OL} = +2.5 mA)			0.4	V
I_{CCA}	Supply Current, Active Mode			5	mA
I_L	Input or Output Leakage Current (V_{IN} = V_{CC} or GND)		-10	10	µA
I_{CCS}	Supply Current, Standby Mode	Commercial		100	µA
		Industrial/Military		100	µA

AC Characteristics



AC Characteristics when Cascading



AC Characteristics for AT17C512/010

V_{CC} = 5V ± 5% Commercial/V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay		30		35	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		45		45	ns
T_{CAC}[2]	CLK to Data Delay		50		50	ns
T_{OH}	Data Hold From $\overline{CE}$, OE, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or OE to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	20		20		ns
T_{HC}	CLK High Time	20		20		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	20		25		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE High Time (guarantees counter Is reset)	20		20		ns
F_{MAX}	MAX Input Clock Frequency	15		15		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.

AC Characteristics for AT17C512/010 when Cascading

V_{CC} = 5V± 5% Commercial/V_{CC} = 5V ± 10% Industrial/Military

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		35		40	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		35		35	ns
T_{OOE}[2]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		30		30	ns
F_{MAX}	MAX Input Clock Frequency	12.5		12.5		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.

AC Characteristics for AT17LV512/010

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{OE}[2]	OE to Data Delay		50		55	ns
T_{CE}[2]	$\overline{CE}$ to Data Delay		55		60	ns
T_{CAC}[2]	CLK to Data Delay		55		60	ns
T_{OH}	Data Hold From $\overline{CE}$, OE, or CLK	0		0		ns
T_{DF}[3]	$\overline{CE}$ or OE to Data Float Delay		50		50	ns
T_{LC}	CLK Low Time	25		25		ns
T_{HC}	CLK High Time	25		25		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	30		35		ns
T_{HCE}	$\overline{CE}$ Hold Time from CLK (to guarantee proper counting)	0		0		ns
T_{HOE}	OE High Time (guarantees counter is reset)	25		25		ns
F_{MAX}	MAX Input Clock Frequency	15		10		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.

AC Characteristics for AT17LV512/010 when Cascading

V_{CC} = 3.3V ± 10%

Symbol	Description	Commercial		Industrial/Military[1]		Units
		Min	Max	Min	Max	
T_{CDF}[3]	CLK to Data Float Delay		50		50	ns
T_{OCK}[2]	CLK to $\overline{CEO}$ Delay		50		55	ns
T_{OCE}[2]	$\overline{CE}$ to $\overline{CEO}$ Delay		35		40	ns
T_{OOE}[2]	$\overline{RESET}$/OE to $\overline{CEO}$ Delay		35		35	ns
F_{MAX}	MAX Input Clock Frequency	12.5		10		MHz

Notes: 1. Preliminary specifications for military operating range only.
2. AC test load = 50 pF.
3. Float delays are measured with 5 pF AC loads. Transition is measured ± 200 mV from steady state active levels.

Thermal Resistance Coefficients(1)

Package Type		θ_{JC} [°C/W]	θ_{JA} [°C/W] Airflow = 0 ft/min
Leadless Array Package (LAP)	8CN4	45	135.71
Plastic Dual Inline Package (PDIP)	8P3	37	107
Plastic Leaded Chip Carrier (PLCC)	20J	35	90

Note: 1. For more information refer to the “Thermal Characteristics of Atmel’s Packages”, available on the Atmel web site, at http://www.atmel.com/atmel/acrobat/doc0636.pdf.

Ordering Information – 5V Devices

Memory Size	Ordering Code	Package	Operation Range
512-Kbit	AT17C512-10CC AT17C512-10PC AT17C512-10JC	8CN4 8P3 20J	Commercial (0°C to 70°C)
	AT17C512-10CI AT17C512-10PI AT17C512-10JI	8CN4 8P3 20J	Industrial (-40°C to 85°C)
1-Mbit	AT17C010-10CC AT17C010-10PC AT17C010-10JC	8CN4 8P3 20J	Commercial (0°C to 70°C)
	AT17C010-10CI AT17C010-10PI AT17C010-10JI	8CN4 8P3 20J	Industrial (-40°C to 85°C)

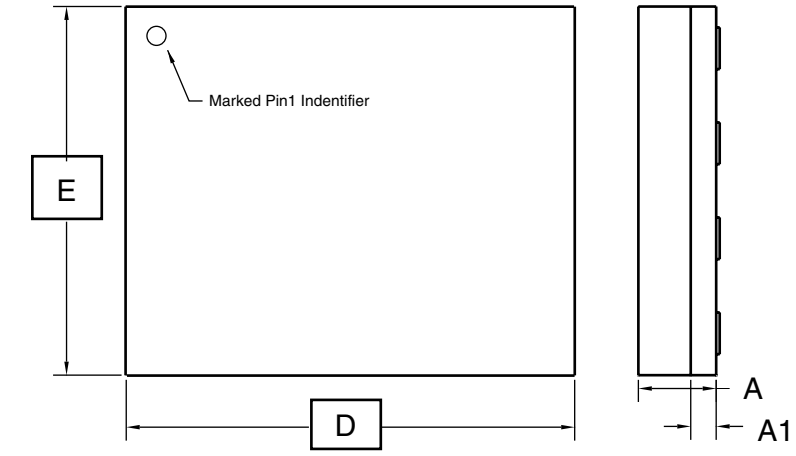
Ordering Information – 3.3V Devices

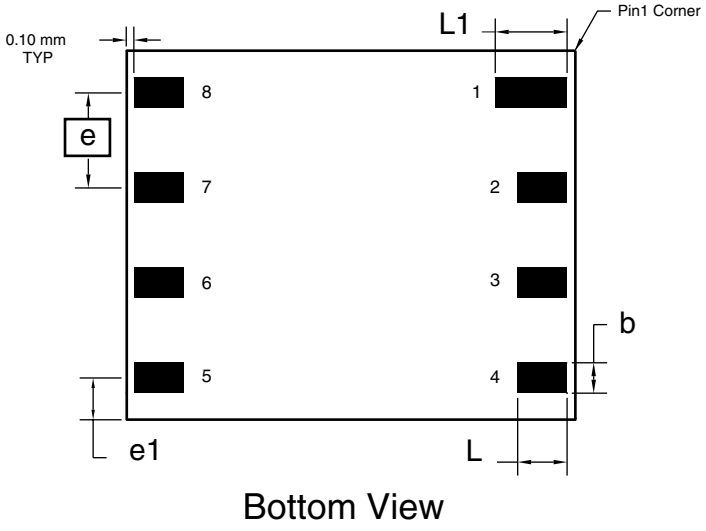
Memory Size	Ordering Code	Package	Operation Range
512-Kbit	AT17LV512-10CC AT17LV512-10PC AT17LV512-10JC	8CN4 8P3 20J	Commercial (0°C to 70°C)
	AT17LV512-10CI AT17LV512-10PI AT17LV512-10JI	8CN4 8P3 20J	Industrial (-40°C to 85°C)
1-Mbit	AT17LV010-10CC AT17LV010-10PC AT17LV010-10JC	8CN4 8P3 20J	Commercial (0°C to 70°C)
	AT17LV010-10CI AT17LV010-10PI AT17LV010-10JI	8CN4 8P3 20J	Industrial (-40°C to 85°C)

Package Type	
8CN4	8-lead, 6 mm x 6 mm x 1 mm, Leadless Array Package (LAP) – Pin-compatible with 8-lead SOIC/VOID Packages
8P3	8-lead, 0.300" Wide, Plastic Dual Inline Package (PDIP)
20J	20-lead, Plastic J-leaded Chip Carrier (PLCC)

Packaging Information

8CN4 – LAP





COMMON DIMENSIONS
(Unit of Measure = mm)

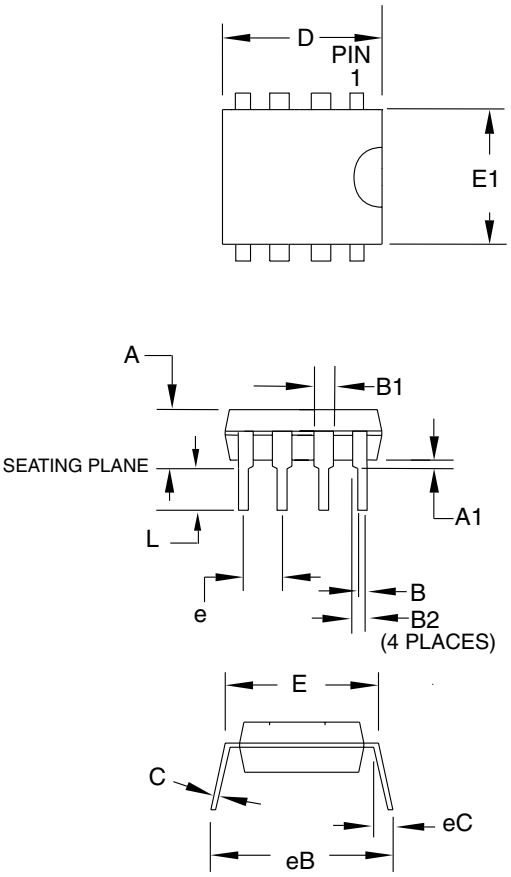
SYMBOL	MIN	NOM	MAX	NOTE
A	0.94	1.04	1.14	
A1	0.30	0.34	0.38	
b	0.45	0.50	0.55	1
D	5.89	5.99	6.09	
E	4.89	5.99	6.09	
e		1.27 BSC		
e1		1.10 REF		
L	0.95	1.00	1.05	1
L1	1.25	1.30	1.35	1

Note: 1. Metal Pad Dimensions.

11/14/01

1150 E.Cheyenne Mtn Blvd. Colorado Springs, CO 80906	**TITLE** **8CN4**, 8-lead (6 x 6 x 1.04 mm Body), Lead Pitch 1.27 mm, Leadless Array Package (LAP)	**DRAWING NO.** 8CN4	**REV.** A

8P3 – PDIP



COMMON DIMENSIONS
(Unit of Measure = mm)

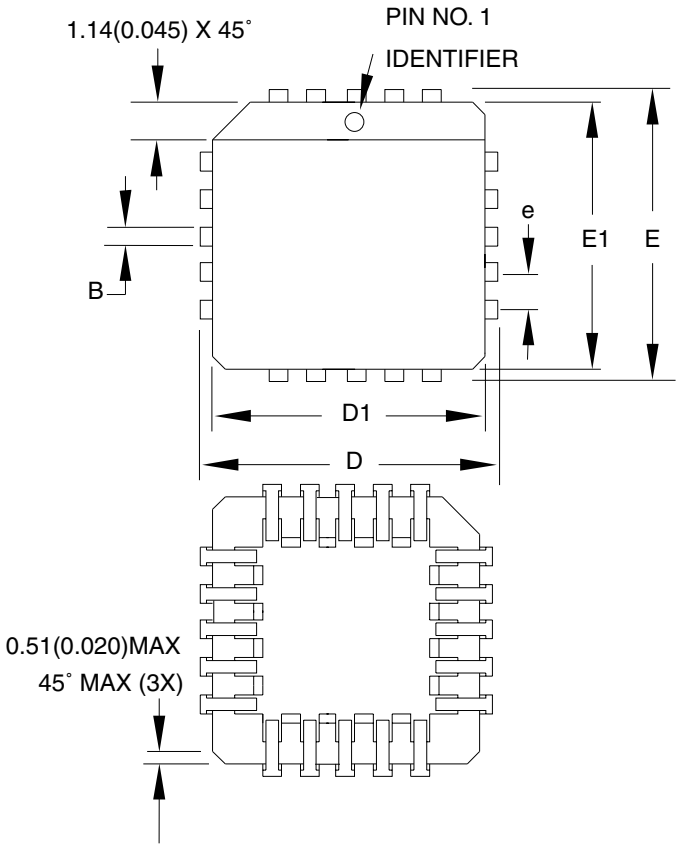
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.318	
A1	0.381	–	–	
D	9.144	–	9.652	Note 2
E	7.620	–	8.255	
E1	6.096	–	6.604	Note 2
B	0.406	–	0.508	
B1	1.397	–	1.651	
B2	0.762	–	1.143	
L	3.175	–	3.429	
C	0.203	–	0.356	
eB	–	–	10.922	
eC	0.000	–	1.524	
e	2.540 TYP			

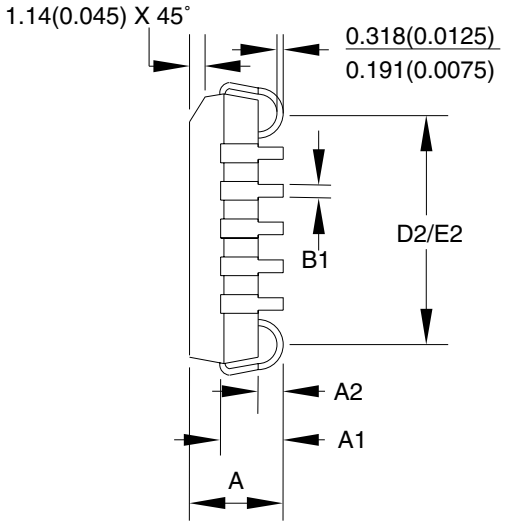
Notes: 1. This package conforms to JEDEC reference MS-001 BA.
2. Dimensions D and E1 do not include mold Flash or Protrusion. Mold Flash or Protrusion shall not exceed 0.25 mm (0.010").

09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**8P3**, 8-lead (0.300"/7.62 mm Wide) Plastic Dual Inline Package (PDIP)	8P3	B

20J – PLCC





COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	4.191	–	4.572	
A1	2.286	–	3.048	
A2	0.508	–	–	
D	9.779	–	10.033	
D1	8.890	–	9.042	Note 2
E	9.779	–	10.033	
E1	8.890	–	9.042	Note 2
D2/E2	7.366	–	8.382	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

Notes:
1. This package conforms to JEDEC reference MS-018, Variation AA.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**20J**, 20-lead, Plastic J-leaded Chip Carrier (PLCC)	20J	B

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel SarL
Route des Arsenaux 41
Casa Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
Atmel Corporate
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 436-4270
FAX 1(408) 436-4314

Microcontrollers
Atmel Corporate
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 436-4270
FAX 1(408) 436-4314

Atmel Nantes
La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Atmel Rousset
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

Atmel Colorado Springs
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Atmel Smart Card ICs
Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Atmel Heilbronn
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

Atmel Colorado Springs
1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Atmel Grenoble
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

Atmel Configurator Hotline
(408) 436-4119

Atmel Configurator e-mail
configurator@atmel.com

FAQ
Available on web site

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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