Spartan-II/Spartan-IIE Family OTP Configuration PROMs (XC17S00A)

DS078 (v1.10) June 25, 2007 **Product Specification**

Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams for Spartan™-II/Spartan-IIE FPGA devices
- Simple interface to the Spartan device
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- 3.3V PROM
- Available in compact plastic 8-pin DIP, 8-pin VOIC, 20-pin SOIC, or 44-pin VQFP packages
- Programming support by leading programmer manufacturers
- Design support using the Xilinx Alliance and Foundation™ series software packages
- Guaranteed 20-year life data retention
- Pb-free (RoHS-compliant) packaging available

Introduction

The XC17S00A family of PROMs provide an easy-to-use, cost-effective method for storing Spartan-II/Spartan-IIE device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the Spartan device D_{IN} pin. The Spartan device generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When a Spartan device is in Slave Serial mode, the PROM and the Spartan device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

Spartan-II/IIE FPGA	Configuration Bits	Compatible Spartan-II/IIE PROM
XC2S15	197,696	XC17S15A
XC2S30	336,768	XC17S30A
XC2S50	559,200	XC17S50A
XC2S100	781,216	XC17S100A
XC2S150	1,040,096	XC17S150A
XC2S200	1,335,840	XC17S200A
XC2S50E	630,048	XC17S50A
XC2S100E	863,840	XC17S100A
XC2S150E(1)	1,134,496	XC17S200A
XC2S200E	1,442,016	XC17S200A
XC2S300E	1,875,648	XC17S300A
XC2S400E	2,693,440	XC17V04(2)
XC2S600E	3,961,632	XC17V04(2)

Notes:

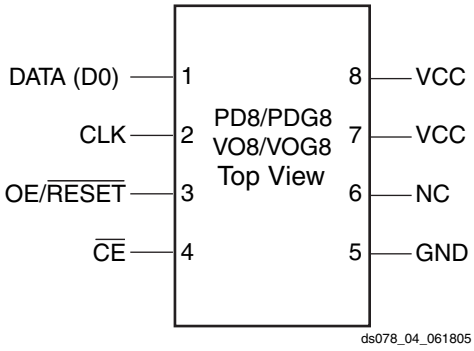
1. Due to the higher configuration bit requirements of the XC2S150E device, an XC17S200A PROM is required to configure this FPGA.
2. See XC17V00 series configuration PROMs data sheet at: http://direct.xilinx.com/bvdocs/publications/ds073.pdf

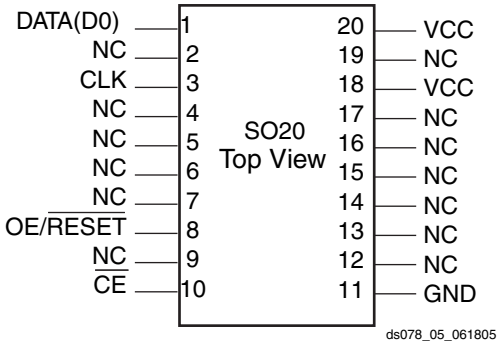
Pin Description

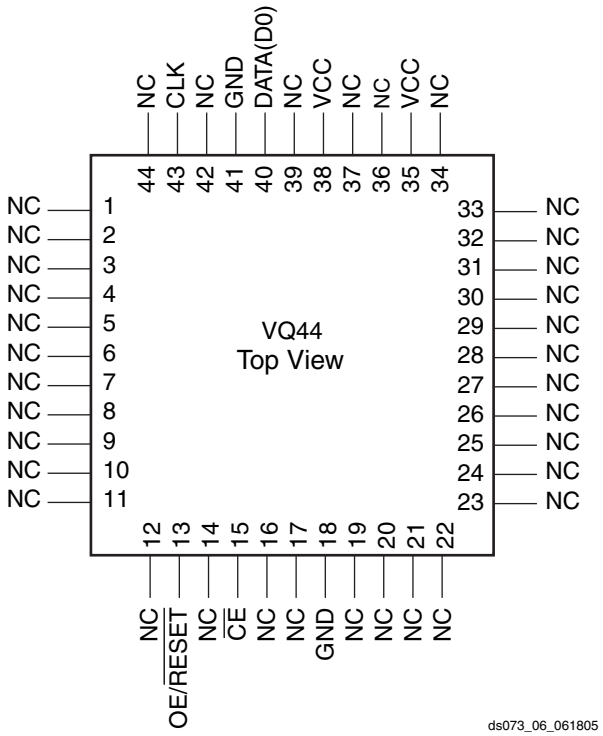
Pins not listed are no connects.

Pin Name	8-pin PDIP (PD8/PDG8) and VOIC/TSOP (VO8/VOG8)	20-pin SOIC (SO20)	44-pin VQFP (VQ44)	Pin Description
DATA	1	1	40	• Data output, High-Z state when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.
CLK	2	3	43	• Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	8	13	• When High, this input holds the address counter reset and puts the DATA output in a high-impedance state. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is in a high-impedance state. The polarity of this input is programmable. The default is active-High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be connected to the FPGAs $\overline{INIT}$ pin and a pull-up resistor. • The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.
$\overline{CE}$	4	10	15	• When High, this pin resets the internal address counter, puts the DATA output in a high-impedance state, and forces the device into low-I_{CC} standby mode.
GND	5	11	18, 41	• GND is the ground connection.
V_{CC}	7, 8	18, 20	38, 35	• The V_{CC} pins are to be connected to the positive voltage supply.

Pinout Diagrams







Controlling PROMs

- Connecting the Spartan device with the PROM:
- The DATA output of the PROM drives the D_{IN} input of the lead Spartan device.
- The Master Spartan device CCLK output drives the CLK input of the PROM.
- The $\overline{\text{RESET}}$/OE input of the PROM is connected to the $\overline{\text{INIT}}$ pin of the Spartan device and a pull-up resistor. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The $\overline{\text{CE}}$ input of the PROM is connected to the DONE pin of the Spartan device and a pull-up resistor. $\overline{\text{CE}}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

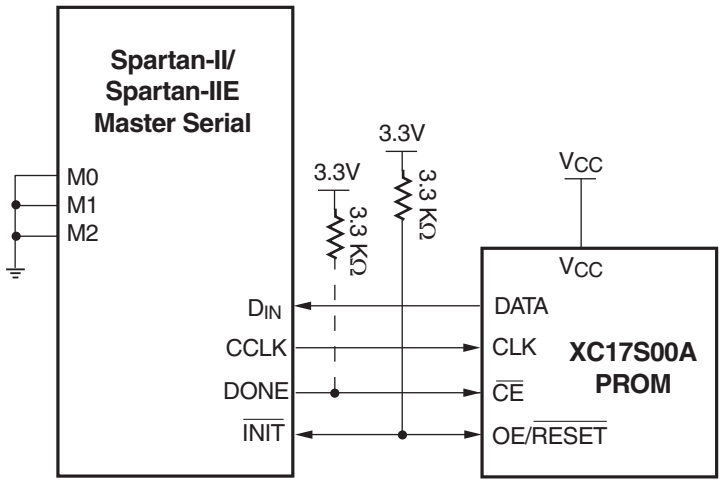
The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the Spartan device mode pins. In Master Serial mode, the Spartan device automatically loads the configuration program from an external memory. The XC17S00A PROM has been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, the Spartan device enters the Master Serial mode when the mode pins are set to Master Serial mode. Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial mode provides a simple configuration interface (Figure 1). Only a serial data line, two control lines, and a clock line are required to configure the Spartan device. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function D_{IN} pin on the Spartan device is used only for configuration, it must still be held at a defined level during normal operation. The Spartan-II/Spartan-IIE family takes care of this automatically with an on-chip pull-up/down resistor or keeper circuit.

The one-time-programmable XC17S00A PROM in Figure 1, page 3 supports automatic loading of configuration programs. An early DONE inhibits the PROM data output one CCLK cycle before the Spartan FPGA I/Os become active.



Notes:
1. If the DriveDone configuration option is not active, pull up DONE with a 3.3 kΩ resistor.

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Figure 1: **XC17S00A PROM Connections to FPGA in Master Serial Mode**

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high-impedance state regardless of the state of the $\overline{OE}$ input.

Programming Spartan-II/Spartan-IIE Family PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

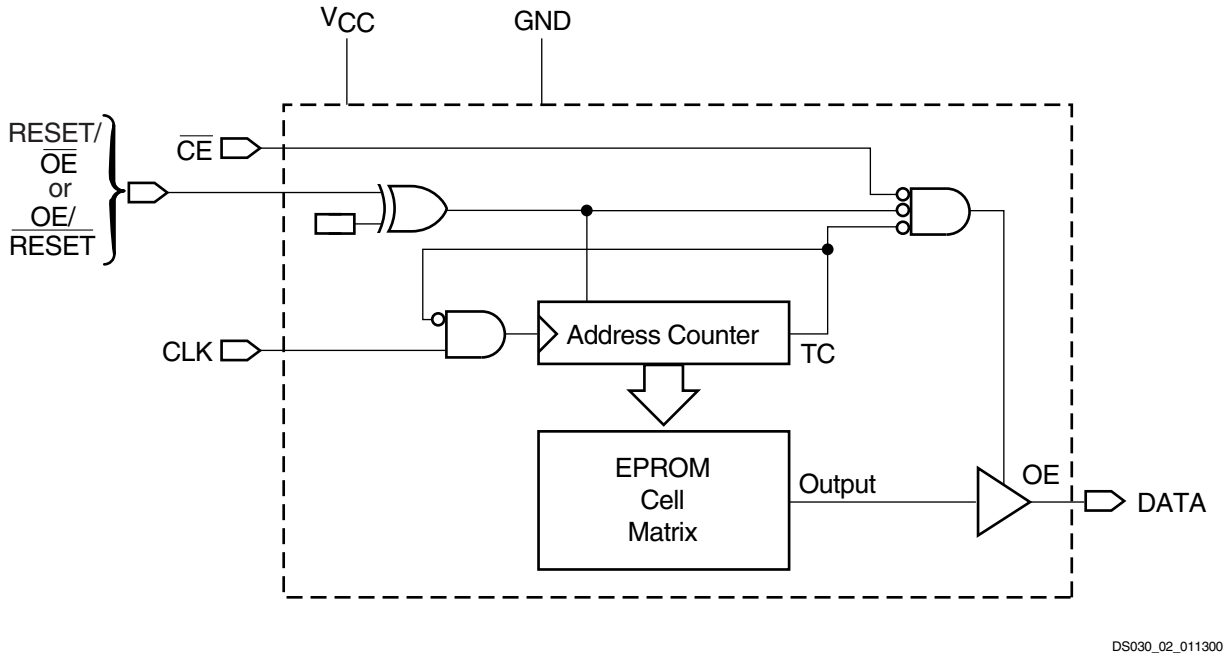


Figure 2: **Simplified Block Diagram (does not show programming circuit)**

Caution! Always tie the two V_{CC} pins together.

Table 1: **Truth Table for XC17S00A Control Inputs**

Control Inputs		Internal Address(2)	Outputs	
RESET(1)	CE		DATA	I_{CC}
Inactive	Low	If address ≤ TC: increment If address > TC: don't change	Active High-Z	Active Reduced
Active	Low	Held reset	High-Z	Active
Inactive	High	Not changing	High-Z	Standby
Active	High	Held reset	High-Z	Standby

Notes:

1. The XC17S00A RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC + 1 = address 0.

XC17S15A, XC17S30A, XC17S50A, XC17S100A, XC17S150A, XC17S200A, and XC17S300A

Absolute Maximum Ratings(1)

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to High-Z output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C

Notes:

1. Stresses beyond those listed under Absolute Maximum Ratings might cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time might affect device reliability.

Operating Conditions(1)

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0° C to +70° C)	3.0	3.6	V
	Industrial	Supply voltage relative to GND (T_A = –40° C to +85° C)	3.0	3.6	V
T_{VCC}		V_{CC} rise time from 0V to nominal voltage	1.0	50	ms

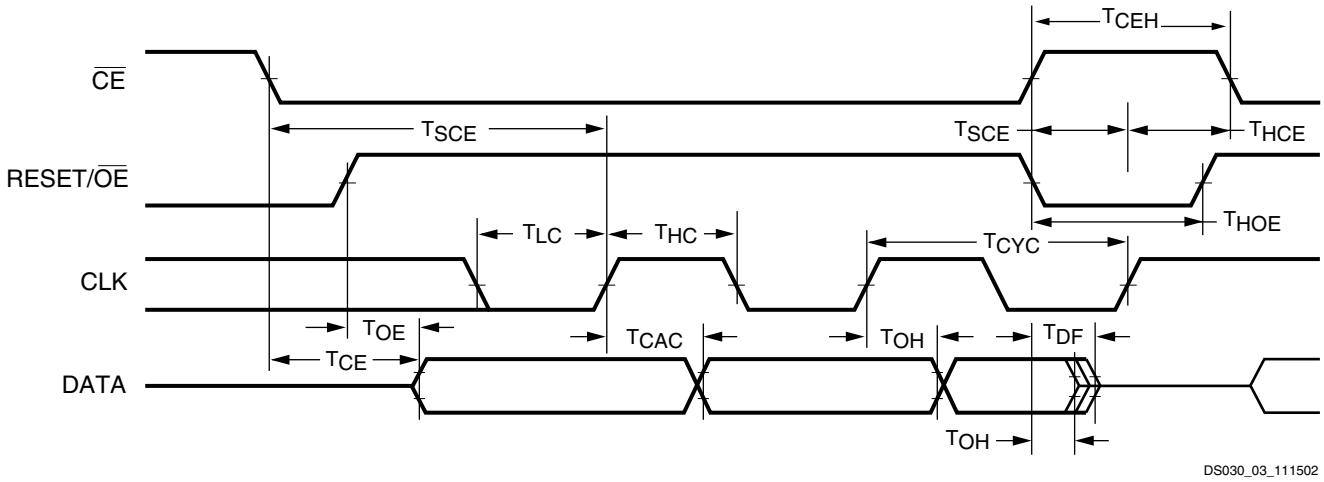
Notes:

1. During normal read operation, both V_{CC} pins must be connected together.
2. At power-up, the device requires the V_{CC} power supply to monotonically rise from 0V to nominal voltage within the specified V_{CC} rise time. If the power supply cannot meet this requirement, then the device may not perform a power-on-reset properly.

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)	2.4	–	V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)	–	0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)	–	15	mA
I_{CCS}	Supply current, standby mode	–	1	mA
I_L	Input or output leakage current	–10	10	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0 MHz)	–	10	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0 MHz)	–	10	pF

AC Characteristics Over Operating Condition[1]

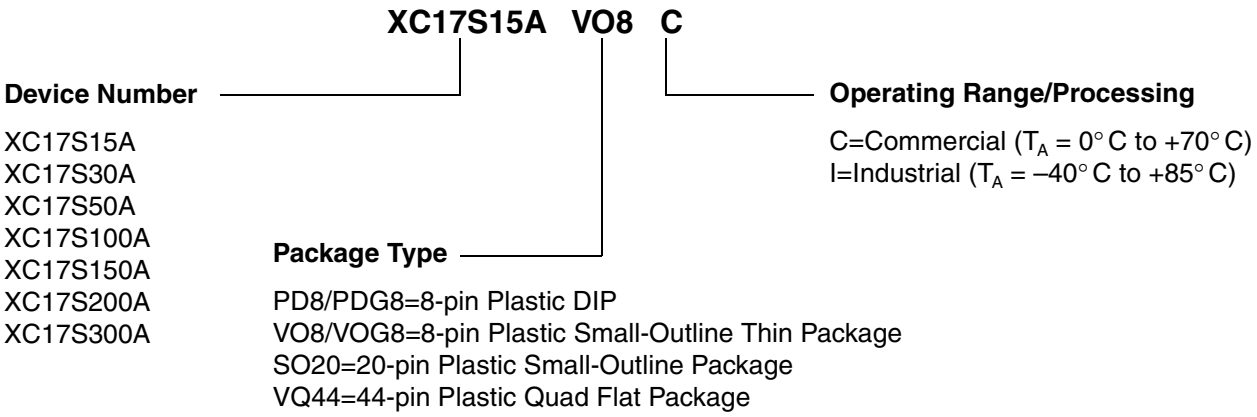


Symbol	Description	Min	Max	Units
T_{OE}	RESET/$\overline{OE}$ to Data Delay	–	45	ns
T_{CE}	$\overline{CE}$ to Data Delay	–	60	ns
T_{CAC}	CLK to Data Delay	–	80	ns
T_{OH}	Data Hold From $\overline{CE}$, RESET/$\overline{OE}$, or CLK[2]	0	–	ns
T_{DF}	$\overline{CE}$ or RESET/$\overline{OE}$ to Data Float Delay[2,3]	–	50	ns
T_{CYC}	Clock Periods	100	–	ns
T_{LC}	CLK Low Time[2]	50	–	ns
T_{HC}	CLK High Time[2]	50	–	ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25	–	ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0	–	ns
T_{HOE}	RESET/$\overline{OE}$ Hold Time (guarantees counters are reset)	25	–	ns
T_{CEH}	CE High time (guarantees counters are reset)	20	–	ns

Notes:

1. AC test load = 50 pF
2. Guaranteed by design, not tested.
3. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{CEH} High < 2µs, T_{CE} = 2 µs.
6. If T_{HOE} High < 2µs, T_{CE} = 2 µs.

Ordering Information

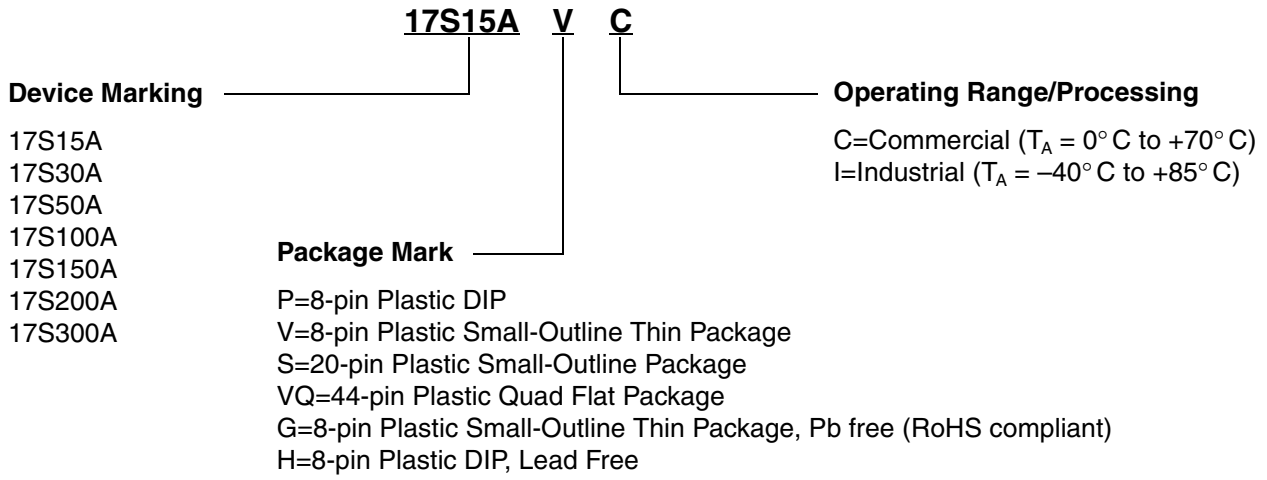


3.3V Valid Ordering Combinations

XC17S15APD8C	XC17S50APD8C	XC17S150APD8C
XC17S15AVO8C	XC17S50APDG8C	XC17S150AVO8C
XC17S15AVOG8C	XC17S50AVO8C	XC17S150ASO20C
XC17S15ASO20C	XC17S50AVOG8C	XC17S150APD8I
XC17S15APD8I	XC17S50ASO20C	XC17S150AVO8I
XC17S15AVO8I	XC17S50APD8I	XC17S150ASO20I
XC17S15ASO20I	XC17S50AVO8I	
	XC17S50ASO20I	
XC17S30APD8C	XC17S100APD8C	XC17S200APD8C
XC17S30AVO8C	XC17S100AVO8C	XC17S200APDG8C
XC17S30ASO20C	XC17S100AVOG8C	XC17S200AVO8C
XC17S30APD8I	XC17S100ASO20C	XC17S200AVOG8C
XC17S30AVO8I	XC17S100APD8I	XC17S200APD8I
XC17S30ASO20I	XC17S100AVO8I	XC17S200APDG8I
	XC17S100ASO20I	XC17S200AVO8I
		XC17S200AVOG8I
		XC17S200AVQ44C
		XC17S200AVQ44I
		XC17S300AVQ44C
		XC17S300AVQ44I

Marking Information

Due to the small size of the PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.



Revision History

The following table shows the revision history for this document.

Date	Revision	Revision
09/14/00	1.0	Initial Xilinx release.
11/13/00	1.1	Updated configuration bits.
04/07/01	1.2	Added to features: “Guaranteed 20 year life data retention”, removed “Programming the FPGA with counters” and related text.
06/20/01	1.3	Revised Figure 1 resistor values to match Spartan-II data sheet.
10/09/01	1.4	Added note for unlisted pins, changed I_{CCA} and I_{CCS}, and added power-on supply requirements and note regarding power-on reset.
11/15/01	1.5	Updated for Spartan-IIE FPGA family.
06/25/02	1.6	Changed Table 1, page 4.
10/15/02	1.7	Changed Table 1, page 4. Added "Pinout Diagrams," page 2.
11/18/02	1.8	Added XC2S400E and XC2S600E to Compatible FPGAS table. Modified document title.
06/24/05	1.9	Added Pb-free information to the "Pinout Diagrams", "Ordering Information", "3.3V Valid Ordering Combinations", and "Marking Information" figures. Removed T_{SOL} from the "Absolute Maximum Ratings(1)" table.
06/25/07	1.10	• Updated format. • Added Pb-free (RoHS-compliant) packaging. • Timing diagram removed from Figure 1, page 3. • Part Numbers XC17S200APDG8I, and XC17S200AVOG8I added to "3.3V Valid Ordering Combinations," page 7.