TOSHIBA MOS DIGITAL INTEGRATE CIRCUIT SILICON GATE CMOS

64M (4M × 16 BITS) CMOS FLASH MEMORY

Lead-Free

1. DESCRIPTION

The TC58FVM6(T/B)5B is a 67108864-bit, 3V read-only electrically erasable and programmable flash memory organized as 4194304 × 16 bits. The TC58FVM6(T/B)5B features commands for Read, Program and Erase operations to allow easy interfacing with microprocessors. The commands are based on the JEDEC standard. The Program and Erase operations are automatically executed in the chip. The TC58FVM6(T/B)5B also features a Simultaneous Read/Write operation so that data can be read during a Write or Erase operation.

2. FEATURES

- Power supply voltage
  V_{DD} = 2.7V to 3.6V
- Operating ambient temperature
  Ta = -40°C to 85°C
- Organization
  4M × 16 Bits
- Functions
  Simultaneous Read/Write
  Page Read
  Auto Program, Auto Page Program
  Auto Block Erase, Auto Chip Erase
  Fast Program Mode/Acceleration Mode
  Program Suspend/Resume
  Erase Suspend/Resume
  Data polling/Toggle bit
  Password block protection
  Block protection/ Boot block protection
  Automatic Sleep, support for hidden ROM area
  Common Flash memory Interface (CFI)
- Block erase architecture
  8 × 8 Kbytes / 127 × 64 Kbytes
- Bank architecture
  8M Bits × 8 Bank
- Boot Block architecture
  TC58FVM6T5B ··· top boot block
  TC58FVM6B5B ··· bottom boot block
- Mode control
  Compatible with JEDEC standard commands
- Erase/Program cycles
  10^5 cycles typ
- Access Time (Random/Page)
  65ns / 25ns (CL=30pF)
  70ns / 30ns (CL=100pF)
- Page Length: 8 words
- Power consumption
  10 μA (Standby)
  15mA (Program/Erase operation)
  5mA (Page Read operation)
  55mA (Random Read operation)
  11mA (Address Increment Read operation)
- Package
  TC58FVM6(T/B)5BTG
  TSOP I 48-P-1220-0.50 (weight: 0.51g)
  TC58FVM6(T/B)5BXG
  P-TFBGA56-0710-0.80DZ (weight: 0.125g)
- Lead-Free

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TABLE OF CONTENTS

64M (4M × 16 BITS) CMOS FLASH MEMORY 1

1. DESCRIPTION 1
2. FEATURES 1
3. ORDERING INFORMATION 3
4.PIN ASSIGNMENT (TOP VIEW) 4
5. BLOCK DIAGRAM 5
6. MODE SELECTION 6
7. ID CODE TABLE 6
8. COMMAND SEQUENCES 7
9. SIMULTANEOUS READ/WRITE OPERATION 9
10. OPERATION MODES 10
10.1. Read Mode 10
10.2. ID Read Mode 10
10.3. Standby Mode 10
10.4. Auto-Sleep Mode 10
10.5. Output Disable Mode 10
10.6. Command Write 11
10.7. Software Reset: Read/Reset Command 11
10.8. Hardware Reset 11
10.9. Comparison between Software Reset and Hardware Reset 11
10.10. Auto-Program Mode 12
10.11. Auto-Page Program Mode 12
10.12. Fast Program Mode 12
10.13. Acceleration Mode 12
10.14. Program Suspend/Resume Mode 13
10.15. Auto Chip Erase Mode 13
10.16. Auto Block Erase/Auto Multi-Block Erase Modes 13
10.17. Erase Suspend/Erase Resume Modes 14
10.18. Block Protection 15
10.19. Hidden ROM Area 20
10.20. CFI (Common Flash memory Interface) 21
10.21. HARDWARE SEQUENCE FLAGS 24
11. DATA PROTECTION 26
11.1. Protection against Program/Erase Caused by Low Supply Voltage 26
11.2. Protection against Malfunction Caused by Glitches 26
11.3. Protection against Malfunction at Power-on 26
12. ABSOLUTE MAXIMUM RATINGS 27
13. CAPACITANCE (T_A = 25°C, f = 1 MHz) 27
14. RECOMMENDED DC OPERATING CONDITIONS 27
15. DC CHARACTERISTICS 28
16. AC TEST CONDITIONS 28
17. AC CHARACTERISTICS AND OPERATING CONDITIONS 29
17.1. Read Cycle 29
17.2. Block Protect 29
17.3. Program and Erase characteristics 30
17.4. Command Write/Program/Erase cycle 31
18. TIMING DIAGRAMS 32
19. FLOWCHARTS 48
20. BLOCK ADDRESS TABLES 65
20.1. TC58FVM6T5B (Top Boot Block) 1/5 65
20.2. TC58FVM6B5B (Bottom Boot Block) 1/5 70
21. BLOCK SIZE TABLE 75
21.1. TC58FVM6T5B (Top Boot Block) 75
21.2. TC58FVM6B5B (Bottom Boot Block) 76
22. PACKAGE DIMENSIONS 77

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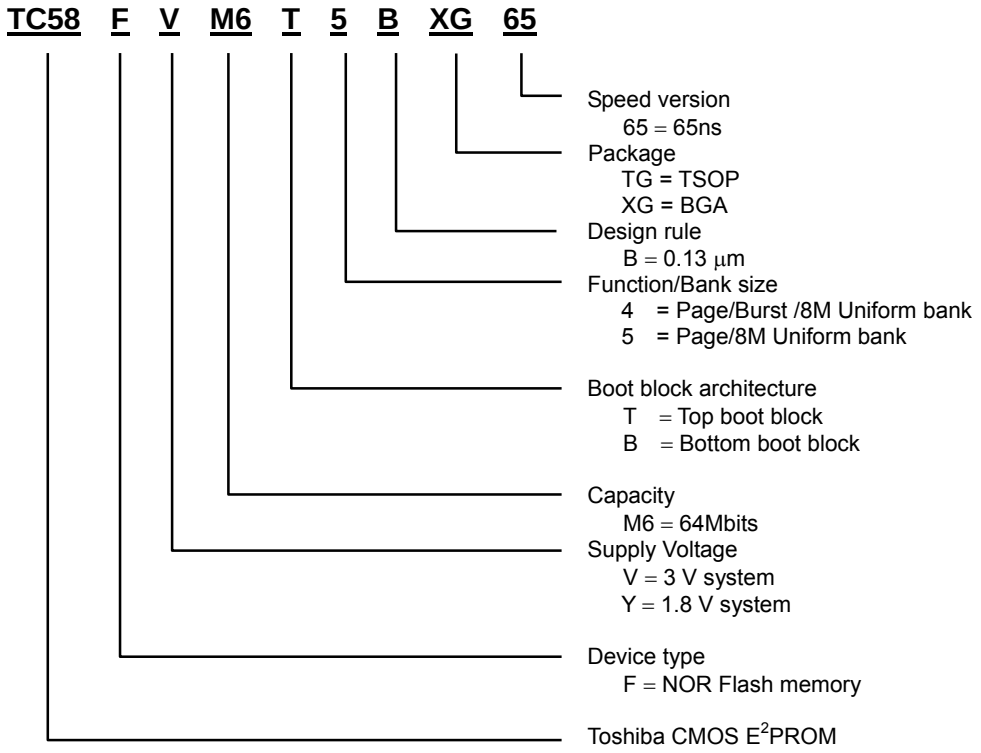
3. ORDERING INFORMATION



Ordering type	Function	Boot Block	Speed version	Package
TC58FVM6T5BXG65	Page	Top	65 ns	P-TFBGA56-0710-0.80DZ (Lead-free)
TC58FVM6B5BXG65		Bottom		
TC58FVM6T5BTG65		Top		TSOPI48-P-1220-0.50 (Lead-free)
TC58FVM6B5BTG65		Bottom		

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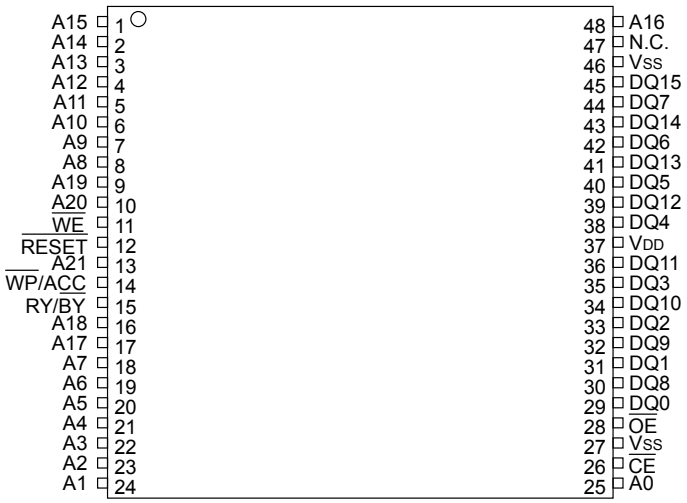
4.PIN ASSIGNMENT (TOP VIEW)

TC58FVM6T5BTG / TC58FVM6B5BTG



PIN NAMES

A0~A21	Address Input
DQ0~DQ15	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
$\overline{WE}$	Write Enable Input
RY/$\overline{BY}$	Ready/Busy Output
$\overline{RESET}$	Hardware Reset Input
$\overline{WP}$/ACC	Write Protect / Program Acceleration Input
V_{DD}	Power Supply
V_{SS}	Ground
N.C.	No Connection

TC58FVM6T5BXG / TC58FVM6B5BXG

	1	2	3	4	5	6	7	8
A	NC							NC
B	NC							NC
C		A3	A7	RY/$\overline{BY}$	$\overline{WE}$	A9	A13	
D		A4	A17	$\overline{WP}$/ACC	$\overline{RESET}$	A8	A12	
E		A2	A6	A18	A21	A10	A14	
F		A1	A5	A20	A19	A11	A15	
G		A0	DQ0	DQ2	DQ5	DQ7	A16	
H		$\overline{CE}$	DQ8	DQ10	DQ12	DQ14	NC	
J		$\overline{OE}$	DQ9	DQ11	V_{DD}	DQ13	DQ15	
K		V_{SS}	DQ1	DQ3	DQ4	DQ6	V_{SS}	
L	NC							NC
M	NC							NC

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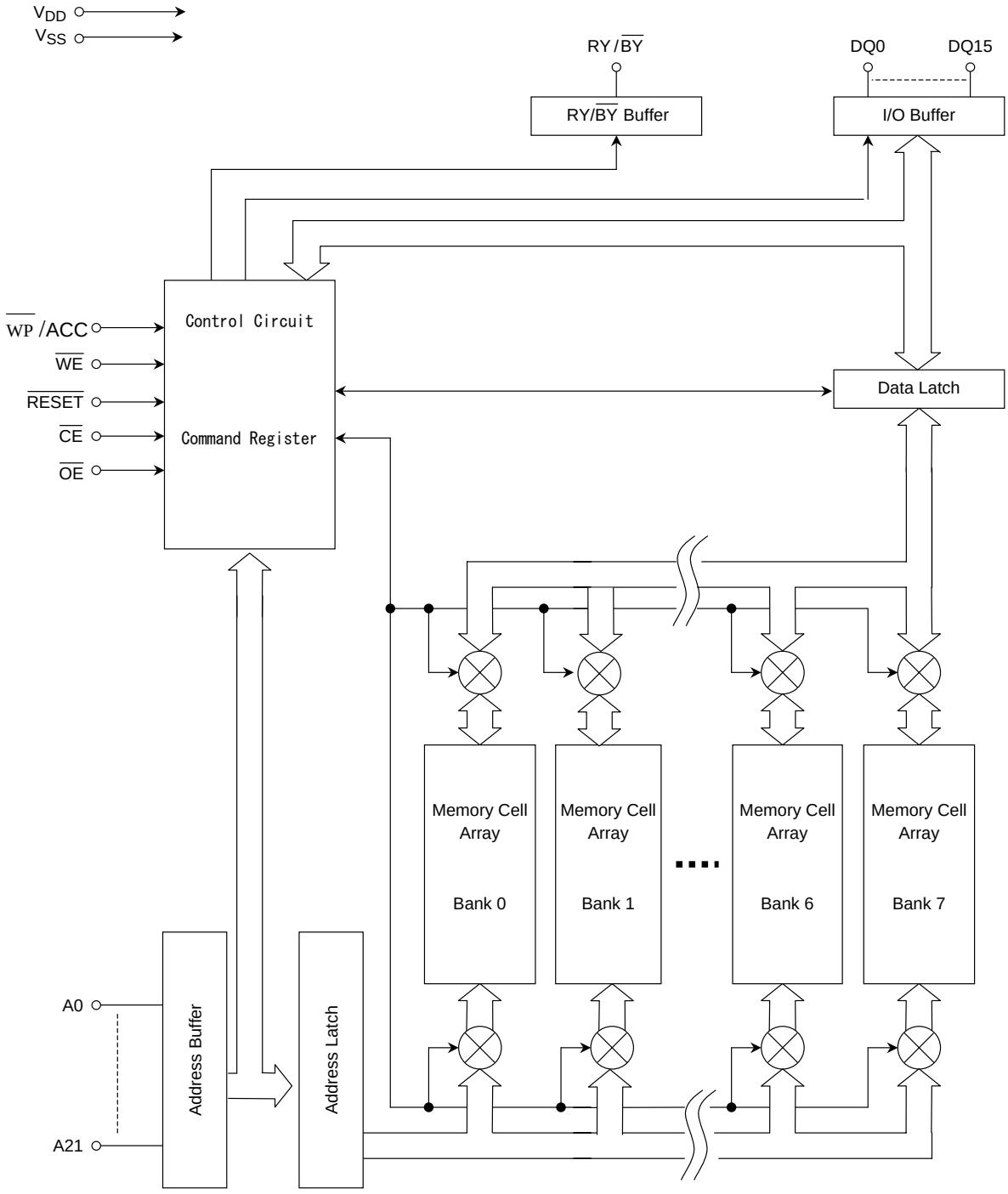
5. BLOCK DIAGRAM



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6. MODE SELECTION

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	A9	A6	A1	A0	$\overline{RESET}$	$\overline{WP}$/ACC	DQ0~DQ15
Read/Page Read	L	L	H	A9	A6	A1	A0	H	*	D_{OUT}
ID Read (Manufacturer Code)	L	L	H	V_{ID}	L	L	L	H	*	Code
ID Read (Device Code)	L	L	H	V_{ID}	L	L	H	H	*	Code
Standby	H	*	*	*	*	*	*	H	*	High-Z
Output Disable	*	H	H	*	*	*	*	*	*	High-Z
Write	L	H	(1) ⊓	A9	A6	A1	A0	H	*	D_{IN}
Block Protect 1	L	V_{ID}	(1) ⊓	V_{ID}	L	H	L	H	*	*
Block Protect 2	L	H	H	*	L	H	L	V_{ID}	*	*
Verify Block Protect	L	L	H	V_{ID}	L	H	L	H	*	Code
Temporary Block Unprotect	*	*	*	*	*	*	*	V_{ID}	*	*
Hardware Reset/Standby	*	*	*	*	*	*	*	L	*	High-Z
Boot Block Protect	*	*	*	*	*	*	*	*	L	*

Notes: * = V_{IH} or V_{IL}, L = V_{IL}, H = V_{IH}
(1) Pulse input

7. ID CODE TABLE

CODE TYPE		A21~A12	A6	A1	A0	CODE (HEX)
Manufacturer Code		X	L	L	L	0098h
Device Code	TC58FVM6T5B	X	L	L	H	002Dh
	TC58FVM6B5B	X	L	L	H	002Eh
Verify Block Protect		BA(1)	L	H	L	Data(2)

Notes : X: V_{IH} or V_{IL}
L: V_{IL} H: V_{IH}
(1) BA: Block Address
(2) 0001h-Protected Block
0000h- Unprotected Block

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8. COMMAND SEQUENCES

COMMAND SEQUENCE	BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Read/Reset	1	XXXh	F0h										
Read/Reset	3	555h	AAh	2AAh	55h	555h	F0h	RA(1)	RD(2)				
ID Read	3	555h	AAh	2AAh	55h	BK(3) + 555h	90h	IA(4)	ID(5)				
Auto Program	4	555h	AAh	2AAh	55h	555h	A0h	PA(6)	PD(7)				
Auto Page Program	11	555h	AAh	2AAh	55h	555h	E6h	PA(6)	PD(7)	PA(6)	PD(7)	PA(6)	PD(7)
Program Suspend	1	BK(3)	B0h										
Program Resume	1	BK(3)	30h										
Auto Chip Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	555h	10h
Auto Block Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA(8)	30h
Block Erase Suspend	1	BK(3)	B0h										
Block Erase Resume	1	BK(3)	30h										
Fast Program Set	3	555h	AAh	2AAh	55h	555h	20h						
Fast Program	2	XXXh	A0h	PA(6)	PD(7)								
Fast Program Reset	2	XXXh	90h	XXXh	F0h(9)								
Block Protect 2(10)	3	XXXh	60h	BPA(11)	60h	XXXh	40h	BPA(11)	BPD(12)				
Hidden ROM Mode Entry	3	555h	AAh	2AAh	55h	555h	88h						
Hidden ROM Program	4	555h	AAh	2AAh	55h	555h	A0h	PA(6)	PD(7)				
Hidden ROM Erase	6	555h	AAh	2AAh	55h	555h	80h	555h	AAh	2AAh	55h	BA(8)	30h
Hidden ROM Protect	5	555h	AAh	2AAh	55h	555h	60h	XX1Ah	68h	XX1Ah	48h	RA(1)	RD(2)
Hidden ROM Exit	4	555h	AAh	2AAh	55h	555h	90h	XXXh	00h				
CFI	1	BK(3) + 55h	98h	CA(13)	CD(14)								

Notes: The system should generate the following address patterns:
555h or 2AAh on address pins A10~A0.
DQ8~DQ15 are ignored.
X : V_{IH} or V_{IL} (0h-Fh)

(1) RA: Read Address
(2) RD: Read Data Output
(3) BK: Bank Address = A21~A19
(4) IA: Bank Address and ID Read Address (A6,A1,A0)
Bank Address = A21~A19
Manufacturer Code = (0,0,0)
Device Code = (0,0,1)
(5) ID: ID Code Output
(6) PA: Program Address Input
Input continuous 8 addresses from (A0, A1, A2) = (0, 0, 0) to (A0, A1, A2) = (1, 1, 1) in Page program.
(7) PD: Program Data Input
Input continuous 8 address from (A0, A1, A2) = (0, 0, 0) to (A0, A1, A2) = (1, 1, 1) in Page program.
(8) BA: Block Address = A21~A12
(9) F0h: 00h is valid too.
(10) Input VID to $\overline{RESET}$
(11) BPA: Block Address and ID Read Address (A6,A1,A0)
Block Address = A21~A12
ID Read Address = (0,1,0)
(12) BPD: Verify data Output
(13) CA: CFI Address
(14) CD: CFI Data Output

: Read Operations

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8. COMMAND SEQUENCES(continue)

COMMAND SEQUENCE	BUS WRITE CYCLES REQ'D	FIRST BUS WRITE CYCLE		SECOND BUS WRITE CYCLE		THIRD BUS WRITE CYCLE		FOURTH BUS WRITE CYCLE		FIFTH BUS WRITE CYCLE		SIXTH BUS WRITE CYCLE		SEVENTH BUS WRITE CYCLE	
		Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data	Addr.	Data
Password Program	4	555h	AAh	2AAh	55h	555h	38h	XX0h	PD0(1)						
		555h	AAh	2AAh	55h	555h	38h	XX1h	PD1(1)						
		555h	AAh	2AAh	55h	555h	38h	XX2h	PD2(1)						
		555h	AAh	2AAh	55h	555h	38h	XX3h	PD3(1)						
Password Unlock	7	555h	AAh	2AAh	55h	555h	28h	XX0h	PD0(1)	XX1h	PD1(1)	XX2h	PD2(1)	XX3h	PD3(1)
Password Verify	3	555h	AAh	2AAh	55h	555h	C8h	PWA(2)	PWD(3)						
Password Protection Mode Lock	5	555h	AAh	2AAh	55h	555h	60h	X0Ah	68h	X0Ah	48h	XXh	PD(0) (4)		
Non-Password Protection Mode Lock	5	555h	AAh	2AAh	55h	555h	60h	X12h	68h	X12h	48h	XXh	PD(0) (4)		
PPB Set	5	555h	AAh	2AAh	55h	555h	60h	BA(5)+ XX02h	68h	BA(5)+ XX02h	48h	XXh	PD(0) (4)		
ALL PPB Clear	5	555h	AAh	2AAh	55h	555h	60h	XX02h	60h	BA(5)+ XX02h	40h	XXh	PD(0) (4)		
Verify Block Protect	3	555h	AAh	2AAh	55h	BA(5) + 555h	90h	BA(5)+ XX02h	PD(0) (4)						
PPB Lock Set	3	555h	AAh	2AAh	55h	555h	78h								
PPB Lock Verify	3	555h	AAh	2AAh	55h	555h	58h	BA(5)	PD(1) (4)						
DPB Set	4	555h	AAh	2AAh	55h	555h	48h	BA(5)	X1h						
DPB Clear	4	555h	AAh	2AAh	55h	555h	48h	BA(5)	X0h						
DPB Verify	3	555h	AAh	2AAh	55h	555h	58h	BA(5)	PD(0) (4)						

Notes: The system should generate the following address patterns:
555h or 2AAh on address pins A10~A0.
DQ8~DQ15 are ignored.

X : V_{IH} or V_{IL} (0h-Fh)

(1) PD0 : 1st Password (Data of 1-16bit)
PD1 : 2nd Password (Data of 17-32bit)
PD2 : 3rd Password (Data of 33-48bit)
PD3 : 4th Password (Data of 49-64bit)

(2) PWA: Password Address Input

(3) PWD: Password Data Output

(4) PD(0): Data (1: Set/ 0: Reset) on DQ0.
PD(1): Data (1: Set/ 0: Reset) on DQ1.

(5) BA: Block Address = A21~A12

: Read Operations

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9. SIMULTANEOUS READ/WRITE OPERATION

The TC58FVM6(T/B)5B features a Simultaneous Read/Write operation. The Simultaneous Read/Write operation enables the device to simultaneously write data to or erase data from a bank while reading data from another bank.

The TC58FVM6(T/B)5B has a total of sixteen banks (8Mbits x 8 Banks). Banks can be switched by using the bank addresses (A21~A19). For a description of bank blocks and addresses, please refer to the Block Address Table and Block Size Table.

The Simultaneous Read/Write operation cannot perform multiple operations within a single bank. The table below shows the operation modes in which simultaneous operation can be performed.

Note that during Auto-Program execution or Auto Block Erase operation, the Simultaneous Read/Write operation cannot read data from addresses in the same bank which have not been selected for operation. Data from these addresses can be read using the Program Suspend or Erase Suspend function, however.

In order to perform simultaneous operation during automatic operation execution, when changing a bank, it is necessary to set $\overline{OE}$ to V_{IH}.

SIMULTANEOUS READ/WRITE OPERATION

STATUS OF BANK ON WHICH OPERATION IS BEING PERFORMED	STATUS OF OTHER BANKS
Read Mode	Read Mode
ID Read Mode(1)	
Auto-Program Mode	
Auto-Page Program Mode	
Fast Program Mode(2)	
Program Suspend Mode	
Auto Block Erase Mode	
Auto Multiple Block Erase Mode(3)	
Erase Suspend Mode	
Program during Erase Suspend	
Program Suspend during Erase Suspend	
CFI Mode	

(1) Only Command Mode is valid.
(2) Excluding times when Acceleration Mode is in use.
(3) If the selected blocks are spread across all eight banks, simultaneous operation cannot be carried out.

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10. OPERATION MODES

In addition to the Read, Write and Erase Modes, the TC58FVM6(T/B)5B features many functions including block protection and data polling. When incorporating the device into a design, please refer to the timing charts and flowcharts in combination with the descriptions below.

10.1. Read Mode

To read data from the memory cell array, set the device to Read Mode.

The device is automatically set to Read Mode immediately after power-on or on completion of an automatic operation. The Software Reset Command releases The ID Read Mode, releases the lock state when an automatic operation ends abnormally, and sets the device to Read Mode. Hardware Reset terminates operation of the device and resets it to Read Mode. When reading data without changing the address immediately after power-on, the host should input Hardware Reset or change $\overline{CE}$ from H to L.

10.2. ID Read Mode

ID Read Mode is used to read the device maker code and device code. The mode is useful in that it allows EPROM programmers to identify the device type automatically.

Access time in ID Read Mode is the same as that in Read Mode. For a list of the codes, please refer to the ID Code Table.

ID read can be executed in two ways, as follows:

(1) Applying V_{ID} to A9

Mainly EPROM programmers use this method. Applying V_{ID} to A9 sets the device to ID Read Mode, outputting the maker code from address 00h and the device code from address 01h. Releasing V_{ID} from A9 returns the device to Read Mode. With this method, all banks are set to ID Read Mode; thus, simultaneous operation cannot be performed.

(2) Input command sequence

With this method simultaneous operation can be performed. Inputting an ID Read command sets the specified bank to ID Read Mode. Banks are specified by inputting the bank address (BK) in the third Bus Write cycle of the Command cycle. To read an ID code, the bank address as well as the ID read address must be specified (with $\overline{WP}$/ACC = V_{IH} or V_{IL}). The maker code is output from address BK + 00; the device code is output from address BK + 01. From other banks, data is output from the memory cells. Inputting a Reset command releases ID Read Mode and returns the device to Read Mode.

10.3. Standby Mode

TC58FVM6(T/B)5B has two ways to put the device into Standby Mode. In Standby Mode, DQ is put into the High-Impedance state.

(1) Control using $\overline{CE}$ and $\overline{RESET}$

With the device in Read Mode, input V_{DD} ± 0.3 V to $\overline{CE}$ and $\overline{RESET}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow.

(2) Control using $\overline{RESET}$ only

With the device in Read Mode, input V_{SS} ± 0.3 V to $\overline{RESET}$. The device will enter Standby Mode and the current will be reduced to the standby current (I_{DDS1}). Even if the device is in the process of performing simultaneous operation, this method will terminate the current operation and set the device to Standby Mode. This is a hardware reset and is described later.

10.4. Auto-Sleep Mode

This function suppresses power dissipation during reading. If the address input does not change for 150 ns, the device will automatically enter Sleep Mode and the current will be reduced to the standby current (I_{DDS2}). However, if the device is in the process of performing simultaneous operation, the device will not enter Standby Mode but will instead cause the operating current to flow. Because the output data is latched, data is output in Sleep Mode. When the address is changed, Sleep Mode is automatically released, and data from the new address is output.

10.5. Output Disable Mode

Inputting V_{IH} to $\overline{OE}$ disables output from the device and sets DQ to High-Impedance.

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10.6. Command Write

The TC58FVM6(T/B)5B uses the standard JEDEC control commands for a single-power supply E²PROM. A Command of Write is executed by inputting the address and data into the Command Register. The command is written by inputting a pulse to $\overline{WE}$ with $\overline{CE}$ = V_{IL} and $\overline{OE}$ = V_{IH} ($\overline{WE}$ control). The command can also be written by inputting a pulse to $\overline{CE}$ with $\overline{WE}$ = V_{IL} ($\overline{CE}$ control). The address is latched on the falling edge of either $\overline{WE}$ or $\overline{CE}$. The data is latched on the rising edge of either $\overline{WE}$ or $\overline{CE}$. DQ0~DQ7 are valid for data input and DQ8~DQ15 are ignored.

To abort input of the command sequence uses the Reset command. The device will reset the Command Register and enter Read Mode. If an undefined command is input, the Command Register will be reset and the device will enter Read Mode.

10.7. Software Reset: Read/Reset Command

Initiate the software reset by inputting a Read/Reset command. The software reset returns the device from ID Read Mode or CFI Mode to Read Mode, releases the lock state if automatic operation has ended abnormally, and clears the Command Register.

10.8. Hardware Reset

A hardware reset initializes the device and sets it to Read Mode. When a pulse is input to $\overline{RESET}$ for t_{RP}, the device abandons the operation which is in progress and enters the Read Mode after t_{READY}. Note that if a hardware reset is applied during data overwriting, such as a Write or Erase operation, data at the address or block being written to at the time of the reset will become undefined.

After a hardware reset, the device enters Read Mode if $\overline{RESET}$ = V_{IH} or Standby Mode if $\overline{RESET}$ = V_{IL}. The DQ pins are High-Impedance when $\overline{RESET}$ = V_{IL}. After the device has entered Read Mode, Read operations and input of any command are allowed.

10.9. Comparison between Software Reset and Hardware Reset

ACTION	SOFTWARE RESET	HARDWARE RESET
Releases ID Read Mode or CFI Mode.	True	True
Clears the Command Register.	True	True
Releases the lock state if automatic operation has ended abnormally.	True	True
Stops any automatic operation which is in progress.	False	True
Stops any operation other than the above and returns the device to Read Mode.	False	True

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10.10. Auto-Program Mode

The TC58FVM6(T/B)5B can be programmed in word units. Auto-Program Mode is set using the Program command. The program address and program data is latched in the fourth Bus Write cycle. Auto programming starts on the rising edge of the $\overline{WE}$ signal in the fourth Bus Write cycle. The Program and Program Verify commands are automatically executed by the chip. The device status during programming is indicated by the Hardware Sequence flag. To read the Hardware Sequence flag, specify the address to which the Write is being performed.

During Auto Program execution, a command sequence for the bank on which execution is being performed cannot be accepted. To terminate execution, use a hardware reset. Note that if the Auto-Program operation is terminated in this manner, the data written so far is invalid.

Any attempt to program a protected block is ignored. In this case, the device enters Read Mode 3 μs after a latch of program data in the fourth Bus Write cycle.

If an Auto-Program operation fails, the device remains in the programming state and does not automatically return to Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure. If a programming operation fails, the device should not be used. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks.

The device allows 0s to be programmed into memory cells which contain a 1. 1s cannot be programmed into cells which contain 0s. If this is attempted, execution of Auto Program will fail. This is a user error, not a device error. A cell containing 0 must be erased in order to set it to 1.

10.11. Auto-Page Program Mode

Auto-Page Program is a function which enables simultaneously Programming or 8words of data.
In this mode, the Programming time for 64M bit is less than 60% compared with the Auto program mode. In word mode, input the page program command during first bus write cycle to third bus writes cycle. Input program data and address of (A0, A1, A2) = (0, 0, 0) in the forth bus write cycle. Input increment address and program data during the fifth bus write cycle to the eleventh bus write cycle. After input of the eleventh bus write cycle, page program operation starts.

10.12. Fast Program Mode

Fast Program is a function which enables execution of the command sequence for the Auto Program to be completed in two cycles. In this mode the first two cycles of the command sequence, which normally requires four cycles, are omitted. Writing is performed in the remaining two cycles. To execute Fast Program, input the Fast Program command. Writes in this mode uses the Fast Program command but operation is the same at that for ordinary Auto-Program. The status of the device is indicated by the Hardware Sequence flag and read operations can be performed as usual. To exit this mode, the Fast Program Reset command must be input. When the command is input, the device will return to Read Mode.

10.13. Acceleration Mode

The TC58FVM6(T/B)5B features an Acceleration Mode that allows write time to be reduced. Applying V_{ACC} pin to $\overline{WP}$/ACC automatically sets the device to Acceleration Mode. In Acceleration Mode, Block Protect Mode changes to Temporary Block Unprotect Mode. Write Mode changes to Fast Program Mode. Modes are switched by the $\overline{WP}$/ACC signal; thus, there is no need for a Temporary Block Unprotect operation or to set or reset Fast Program Mode. Operation of Write is the same as in Auto-Program Mode. Removing V_{ACC} from $\overline{WP}$/ACC terminates Acceleration Mode.

This function can perform only Auto Program Mode and Auto Page Program Mode. ID Read or other commands cannot be done.

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10.14. Program Suspend/Resume Mode

Program Suspend is used to enable Data Read by suspending the Write operation. The device accepts a Program Suspend command in Write Mode (including Write operations performed during Erase Suspend) but ignores the command in other modes. When the command is input, the address of the bank on which Write is being performed must be specified. In Program Suspend Mode, it is invalid except a Read command, a ID Read command, a CFI command, and a Resume command. After input of the command, the device will enter Program Suspend Read Mode after t_{SUSP}.

During Program Suspend, Cell Data Read, ID Read and CFI Data Read can be performed. When Data Write is suspended, the address to which Write was being performed becomes undefined. ID Read and CFI Data Read are the same as usual.

After completion of Program Suspend, input a Program Resume command to return to Write Mode. When inputting the command, specify the address of the bank on which Write is being performed. If the ID Read or CFI Data Read function is being used, abort the function before inputting the Resume command. On receiving the Resume command, the device returns to Write Mode and resumes outputting the Hardware Sequence flag for the bank to which data is being written.

Program Suspend can be run in Fast Program Mode or Acceleration Mode. However, note that when running Program Suspend in Acceleration Mode, V_{ACC} must not be released.

10.15. Auto Chip Erase Mode

The Auto Chip Erase Mode is set using the Chip Erase command. An Auto Chip Erase operation starts on the latch of the command in the sixth bus cycle. All memory cells are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the Hardware Sequence flag.

Command input is ignored during an Auto Chip Erase. A hardware reset can interrupt an Auto Chip Erase operation. If an Auto Chip Erase operation is interrupted, it cannot be completed correctly. Hence, an additional Erase operation must be performed.

Any attempt to erase a protected block is ignored. If all blocks are protected, the Auto Erase operation will not be executed and the device will enter Read mode 400 μs after the latch of command in the sixth bus cycle.

If an Auto Chip Erase operation fails, the device will remain in the erasing state and will not return to the Read Mode. The device status is indicated by the Hardware Sequence flag. Either a Reset command or a hardware reset is required to return the device to Read Mode after a failure.

In this case, it cannot be ascertained which block the failure occurred in. Either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed blocks, and stop using them. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks

10.16. Auto Block Erase/Auto Multi-Block Erase Modes

The Auto Block Erase Mode and Auto Multi-Block Erase Mode are set using the Block Erase command. The block address is latched in the sixth bus cycle. The auto block erase starts as soon as the Erase Hold Time (t_{BEH}) has elapsed after the latch of the command. When multiple blocks are erased, the sixth Bus Write cycle is repeated with each block address and Auto Block Erase command being input within the Erase Hold Time (this constitutes an Auto Multi-Block Erase operation). If a command other than an Auto Block Erase command or Erase Suspend command is input during the Erase Hold Time, the device will reset the Command Register and enter Read Mode. The Erase Hold Time restarts on each successive command latch. Once operation starts, all memory cells in the selected block are automatically preprogrammed to 0, erased and verified as erased by the chip. The device status is indicated by the setting of the Hardware Sequence flag. When the Hardware Sequence flag is read, the addresses of the blocks on which auto-erase operation is being performed must be specified. If the selected blocks are spread across all 8 banks, simultaneous operation cannot be carried out.

All commands (except Erase Suspend) are ignored during an Auto Block Erase or Auto Multi-Block Erase operation. Either operation can be aborted using a Hardware Reset. If an auto-erase operation is interrupted, it cannot be completed correctly; therefore, a further erase operation is necessary to complete the erasing.

Any attempt to erase a protected block is ignored. If all the selected blocks are protected, the auto-erase operation is not executed and the device returns to Read Mode 400 μs after the latch of command in the last bus cycle.

If an auto-erase operation fails, the device remains in the Erasing state and does not return to Read Mode. The device status is indicated by the Hardware Sequence flag. After a failure, either a Reset command or a Hardware Reset is required to return the device to Read Mode. If multiple blocks are selected, it will not be possible to ascertain the block in which the failure occurred. In this case either abandon use of the device altogether, or perform a Block Erase on each block, identify the failed blocks, and stop using them. To build a more reliable system, the host processor should take measures to prevent subsequent use of failed blocks.

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10.17. Erase Suspend/Erase Resume Modes

Erase Suspend Mode suspends Auto Block Erase and reads data from or writes data to an unselected block. The Erase Suspend command is allowed during an auto block erase operation but is ignored in all other oreration modes. When the command is input, the address of the bank on which Erase is being performed must be specified.

In Erase Suspend Mode, it is invalid except a Read command, a ID Read command, a CFI command, a Program command, and a Resume command. If an Erase Suspend command is input during an Auto Block Erase, the device will enter Erase Suspend Read Mode after t_{SUSE}. The device status (Erase Suspend Read Mode) can be verified by checking the Hardware Sequence flag. If data is read consecutively from the block selected for Auto Block Erase, the DQ2 output will toggle and the DQ6 output will stop toggling and RY/$\overline{BY}$ will be set to High-Impedance.

Inputting a Write command during an Erase Suspend enables a Write to be performed to a block which has not been selected for the Auto Block Erase. Data is written in the usual manner.

To resume the Auto Block Erase, input an Erase Resume command. On input of the command, the address of the bank on which the Write was being performed must be specified. On receiving an Erase Resume command, the device returns to the state it was in when the Erase Suspend command was input. If an Erase Suspend command is input during the Erase Hold Time, the device will return to the state it was in at the start of the Erase Hold Time. At this time more blocks can be specified for erasing. If an Erase Resume command is input during an Auto Block Erase, Erase resumes. At this time toggle output of DQ6 resumes and 0 is output on RY/$\overline{BY}$.

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10.18. Block Protection

TC58FVM6(T/B)5B has Block Protection that is a function for disabling writing and erasing specific blocks. Block Protection features several level of Block Protection.

(1) Write Protect ($\overline{WP}$/ACC pin) [Hardware Protection]

The TC58FVM6(T/B)5B has Hardware Block protection feature by $\overline{WP}$/ACC =V_{IL}. The TC58FVM6T5B protects BA133 and BA134 with $\overline{WP}$/ACC =V_{IL}. TC58FVM6B5B protects BA0 and BA1 with $\overline{WP}$/ACC =V_{IL}. This mode is released with $\overline{WP}$/ACC =V_{IH}. When the device is programming operation or erasing operation, $\overline{WP}$/ACC pin has to fix to V_{IH} or V_{IL}.

(2) Block protection 1 Persistent Protection Bit (PPB) [V_{ID} Protection]

Specify a device block address and make the following signal settings A9= $\overline{OE}$ =V_{ID}, A1 = V_{IH} and $\overline{CE}$ = A0 = A6 = V_{IL}. Now when a pulse is input to $\overline{WE}$ for t_{PPLH}, the device will start to write to the block protection circuit. Block protection can be verified using the Verify Block Protect command. Inputting V_{IL} on $\overline{OE}$ sets the device to Verify Mode. 01h is output if the block is protected and 00h is output if the block is unprotected. If block protection was unsuccessful, the operation must be repeated. Releasing V_{ID} from A9 and $\overline{OE}$ terminates this mode.

When the device state is Password Protection Mode, the hosts have to execute the Password Unlock command before performing this protection command.

(3) Block protection 2 Persistent Protection Bit (PPB) [V_{ID} Protection]

Inputting the Block Protect 2 command with $\overline{RESET}$ =V_{ID} also performs block protection. The first cycle of the command sequence is the Set-up command. In the second cycle, the Block Protect command is input, in which a block address and A1 = V_{IH} and A0 = A6 = V_{IL} are input. Now the device writes to the block protection circuit. There is a wait of t_{PPLH} until this write is completed; however, no intervention is necessary during this time. In the third cycle the Verify Block Protect command is input. This command verifies the write to the block protection circuit. Read is performed in the fourth cycle. If the protection operation is complete, 01h is output. If a value other than 01h is output, block protection is not complete and the Block Protect command must be input again. Removing the V_{ID} input from $\overline{RESET}$, exits this mode.

When the device state is Password Protection Mode, the hosts have to execute the Password Unlock command before performing this protection command.

(4) Block Protection 3 Persistent Protection Bit(PPB) [Software Protection]

This feature is the block protection without V_{ID}. By using Persistent Protection Bit, protection can be set to each block. The PPBs retains the state across power cycle. Each PPB can be individually modifiable through the PPB Set command. All PPB can be cleared by the PPB Clear Command at a time. The PPB Verify command to the device can check the PPB status.

The 5th and 6th write bus cycle of the PPB Set are PPB Verify cycle. When completely finish the PPB Set, the device outputs '1' on DQ0 at the sixth bus write cycle. When device outputs '0' on DQ0, the PPB Set is not complete, then the hosts must retry from fourth bus write cycle. Similarly, when completely finish the PPB Clear, the device outputs '0' on DQ0 at the sixth bus write cycle. When the device outputs '1' on DQ1, the PPB Clear is not complete, then the hosts must retry from fourth bus write cycle.

When PPB is locked by the PPB Lock Set command, PPB is disabled for PPB Set and PPB Clear Operation. The PPB Lock Verify command can check the PPB Lock status on the DQ1 ('1' is Set state and '0' is Clear state). Behaviors of PPB Lock differ between password protection mode and non-password protection mode.

At the time of the finishing PPB Set, PPB Clear, PPB Lock Set and PPB Lock Verify, the hosts have to inputting the Hidden ROM Exit command.

At the time of shipment, the PPBs and PPB Lock are settled to "0".

(5) Block Protection 4 Dynamic Protection Bit (DPB) [Software Protection]

This feature is the block protection without V_{ID}. By using Dynamic Protection Bit, protection can be set to each block. After power-up or hardware reset cycle, all DPB are settled to "0" as clear. Each DPB can be individually modifiable through the DPB Set command and DPP Clear command.

The Writing of the DPB Verify command to the device can check the Set or Clear of the DPB status. When completely finish the DPB Set, device will be outputting '1' on DQ0 at the fourth bus write cycle in the DPB verify. When Device is outputting '0' on DQ0, the DPB Set is not complete, then the hosts must retry from the DPB set command. Similarly, when completely finish the DPB Clear, the device will be outputting '0' on DQ0 at the fourth bus write cycle in the DPB verify. When the device is outputting '1' on DQ0, the DPB Clear is not complete, then the user must retry from the DPB clear command. At the time of the finishing DPB Set, DPB Clear, and DPB Verify, the hosts have to inputting the Hidden ROM Exit command.

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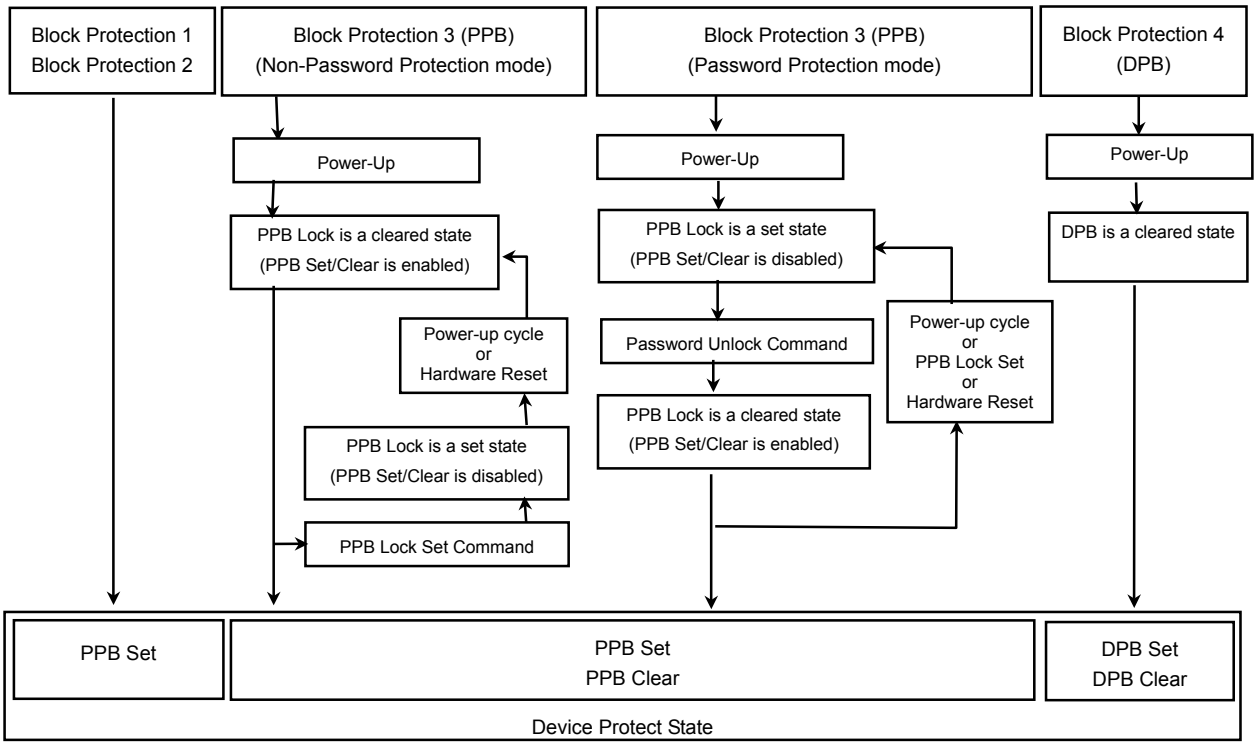
10.18.1 Relationship of the Each Block Protection



* A program of one of PPB and the DPB protects an object block.

10.18.2. Block Protection Matrix

Hardware Protection		Software Protection		Block Protect Status	
$\overline{WP}$/ACC	$\overline{RESET}$	PPB	DPB	Two Boot Block	Other Block
L	H	Clear	Clear	Protected	Unprotected
		Set	X		Protected
		X	Set		
	VID	X	X		Unprotected
H	H	Clear	Clear	Unprotected	Unprotected
		Set	X	Protected	Protected
		X	Set		
	VID	X	X	Unprotected	Unprotected

Notes X: H or L, Set state or Clear state

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10.18.3. Non-Password Protection Mode and Password Protection Mode

At Block Protection 3, there are two Protection Mode of Non-Password Protection Mode and Password Protection Mode. Operation of a PPB lock differs in each mode. The hosts need to choose either Non-Password Protection Mode or Password Protection Mode before using of this device.

Non-Password Protection Mode Lock Command sets the device to Non-Password Protection Mode. Password Protection Mode Lock Command sets the device to Password Protection Mode. The respective program command can be executed only once, and Mode Lock Erase is impossible. At the shipment, the Non-Password Protection Mode and the Password Protection Mode aren't set state. In the case of using Non-Password Protection Mode, the hosts have to execute a Non-Password Protection Mode Lock in order to prevent the device from being changed to Password Protection Mode. In the case of using Password Protection Mode, the hosts have to execute a Password Protection Mode Lock. Once a Protection Mode is set, it is not eternally changeable.

After latching the fourth bus write cycle command of " 68h", the hosts have to wait 100us. The 5th and 6th write bus cycles are Protection Mode Verify command. When the Protection Mode Lock (Set) is completely finished, the device will output '1' on DQ0 at the sixth bus write cycle. When the device is outputting '0' on DQ0, the Protection Mode Lock (Set) is not complete, then the hosts must retry from fourth bus write cycle.

When the Protection Mode Lock (Set) is finished, the hosts have to execute the Hidden ROM Exit command.

Non-Password Protection Mode Lock	Password Protection Mode Lock	Device Status
0	0	Non-Password Protection Mode (At Shipment)
Programmed ("1")	0	Non-Password Protection Mode
0	Programmed ("1")	Password Protection Mode
Programmed ("1")	Programmed ("1")	Inhibit

10.18.4. PPB Lock in Non-Password Protection Mode and Password Protection Mode

In the case of Non-Password Protection Mode, the PPB Lock is cleared by power-up cycle and Hardware Reset. When PPB Lock is set, the PPBs are disabled for modification by Block Protection 3. After Power-up cycle and Hardware Reset again, PPB Lock becomes '0' as clear. In Non-Password Protection Mode, Password Unlock command is ignored.

In the case of Password Protection Mode, the PPB Lock is set by power-up cycle and Hardware Reset. Once Password Protection Mode is set, PPB is disabled for modification by PPB Set and Clear without the Password Unlock command. The state of PPB Lock doesn't differ before and after Password Protection Mode Lock Command. PPB Lock is set again by power-up cycle, Hardware Reset, or PPB lock Set. In Password Protection Mode, Password Program command and Password Verify command is permanently ignored. Therefore, when the user chooses the Password Protection Mode, it is necessary to program a 64-bit password to this device before performing a password protection mode lock command. After Password program command, the user has to check by Password Verify command whether the desired Password is certainly programmed. Once Password Protection Mode was set, the user cannot check the Password. At modifying PPB, the user has to use the Password Unlock command with a 64-bit password. Please set a Password certainly.

PPB Lock Status of the Non-Password Protection Mode and the Password Protection Mode

	Non-Password Protection Mode	Password Protection Mode
After Power-up cycle and Hardware Reset	PPB Lock is '0' (clear)	PPB Lock is '1' (set)

PPB Lock Status change method of the each Protection Mode

	Non-Password Protection Mode	Password Protection Mode
PPB Lock Set	PPB Lock Set	PPB Set Command Power-up cycle Hardware Reset
PPB Lock Clear	Power-up cycle Hardware Reset	Password Unlock Command

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10.18.5. Description of Password Protection Command

(1) Password Program Command

The Password Protect Command permits programming the password that is used as part of the Hardware Protection scheme. The actual Password length is 64-bits. The 64-bits password is split to four of 16-bits Password Program. In Password Protection Mode, Password Program and Password verify are disabled. During programming the Password, Simultaneous Operation is disabled. Read operations to any memory location is available after completion of the password programming. The status of password program operation can be checked by hardware sequence flags. When this mode is finished, the hosts have to execute the Hidden ROM Exit command. Password is set as four words of "FFFFh" at the time of shipment.

The Hardware Sequence Flags of the Password Program

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	RY/$\overline{BY}$
In Progress	0	Toggle	0	0	0	1	0	0	0
Program Complete	1	1	0	0	0	1	0	0	High-Z
Program Failed	0	Toggle	1	0	0	1	0	0	0

(2) Password Verify Command

The Password Verify Command is verify the Password. Verification of a Password can be performed when the Password Protection Mode Lock is not programmed. In Password Protection Mode, if the user attempts to verify the Password, the device output "FFFFh". The hosts have to execute the Hidden ROM Entry command before Password Verify. During verification the Password, Simultaneous Operation is disabled. At the forth bus write cycle of Password Verify Command, the hosts have to fix the two address bits (A1, A0). When this mode is finished, the hosts have to execute the Hidden ROM Exit command.

(3) Password Unlock Command

The Password Unlock Command clears the PPB Lock Bit when the user sets the Password Protection Mode. In order to perform Password Unlock command, the exact Password is necessary. It is necessary to input password unlock command at intervals of 2us or more. If the interval is shorter than 2us, the command is ignored.

At Password Unlock Command the 64-bits password is input in four step at 4th, 5th, 6th, 7th write bus cycles. The address A1:A0 is 0:0 at 4th write bus cycle, A1:A0 is 0:1 at 5th write bus cycle, A1:A0 is 1:0 at 6th write bus cycle, and finally A1:A0 is 1:1 at 7th write bus cycle. A wrong Password input at the Password Unlock sequence causes mismatch of Password and PPB Lock Bit is not changed.

When the Password Unlock Command is entered, the RY/$\overline{BY}$ pin is Low, which is indicating the device is busy. The status of password unlock operation can be checked by hardware sequence flags. Then flags are output by specifying the address of Bank0 (Bottom Boot Block) or Bank7 (Top Boot Block). Inputting address of the other Bank then, actual cell array data is output. The hardware sequence flags indicate whether exact password is inputted at 4-6th write bus cycles by intervals of 2us or more. During inputting password at 4-7th write bus cycles, DQ6 is toggling. When the first Password Unlock is successful, RY/$\overline{BY}$ pin is LOW and DQ6 stop toggling. Then user can input next password. When the Password Unlock Command operation completes, the user has to perform Hidden ROM Exit command. PPB Lock Bit should be read in order to check whether Password Unlock has completed successfully.

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Status Flags of progressing the Password Unlock Command

	DQ7	DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0	RY/$\overline{BY}$
PWD Unlock in Progress	0	Toggle	0	0	0	1	0	0	0
Finished Input PWD (1)	0(2)	1	0	0	0	1	0	0	0
Finished Input PWD (1)	1(3)	1	0	0	0	1	0	0	High-Z
Finished Input PWD (4)	Array Data								High-Z

Notes:

（1） Specified BA within Bank-0 (Bottom Boot Block Device)/ Bank-7 (Top Boot Block Device)
（2） After inputting PWD at the 4th ,5th and 6th bus write cycles, DQ7 is “0”
（3） After inputting PWD at the 7th bus write cycle, DQ7 is “1”
（4） Specified BA without Bank-0 (Bottom Boot Block Device)/ Bank-7 (Top Boot Block Device)

10.18.6. Temporary Block Unprotection

The TC58FVM6(T/B)5B has a temporary block unprotection feature which disables block protection for all protected blocks. Unprotection is enabled by applying V_{ID} to the $\overline{RESET}$ pin. Now Write and Erase operations can be performed on all blocks except the boot blocks which have been protected by the Boot Block Protect operation. The device returns to its previous state when V_{ID} is removed from the $\overline{RESET}$ pin. That is, previously protected blocks will be protected again.

10.18.7. Verify Block Protect

The Verify Block Protect command is used to ascertain whether a block is protected or unprotected. Verification is performed either by inputting the Verify Block Protect command or by applying V_{ID} to the A9 pin**.** The Verify Block Protect command, which can be performed simultaneously with operations in another bank, is performed by setting the block address with A0 = A6 = V_{IL} and A1 = V_{IH}. If the block is protected, 01h is output. If the block is unprotected, 00h is output. The status depends on PPB, DPB, $\overline{WP}$/ACC and $\overline{RESET}$ state.

Inputting the verify block protect command sequence sets the specified bank to the Verify Block Protect mode. Inputting a Reset command releases this mode and returns the device to Read Mode. When verifying block protect across a bank boundary, a Reset command is needed at the time of the change of a bank

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10.19. Hidden ROM Area

The TC58FVM6(T/B)5B features a 64-Kbyte hidden ROM area, which is separate from the memory cells. The area consists of one block. Data Read, Write and Protect can be performed on this block. Because Protect cannot be released, once the block is protected, data in the block cannot be overwritten.

The hidden ROM area is located in the address space indicated in the HIDDEN ROM AREA ADDRESS TABLE. To access the Hidden ROM area, input a Hidden ROM Mode Entry command. The device now enters Hidden ROM Mode, allowing Read, Write, Erase and Block Protect to be executed. Write and Erase operations are the same as auto operations except that the device is in Hidden ROM Mode.

To protect the hidden ROM area, use the Block Protection 1 function or the Block Protection 2 function. The operation of Block Protect 2 here is the same as a normal Block Protect except that V_{IH} rather than V_{ID} is input to $\overline{RESET}$. When the PPB Lock has been settled, Hidden ROM protect state cannot be changed by the Block Protection 1 function or the Block Protection 2 function. The hosts have to decide the protection state of Hidden ROM Area before the PPB Lock has been settled. Once the block has been protected, protection cannot be released, even using the temporary block unprotection function. Using Block Protection for Hidden ROM Area must be careful.

Note that in Hidden ROM Mode, simultaneous operation cannot be performed for BANK7 in top boot type and for BANK0 in bottom boot type.

To exit Hidden ROM Mode, use the Hidden ROM Mode Exit command. This will return the device to Read Mode.

HIDDEN ROM AREA ADDRESS TABLE

TYPE	BOOT BLOCK ARCHITECTURE	ADDRESS RANGE	SIZE
TC58FVM6T5B	TOP BOOT BLOCK	3F8000h~3FFFFFh	32 Kwords
TC58FVM6B5B	BOTTOM BOOT BLOCK	000000h~007FFFh	32 Kwords

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10.20. CFI (Common Flash memory Interface)

The TC58FVM6(T/B)5B conforms to the CFI specifications. To read information from the device, input the Query command followed by the address. In Word Mode DQ8~DQ15 all output 0s. To exit this mode, input the Reset command.

CFI CODE TABLE 1 (Continue)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
10h 11h 12h	0051h 0052h 0059h	ASCII string “QRY”
13h 14h	0002h 0000h	Primary OEM command set 2: AMD/FJ standard type
15h 16h	0040h 0000h	Address for primary extended table
17h 18h	0000h 0000h	Alternate OEM command set 0: none exists
19h 1Ah	0000h 0000h	Address for alternate OEM extended table
1Bh	0023h	V_{DD} (min) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1Ch	0036h	V_{DD} (max) (Write/Erase) DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
1Dh	0000h	V_{PP} (min) voltage
1Eh	0000h	V_{PP} (max) voltage
1Fh	0004h	Typical time-out per single word write (2^N μs)
20h	0000h	Typical time-out for minimum size buffer write (2^N μs)
21h	000Ah	Typical time-out per individual block erase (2^N ms)
22h	0000h	Typical time-out for full chip erase (2^N ms)
23h	0005h	Maximum time-out for word write (2^N times typical)
24h	0006h	Maximum time-out for buffer write (2^N times typical)
25h	0004h	Maximum time-out per individual block erase (2^N times typical)
26h	0000h	Maximum time-out for full chip erase (2^N times typical)
27h	0017h	Device Size (2^N byte) 17h:64Mbit
28h 29h	0001h 0000h	Flash device interface description 1: x 16
2Ah 2Bh	0004h 0000h	Maximum number of bytes in multi-byte write (2^N)

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CFI CODE TABLE 2(Sequel)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
2Ch	0002h	Number of erase block regions within device
2Dh 2Eh 2Fh 30h	0007h 0000h 0020h 0000h	Erase Block Region 1 information Bits 0~15: y = block number Bits 16~31: z = block size (z × 256 bytes)
31h 32h 33h 34h	00FEh 0000h 0000h 0001h	Erase Block Region 2 information
40h 41h 42h	0050h 0052h 0049h	ASCII string “PRI”
43h	0031h	Major version number, ASCII
44h	0031h	Minor version number, ASCII
45h	0000h	Address-Sensitive Unlock 0: Required 1: Not required
46h	0002h	Erase Suspend 0: Not supported 1: For Read-only 2: For Read & Write
47h	0001h	Block Protect 0: Not supported X: Number of blocks per group
48h	0001h	Block Temporary Unprotect 0: Not supported 1: Supported
49h	0007h	Block Protect/Unprotect scheme
4Ah	0001h	Simultaneous operation 0: Not supported 1: Supported
4Bh	0000h	Burst Mode 0: Not supported
4Ch	0001h	Page Mode 0: Not supported 1: Supported
4Dh	0085h	V_{ACC} (min) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
4Eh	00C6h	V_{ACC} (max) voltage DQ7~DQ4: 1 V DQ3~DQ0: 100 mV
4Fh	000xh	Top/Bottom Boot Block Flag X = 2: Bottom Boot Block: TC58FVM6B5B X = 3: Top Boot Block: TC58FVM6T5B
50h	0001h	Program Suspend 0: Not supported 1: Supported

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CFI CODE TABLE 3(Sequel)

ADDRESS A6~A0	DATA DQ15~DQ0	DESCRIPTION
57h	0010h	Bank Organization 00h: Data at 4Ah is zero X: Number of Banks
58h	00XXh	Bank0 Region information XX: Number of blocks Bank0 TOP : 10h BOTTOM:17h
59h	0010h	Bank1 Region information Number of blocks Bank1 n=16
5Ah	0010h	Bank2 Region information Number of blocks Bank2 n=16
5Bh	0010h	Bank3 Region information Number of blocks Bank3 n=16
5Ch	0010h	Bank4 Region information Number of blocks Bank4 n=16
5Dh	0010h	Bank5 Region information Number of blocks Bank5 n=16
5Eh	0010h	Bank6 Region information Number of blocks Bank6 n=16
5Fh	00XXh	Bank7 Region information XX: Number of blocks Bank7 TOP : 17h BOTTOM:10h

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10.21. HARDWARE SEQUENCE FLAGS

The TC58FVM6(T/B)5B has a Hardware Sequence flag which allows the device status to be determined during an auto mode operation. The output data is read out using the same timing as that used when $\overline{CE}$ = $\overline{OE}$ = V_{IL} in Read Mode. The RY/$\overline{BY}$ output can be either High or Low.

The device re-enters Read Mode automatically after an auto mode operation has been completed successfully. The Hardware Sequence flag is read to determine the device status and the result of the operation is verified by comparing the read-out data with the original data.

STATUS				DQ7	DQ6	DQ5	DQ3	DQ2	RY/$\overline{BY}$
In Progress	Auto Programming/Auto Page Programming			$\overline{DQ7}$ (4)	Toggle	0	0	1	0
	Read in Program Suspend(1)			Data	Data	Data	Data	Data	High-Z
	In Auto Erase	Erase Hold Time	Selected(2)	0	Toggle	0	0	Toggle	0
			Not-selected(3)	0	Toggle	0	0	1	0
		Auto Erase	Selected	0	Toggle	0	1	Toggle	0
			Not-selected	0	Toggle	0	1	1	0
	In Erase Suspend	Read	Selected	1	1	0	0	Toggle	High-Z
			Not-selected	Data	Data	Data	Data	Data	High-Z
		Programming	Selected	$\overline{DQ7}$	Toggle	0	0	Toggle	0
			Not-selected	$\overline{DQ7}$	Toggle	0	0	1	0
Time Limit Exceeded	Auto Programming/Auto Page Programming			$\overline{DQ7}$ (4)	Toggle	1	0	1	0
	Auto Erase			0	Toggle	1	1	N/A	0
	Programming in Erase Suspend			$\overline{DQ7}$	Toggle	1	0	N/A	0

Notes:DQ outputs cell data and RY/$\overline{BY}$ goes High-Impedence when the operation has been completed.
DQ0 and DQ1 pins are reserved for future use. 0 is output on DQ0, DQ1 and DQ4.

(1) Data output from an address to which Write is being performed is undefined.
(2) Output when the block address selected for Auto Block Erase is specified and data is read from there.
(3) Output when a block address not selected for Auto Block Erase of same bank as selected block is specified and data is read from there. During Auto Chip Erase, all blocks are selected.
(4) In case of Page program operation is program data of (A0, A1, A2) = (1, 1, 1) in eleventh bus write cycle.

10.21.1. DQ7 ($\overline{DATA}$ polling)

During an Auto-Program or auto-erase operation, the device status can be determined using the data polling function. $\overline{DATA}$ polling begins on the rising edge of $\overline{WE}$ in the last bus cycle. In an Auto-Program operation, DQ7 outputs inverted data during the programming operation and outputs actual data after programming has finished. In an auto-erase operation, DQ7 outputs 0 during the Erase operation and outputs 1 when the Erase operation has finished. If an Auto-Program or auto-erase operation fails, DQ7 simply outputs the data.
When the operation has finished, the address latch is reset. Data polling is asynchronous with the $\overline{OE}$ signal.

10.21.2. DQ6 (Toggle bit 1)

The device status can be determined by the Toggle Bit function during an Auto-Program or auto-erase operation. The Toggle bit begins toggling on the rising edge of $\overline{WE}$ in the last bus cycle. DQ6 alternately outputs a 0 or a 1 for each $\overline{OE}$ access while $\overline{CE}$ = V_{IL} while the device is busy. When the internal operation has been completed, toggling stops and valid memory cell data can be read by subsequent reading. If the operation fails, the DQ6 output toggles.
If an attempt is made to execute an Auto Program operation on a protected block, DQ6 will toggle for around 3 μs. It will then stop toggling. If an attempt is made to execute an auto erase operation on a protected block, DQ6 will toggle for around 400 μs. It will then stop toggling. After toggling has stopped the device will return to Read Mode.

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10.21.3. DQ5 (internal time-out)

If an Auto-Program or auto-erase operates normally, DQ5 outputs a 0. If the internal timer times out during a Program or Erase operation, DQ5 outputs a 1. This indicates that the operation has not been completed within the allotted time.
Any attempt to program a 1 into a cell containing a 0 will fail (see Auto-Program Mode). In this case, DQ5 outputs a 1. In this case, DQ5 doesn't indicate defective device but mistaken usage.
After an Auto-Program or auto-erase operation ends normally, the device outputs actual cell array data. Therefor only with the data of DQ5 can't specify whether cell array data or hardware sequence flag. The hosts shuold check the state of device whether progrress or not, using DQ7, DQ6, or RY/$\overline{BY}$.
In the case of internal time-out, either hardware reset or a software Reset command is required to return the device to Read Mode.

10.21.4. DQ3 (Block Erase timer)

The Block Erase operation starts 50 μs (the Erase Hold Time) after the rising edge of $\overline{WE}$ in the last command cycle. DQ3 outputs a 0 for the duration of the Block Erase Hold Time and a 1 when the Block Erase operation starts. Additional Block Erase commands can only be accepted during the Block Erase Hold Time. Each Block Erase command input within the hold time resets the timer, allowing additional blocks to be marked for erasing. DQ3 outputs a 1 if the Program or Erase operation fails.

10.21.5. DQ2 (Toggle bit 2)

DQ2 is used to indicate which blocks have been selected for Auto Block Erase or to indicate whether the device is in Erase Suspend Mode.
If data is read continuously from the selected block during an Auto Block Erase, the DQ2 output will toggle. Now 1 will be output from non-selected blocks; thus, the selected block can be ascertained. If data is read continuously from the block selected for Auto Block Erase while the device is in Erase Suspend Mode, the DQ2 output will toggle. Because the DQ6 output is not toggling, it can be determined that the device is in Erase Suspend Mode. If data is read from the address to which data is being written during Erase Suspend in Programming Mode, DQ2 will output a 1.

10.21.6. RY/$\overline{BY}$ (READY/ $\overline{BUSY}$)

The TC58FVM6(T/B)5B has a RY/$\overline{BY}$ signal to indicate the device status to the host processor. A 0 (Busy state) indicates that an Auto-Program or auto-erase operation is in progress. A 1 (Ready state) indicates that the operation has finished and that the device can now accept a new command. RY/$\overline{BY}$ outputs a 0 when an operation has failed.

RY/$\overline{BY}$ outputs a 0 after the rising edge of $\overline{WE}$ in the last command cycle.

During an Auto Block Erase operation, commands other than Erase Suspend are ignored. RY/$\overline{BY}$ outputs a 1 during an Erase Suspend operation. The output buffer for the RY/$\overline{BY}$ pin is an open-drain type circuit, allowing a wired-OR connection. A pull-up resistor must be inserted between V_{DD} and the RY/$\overline{BY}$ pin.

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11. DATA PROTECTION

The TC58FVM6(T/B)5B includes a function which guards against malfunction or data corruption.

11.1. Protection against Program/Erase Caused by Low Supply Voltage

To prevent malfunction at power-on or power-down, the device will not accept commands while V_{DD} is below V_{LKO}. In this state, command input is ignored.
If V_{DD} drops below V_{LKO} during an Auto Operation, the device will terminate Auto-Program execution. In this case, Auto operation is not executed again when V_{DD} returns to recommended V_{DD} voltage. Therefore, command need to be input to execute Auto operation again.
When $V_{DD} > V_{LKO}$, make up countermeasure to be input accurately command in system side please.

11.2. Protection against Malfunction Caused by Glitches

To prevent malfunction write during operation caused by noise from the system, the device will not accept pulses shorter than 3 ns (Typ.) input on $\overline{WE}$, $\overline{CE}$ or $\overline{OE}$. However, if a glitch exceeding 3 ns (Typ.) occurs and the glitch is input to the device malfunction write may occur.
The device uses standard JEDEC commands. It is conceivable that, in extreme cases, system noise may be misinterpreted as part of a command sequence input and that the device will acknowledge it. Then, even if a proper command is input, the device may not operate. To avoid this possibility, clear the Command Register before command input. In an environment prone to system noise, Toshiba recommends input of a software or hardware reset before command input.

11.3. Protection against Malfunction at Power-on

To prevent damage to data caused by sudden noise at power-on, when power is turned on with $\overline{WE}=\overline{CE}=V_{IL}$ the device does not latch the command on the first rising edge of $\overline{WE}$ or $\overline{CE}$. Instead, the device automatically Resets the Command Register and enters Read Mode.

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12. ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		RANGE	UNIT
V_{DD}	V_{DD} Supply Voltage		−0.6~4.6V	V
V_{IN}	Input Voltage		−0.5~VDD+0.5V(≦4.6) (1)	V
V_{DQ}	Input/Output Voltage		−0.5~VDD+0.5V(≦4.6) (1)	V
V_{ID}	Maximum Input Voltage for A9, $\overline{OE}$ and $\overline{RESET}$ (2)		13.0	V
V_{ACC}	Maximum Input Voltage for $\overline{WP}$/ACC (2)		13.0	V
P_D	Power Dissipation		600	mW
T_{solder}	Soldering Temperature (10s)		260	°C
T_{stg}	Storage Temperature	TC58FVM6(T/B)5BTG	−55~150	°C
		TC58FVM6(T/B)5BXG	−55~125	°C
T_{opr}	Operating Temperature		−40~85	°C
I_{OSHORT}	Output Short-Circuit Current(3)		100	mA

(1) This level may undershoot to −2.0 V for periods < 20 ns, and may overshoot to +2.0 V for periods < 20 ns.
(2) Do not apply V_{ID}/V_{ACC} when the supply voltage is not within the device's recommended operating voltage range.
(3) Outputs should be shorted for no more than one second.
No more than one output should be shorted at a time.

13. CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	CONDITION	MAX	UNIT
C_{IN}	Input Pin Capacitance	V_{IN} = 0 V	7	pF
C_{OUT}	Output Pin Capacitance	V_{OUT} = 0 V	12	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0 V	7	pF
C_{IN3}	$\overline{WP}$/ACC Capacitance	V_{IN} = 0 V	14	pF

This parameter is periodically sampled and is not tested for every device.

14. RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	MAX	UNIT
V_{DD}	V_{DD} Supply Voltage	2.7	3.6	V
V_{IH}	Input High-Level Voltage	0.7 × V_{DD}	V_{DD} + 0.3	
V_{IL}	Input Low-Level Voltage	−0.3	0.2 × V_{DD}	
V_{ID}	High-Level Voltage for A9, $\overline{OE}$ and $\overline{RESET}$	11.4	12.6	
V_{ACC}	High-Level Voltage for $\overline{WP}$/ACC	8.5	12.6	
Ta	Operating Ambient Temperature	−40	85	°C

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15. DC CHARACTERISTICS

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
I_{LI}	Input Leakage Current	0 V ≦ V_{IN} ≦ V_{DD}	—	—	±1	μA
I_{LO}	Output Leakage Current	0 V ≦ V_{OUT} ≦ V_{DD}	—	—	±1	
V_{OH}	Output High Voltage	I_{OH} = −0.1 mA	V_{DD} − 0.4	—	—	V
		I_{OH} = −2.5 mA	0.85 x V_{DD}	—	—	
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA	—	—	0.4	
I_{DDO1}	V_{DD} Average Random Read Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA t_{RC} =100ns	—	37	55	mA
I_{DDO2}	V_{DD} Average Program Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA	—	11	15	
I_{DDO3}	V_{DD} Average Erase Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA	—	9	15	
I_{DDO4}	V_{DD} Average Read-While-Program Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA t_{RC} = 100ns	—	48	70	
I_{DDO5}	V_{DD} Average Read-while-Erase Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA t_{RC} = 100ns	—	46	70	
I_{DDO6}	V_{DD} Average Program-while-Erase-Suspend Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA	—	11	15	
I_{DDO7}	V_{DD} Average Page Read Current	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA t_{PRC} = 25ns	—	2	5	
I_{DDO8}	V_{DD} Average Address Increment Read Current (2)	V_{IN} = V_{IH}/V_{IL}, I_{OUT} = 0 mA t_{RC} =100ns t_{PRC} = 25ns	—	5	11	
I_{DDS1}	VDD Standby Current	$\overline{WP}$/ACC = V_{DD} and $\overline{CE}$ = $\overline{RESET}$ = V_{DD} or $\overline{RESET}$ = V_{SS}	—	3	10	μA
I_{DDS2}	V_{DD} Standby Current (Automatic Sleep Mode(1))	V_{IH} = V_{DD} V_{IL} = V_{SS}	—	3	10	
I_{ID}	High-Voltage Input Current for A9, $\overline{OE}$ and $\overline{RESET}$	11.4 V ≦ V_{ID} ≦ 12.6 V	—	—	35	
I_{ACC}	High-Voltage Input Current for $\overline{WP}$/ACC	8.5V ≦ V_{ACC} ≦12.6 V	—	—	20	mA
V_{LKO}	Low-V_{DD} Lock-out Voltage	—	1.0	—	2.0	V

(1) The device enters Automatic Sleep Mode in which the address remains fixed for during 150 ns.

(2) (I_{DDO1+} I_{DDO7} × 7)／8words

16. AC TEST CONDITIONS

PARAMETER	CONDITION
Input Pulse Level	V_{DD}, 0.0 V
Input Pulse Rise and Fall Time (10%~90%)	5 ns
Timing Measurement Reference Level (input)	V_{DD}/2, V_{DD}/2
Timing Measurement Reference Level (output)	V_{DD}/2, V_{DD}/2
Output Load	C_L (100 pF) + 1 TTL Gate / C_L (30 pF) + 1 TTL Gate

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17. AC CHARACTERISTICS AND OPERATING CONDITIONS

17.1. Read Cycle

	Output load capacitance (CL)	30 pF		100 pF		
Symbol	Parameter	MIN	MAX	MIN	MAX	UNIT
t_{RC}	Read Cycle Time	65	—	70	—	ns
t_{PRC}	Page Read Cycle Time	25	—	30	—	ns
t_{ACC}	Address Access Time	—	65	—	70	ns
t_{CE}	$\overline{CE}$ Access Time	—	65	—	70	ns
t_{OE}	$\overline{OE}$ Access Time	—	25	—	30	ns
t_{PACC}	Page Access Time	—	25	—	30	ns
t_{OEH}	$\overline{OE}$ High-Level Hold Time (read)	0	—	0	—	ns
t_{CEE}	$\overline{CE}$ to Output Low-Z	0	—	0	—	ns
t_{OEE}	$\overline{OE}$ to Output Low-Z	0	—	0	—	ns
t_{OH}	Output Data Hold Time	0	—	0	—	ns
t_{AOH}	Output Data Hold Time (Page Read)	0	—	0	—	ns
t_{DF1}	$\overline{CE}$ to Output High-Z	—	25	—	25	ns
t_{DF2}	$\overline{OE}$ to Output High-Z	—	25	—	25	ns

Hardware RESET ($\overline{RESET}$)

Symbol	Parameter	MIN	MAX	UNIT
t_{READY}	Read Mode Recovery Time from $\overline{RESET}$ (During Auto Operation)	—	25	μs
t_{READY}	Read Mode Recovery Time from $\overline{RESET}$ （During Non Auto Operation）	—	500	ns
t_{RP}	$\overline{RESET}$ Low Level Hold Time	500	—	ns
t_{RH}	Recovery Time from $\overline{RESET}$	50	—	ns
t_{RPD}	$\overline{RESET}$ goes Low to Standby Mode	20	—	μs

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17.2. Block Protect

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{VPT}	V_{ID} Transition Time	4	—	μs
t_{VPS}	V_{ID} Set-up Time	4	—	μs
t_{CESP}	$\overline{CE}$ Set-up Time	4	—	μs
t_{VPH}	$\overline{OE}$ Hold Time	4	—	μs
t_{PPLH}	$\overline{WE}$ Low-Level Hold Time	100	—	μs

17.3. Program and Erase characteristics

SYMBOL	PARAMETER	MIN	TYP.	MAX	UNIT
t_{PPW}	Auto-Program Time (Word Mode)	—	11	300	μs
t_{PPW}	Accelerated Auto-Program Time (Word Mode)	—	8	300	μs
t_{PPAW}	Auto-Page program time	—	58	2400	μs
t_{PPAW}	Accelerated Auto-Page program time	—	21	2400	μs
t_{PCEW}	Auto Chip Erase Time(1)	—	94	675	s
t_{PCEW}	Accelerated Auto Chip Erase Time(1)	—	81	675	s
t_{PBEW}	Auto Block Erase Time(1)	—	0.7	5(2)	s
t_{EW}	Erase/Program Cycle	10^5	—	—	Cycle.

(1) Auto Chip Erase Time and Auto Block Erase Time include internal pre program time.

(2) Minimum interval between resume and the following suspend command is 150 μs. If it's shorter than 150 μs, auto block erase time is expand more than maximum(5 s).

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17.4. Command Write/Program/Erase cycle

SYMBOL	PARAMETER	MIN	MAX	UNIT
t_{CMD}	Command Write Cycle Time	60	—	ns
t_{AS}	Address Set-up Time	0	—	ns
t_{AH}	Address Hold Time	30	—	ns
t_{DS}	Data Set-up Time	30	—	ns
t_{DH}	Data Set-up Time	0	—	ns
t_{WELH}	$\overline{WE}$ Low-Level Hold Time ($\overline{WE}$ Control)	30	—	ns
t_{WEHH}	$\overline{WE}$ High-Level Hold Time ($\overline{WE}$ Control)	20	—	ns
t_{CES}	$\overline{CE}$ Set-up Time to $\overline{WE}$ Active ($\overline{WE}$ Control)	0	—	ns
t_{CEH}	$\overline{CE}$ Hold Time from $\overline{WE}$ High Level ($\overline{WE}$ Control)	0	—	ns
t_{CELH}	$\overline{CE}$ Low-Level Hold Time ($\overline{CE}$ Control)	30	—	ns
t_{CEHH}	$\overline{CE}$ High-Level Hold Time ($\overline{CE}$ Control)	20	—	ns
t_{WES}	$\overline{WE}$ Set-up time to $\overline{CE}$ Active ($\overline{CE}$ Control)	0	—	ns
t_{WEH}	$\overline{WE}$ Hold Time from $\overline{CE}$ High Level ($\overline{CE}$ Control)	0	—	ns
t_{OES}	$\overline{OE}$ Set-up Time	0	—	ns
t_{OEHP}	$\overline{OE}$ High Level Hold Time (Polling)	10	—	ns
t_{OEHT}	$\overline{OE}$ High Level Hold Time (Toggle Read)	20	—	ns
t_{CEHT}	$\overline{CE}$ High Level Hold Time (Toggle Read)	20	—	ns
t_{AHT}	Address Hold Time (Toggle)	0	—	ns
t_{AST}	Address Set-up Time (Toggle)	0	—	ns
t_{BEH}	Erase Hold Time	50	—	μs
t_{VDS}	V_{DD} Set-up Time	500	—	μs
t_{BUSY}	Program/Erase Valid to RY/$\overline{BY}$ Delay	—	90	ns
	Program/Erase Valid to RY/$\overline{BY}$ Delay during Suspend Mode	—	300	ns
t_{RB}	RY/$\overline{BY}$ Recovery Time	0	—	ns
t_{SUSP}	Program Suspend Command to Suspend Mode	—	2	μs
t_{SUSPA}	Page Program Suspend Command to Suspend Mode	—	2.5	μs
t_{RESP}	Program Resume Command to Program Mode	—	1	μs
t_{SUSE}	Erase Suspend Command to Suspend Mode	—	25	μs
t_{RESE}	Erase Resume Command to Erase Mode	—	1	μs

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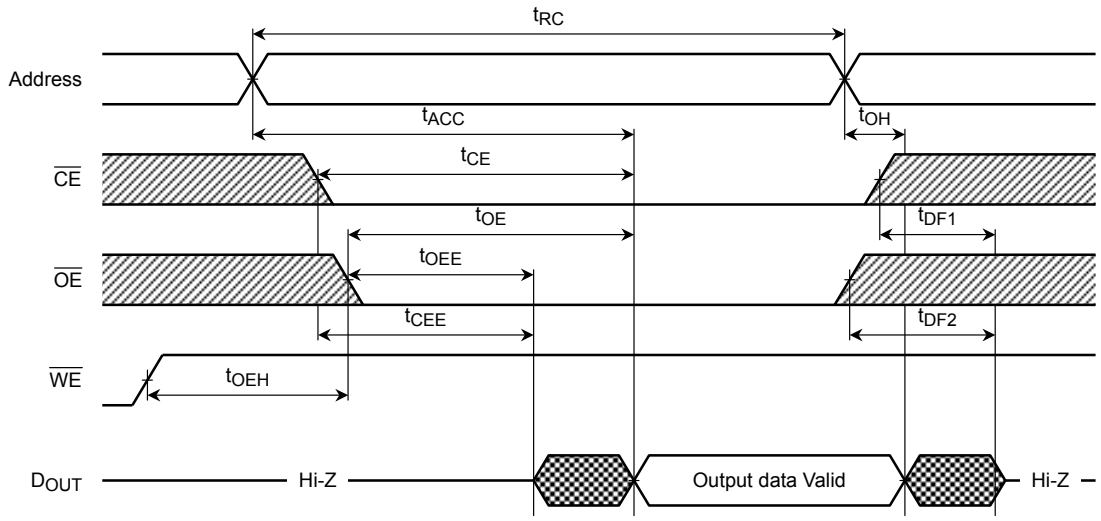
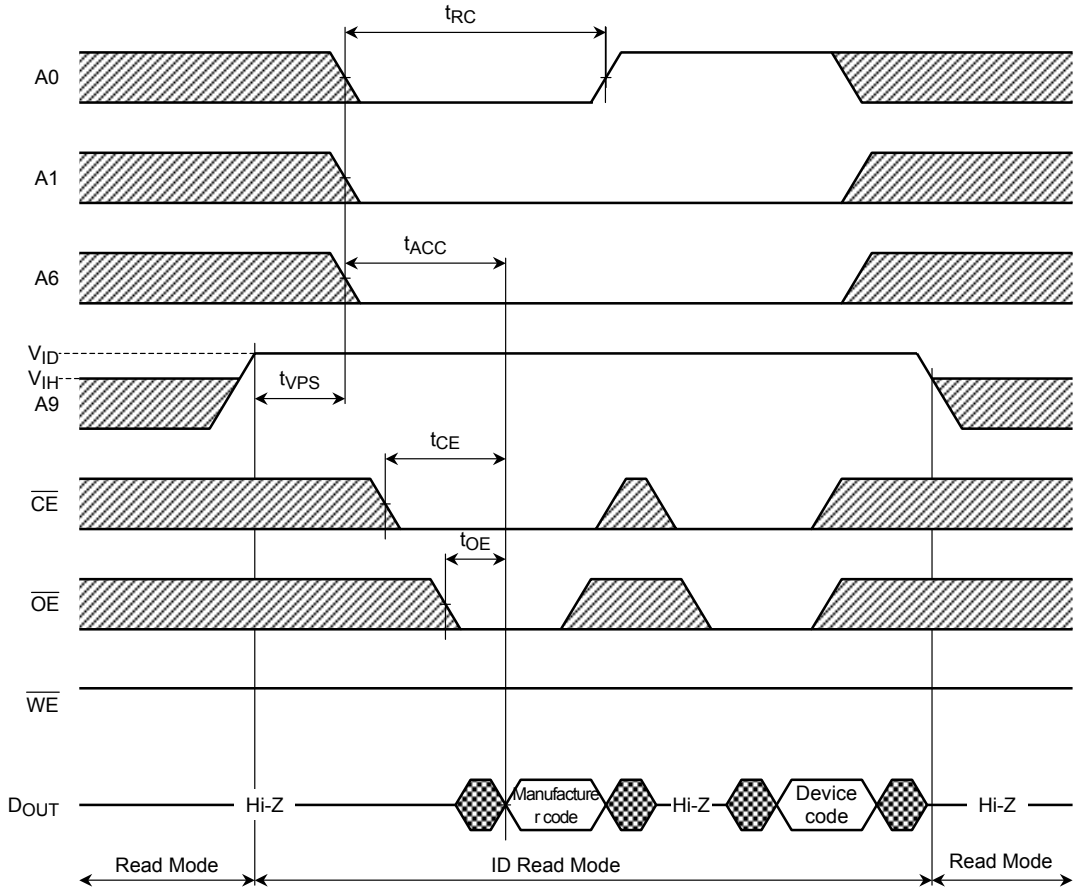
18. TIMING DIAGRAMS

V_{IH} or V_{IL} Data invalid

Read/ID Read Operation



ID Read Operation (apply V_{ID} to A9)



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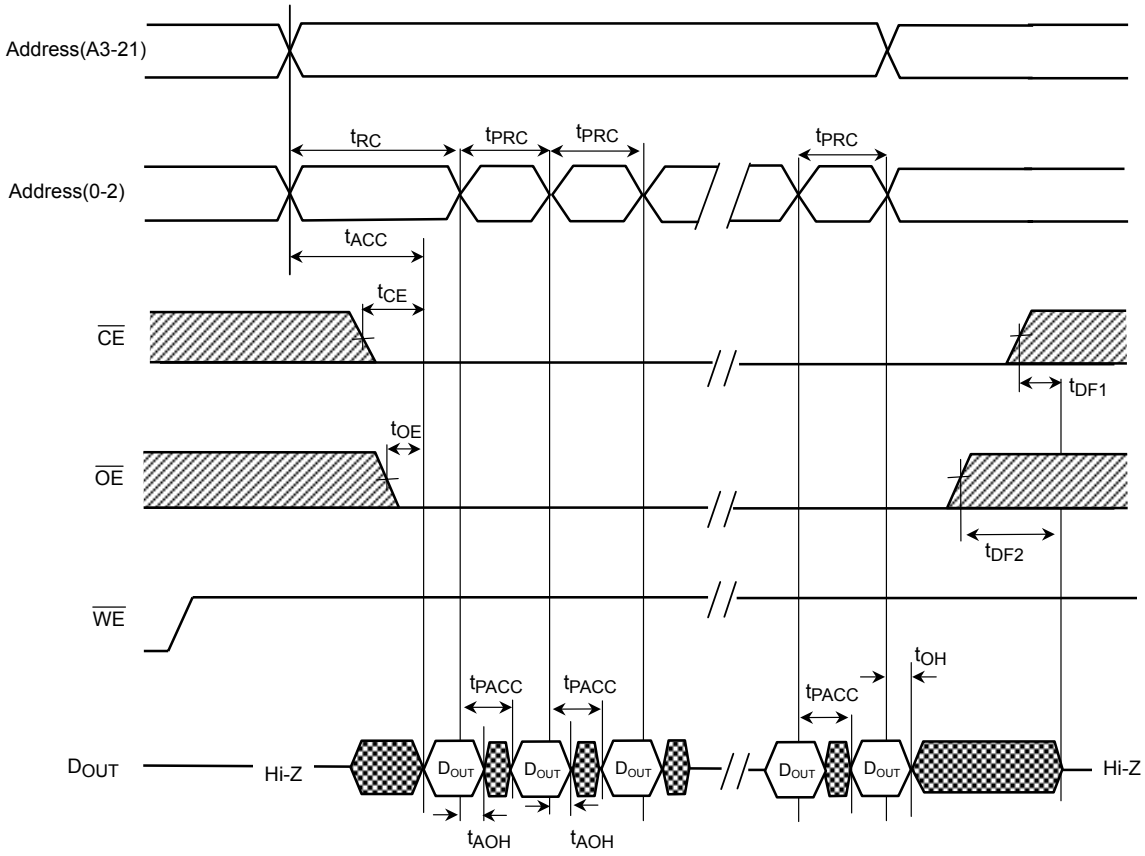
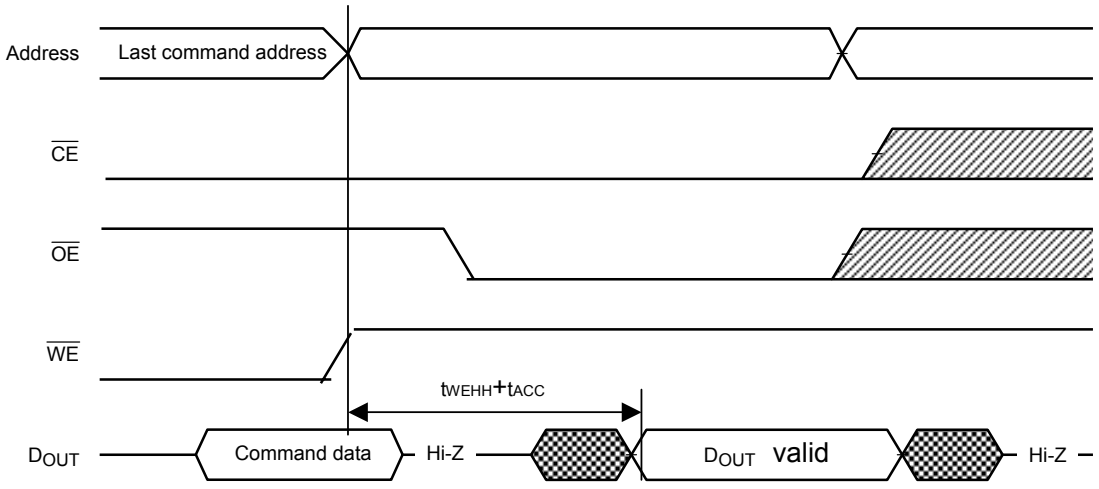
Page Read Operation



Read after command input (Only Hidden Rom/CFI Read)



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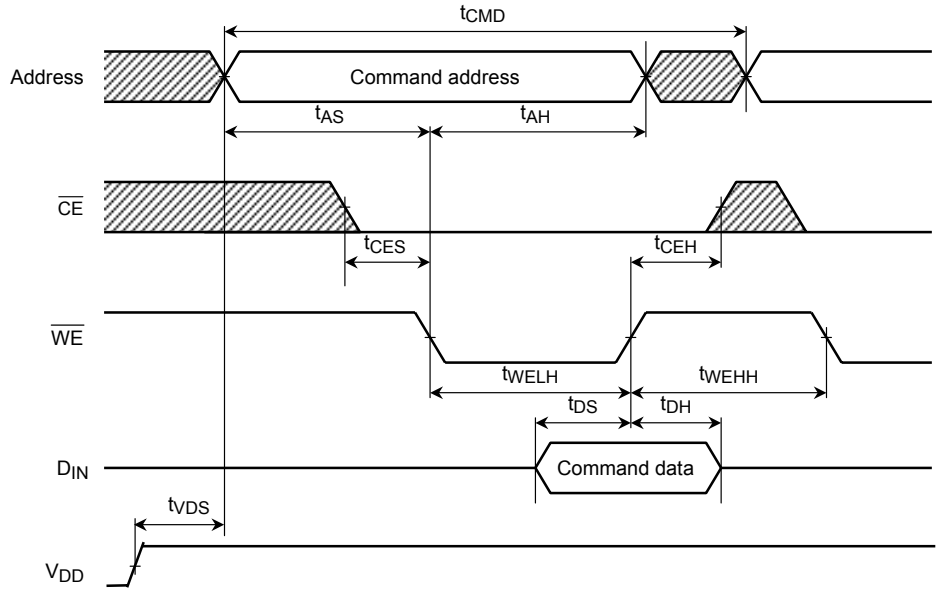
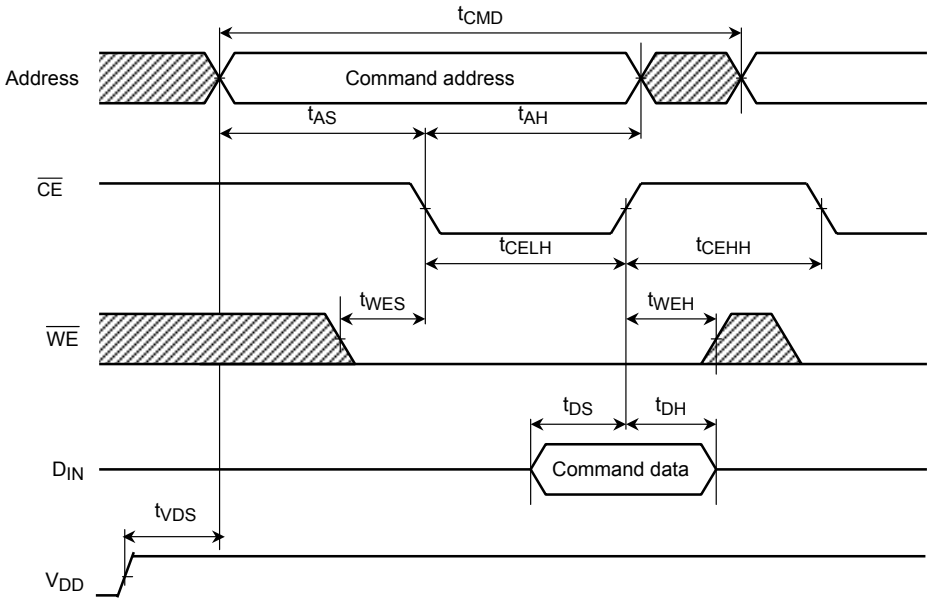
Command Write Operation

This is the timing of the Command Write Operation. The timing which is described in the following pages is essentially the same as the timing shown on this page.

- $\overline{WE}$ Control



- $\overline{CE}$ Control



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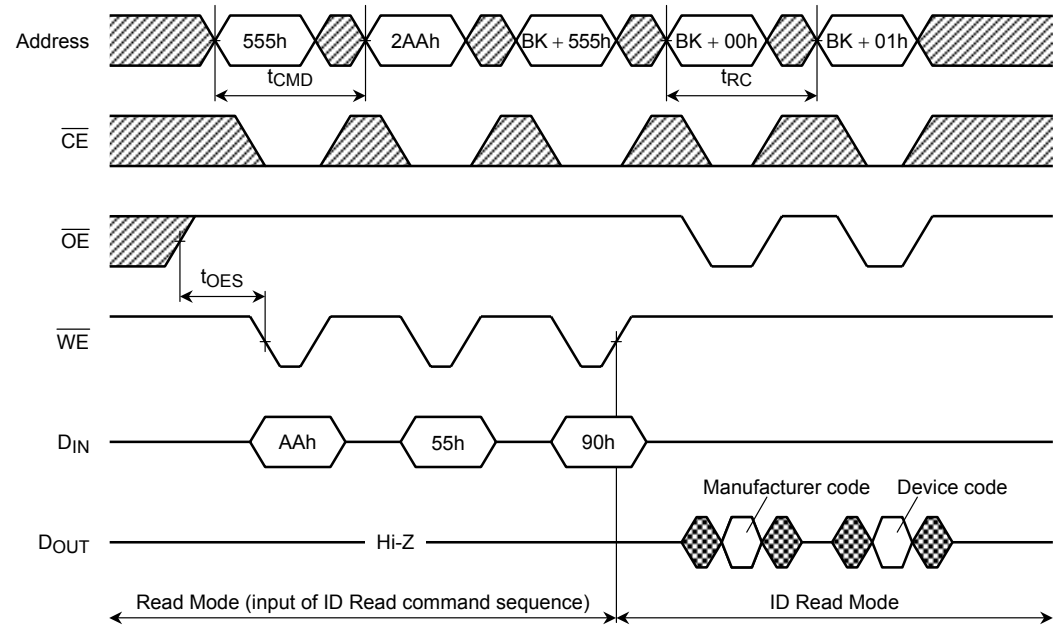
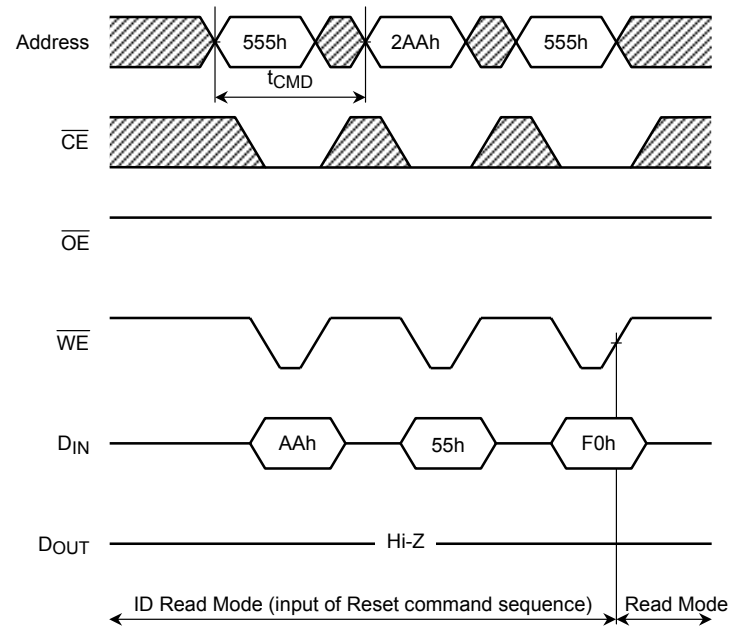
ID Read Operation (input command sequence)



(Continued)



BK: Bank address

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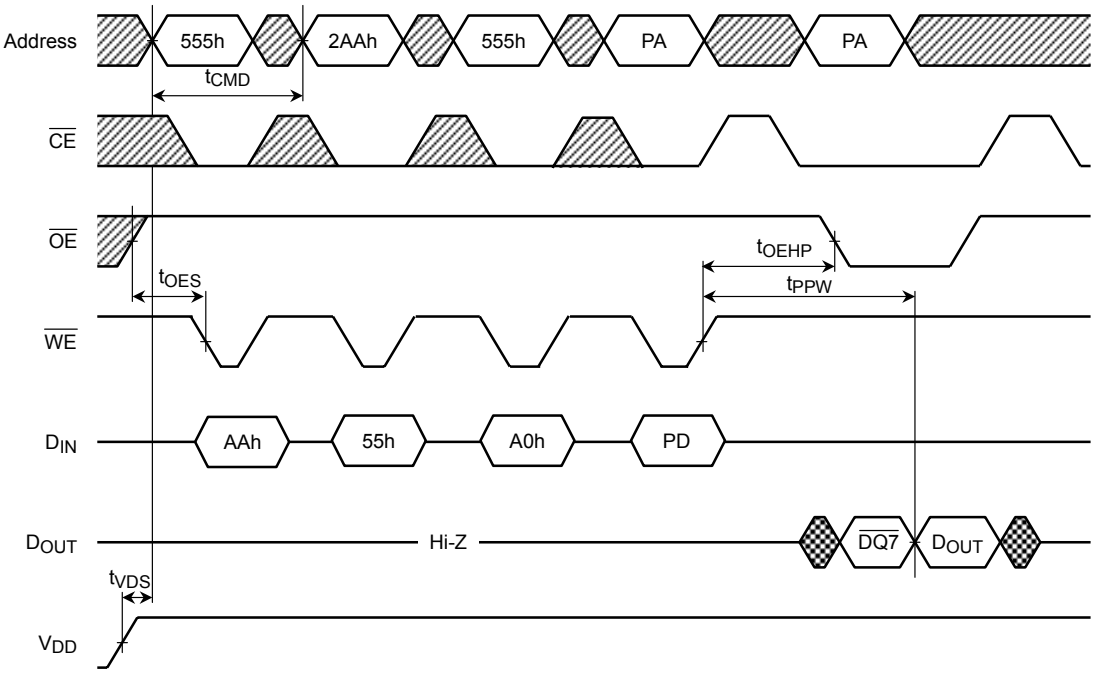
Auto-Program Operation ($\overline{WE}$ Control)



Notes: PA: Program address
PD: Program data

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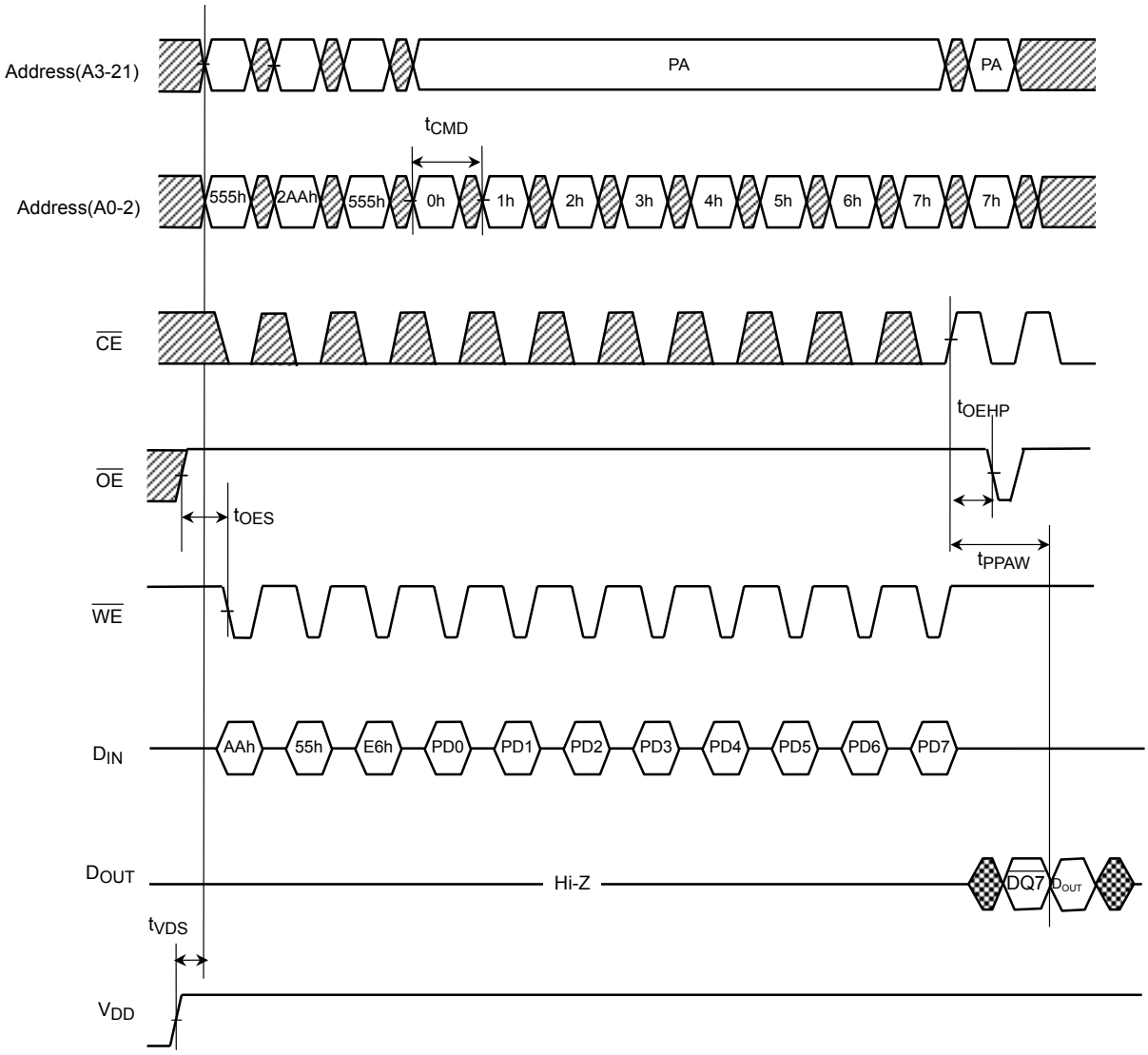
Auto Page Program Operation ($\overline{WE}$ Control)



Notes: PA: Program address
PD: Program Data

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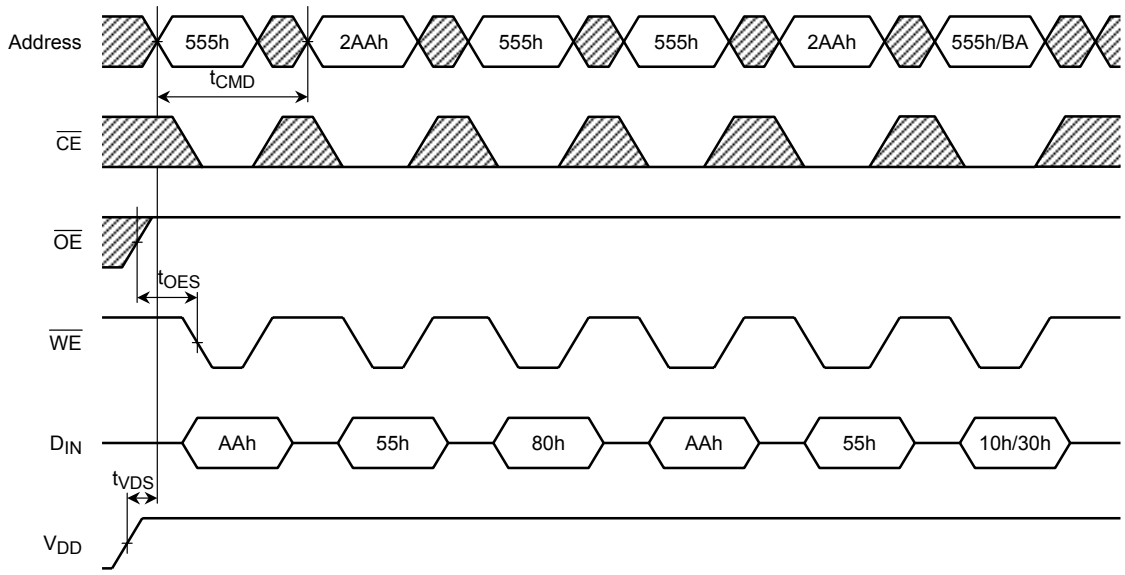
Auto Chip Erase/Auto Block Erase Operation ($\overline{WE}$ Control)



Notes: BA: Block Address

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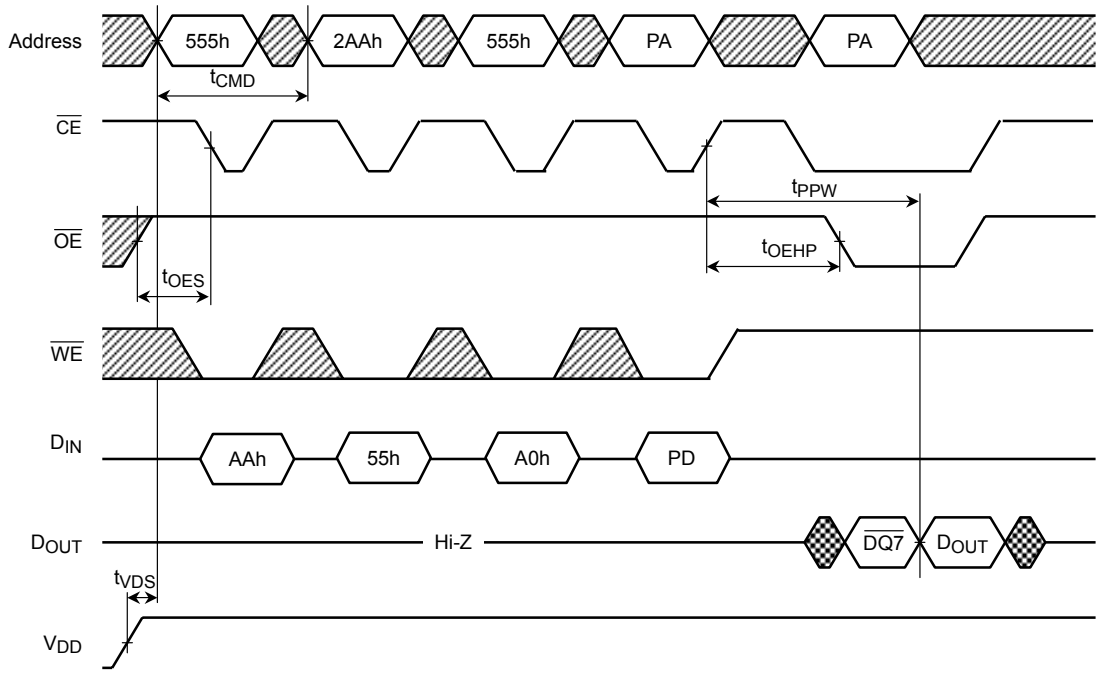
Auto-Program Operation ($\overline{CE}$ Control)



Note: PA: Program address
PD: Program data

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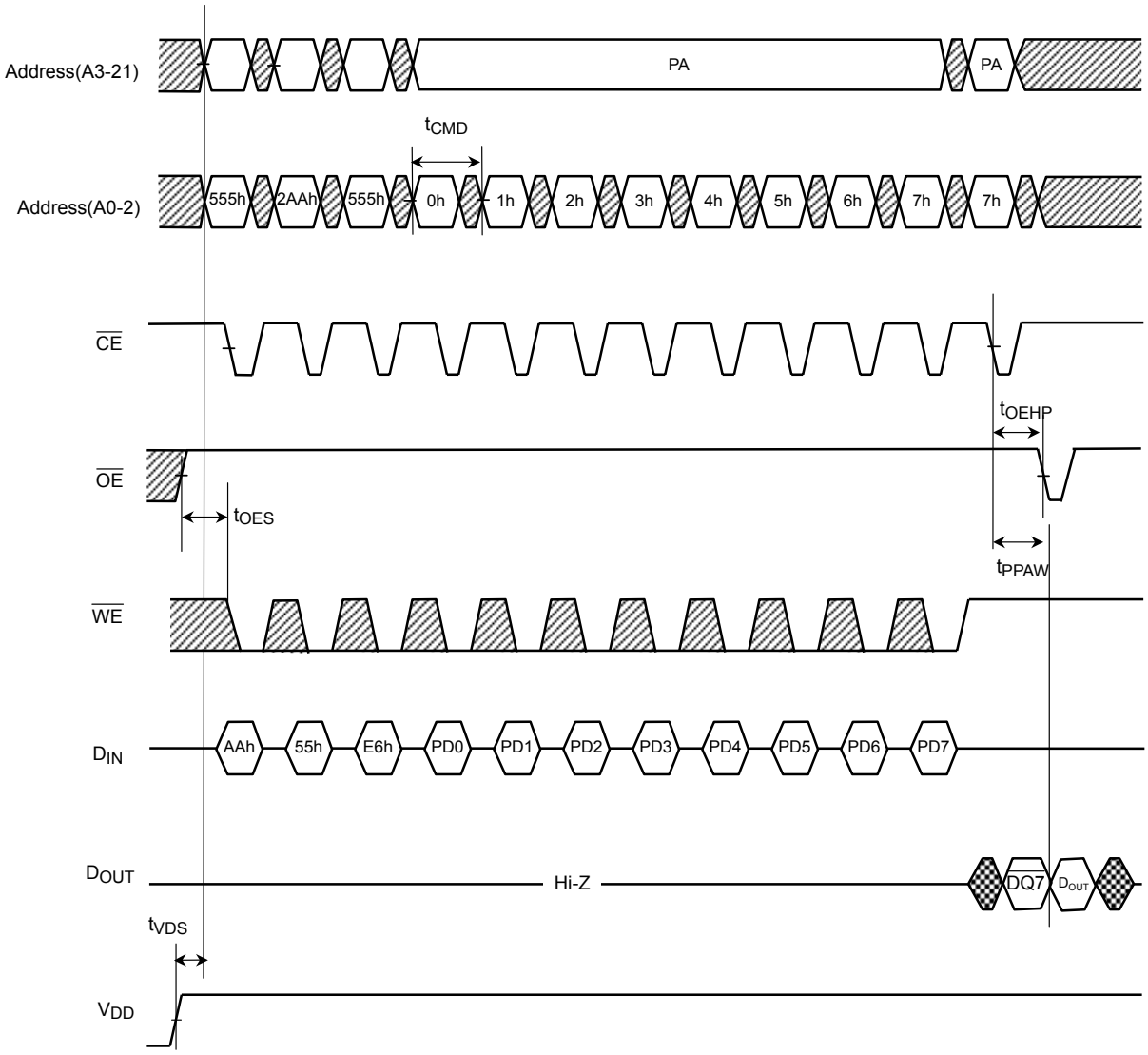
Auto Page Program Operation ($\overline{CE}$ Control)



Notes: PA: Program address
PD: Program data

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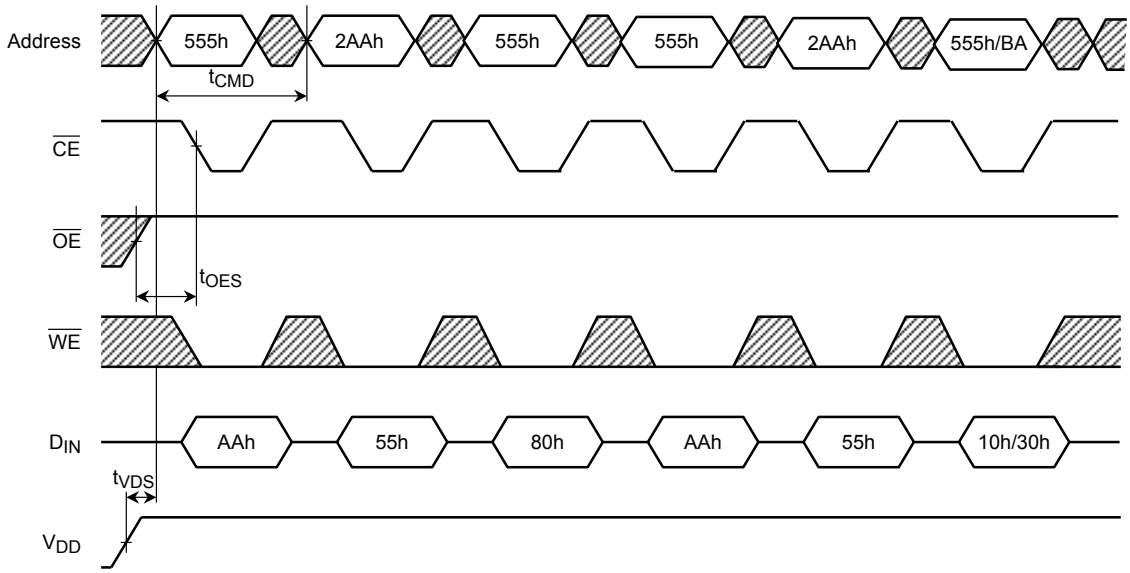
Auto Chip Erase/Auto Block Erase Operation ($\overline{CE}$ Control)



Note: BA: Block address for Auto Block Erase operation

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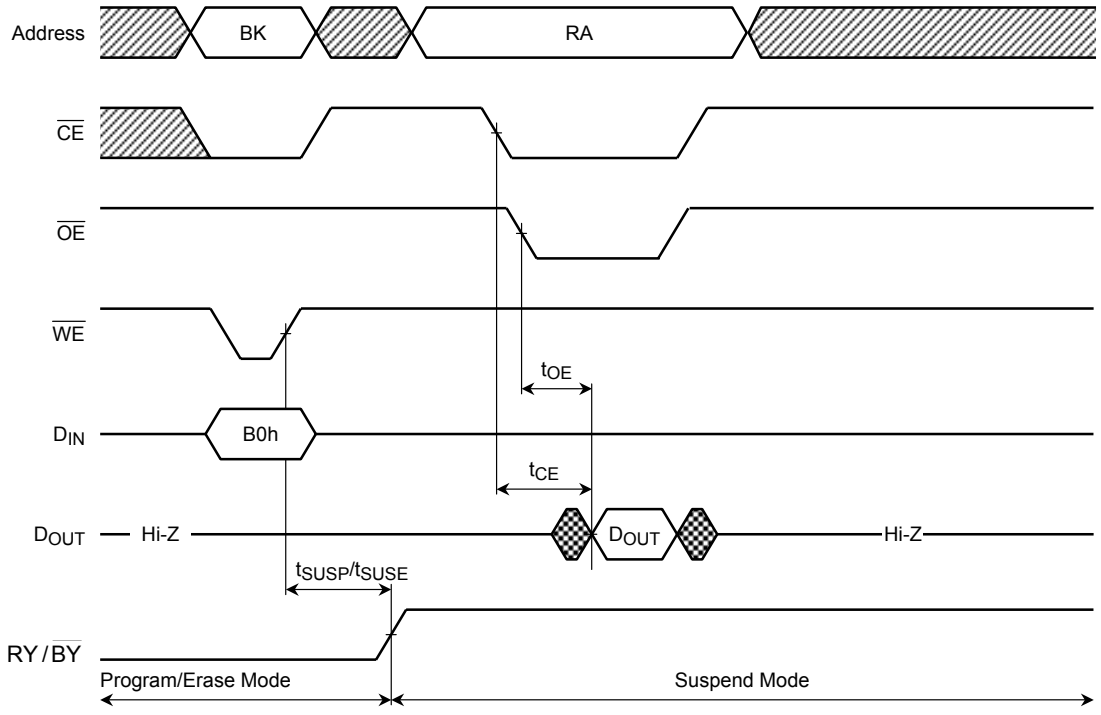
Program/Erase Suspend Operation



RA: Read address

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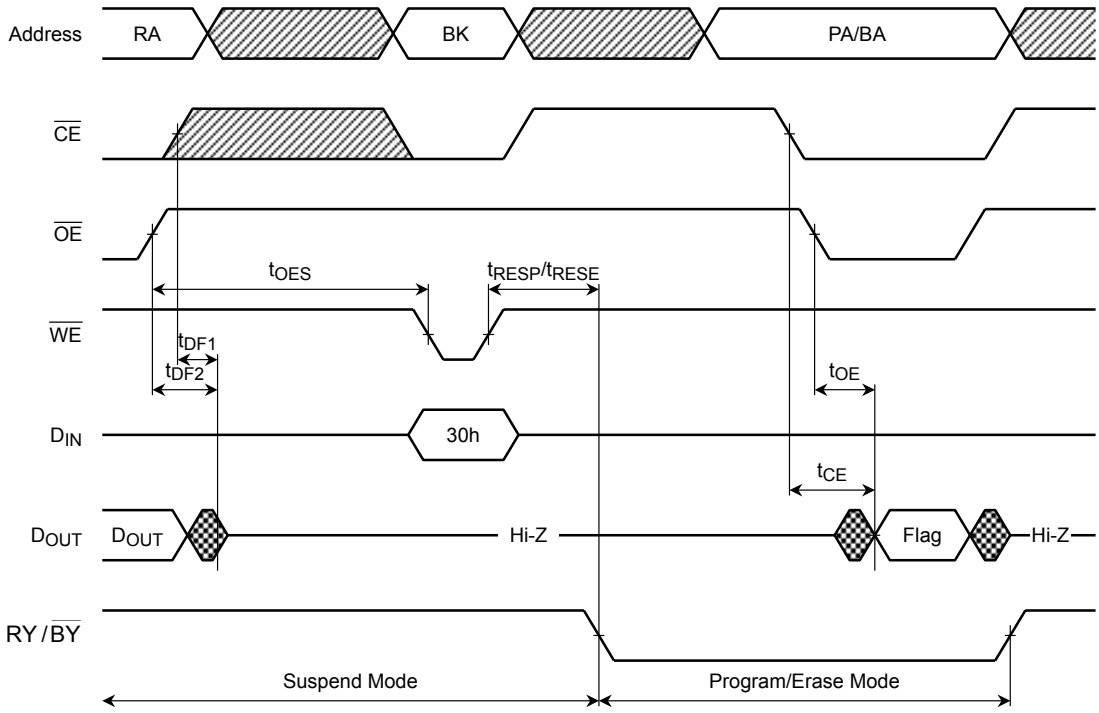
Program/Erase Resume Operation



PA: Program address
BK: Bank address
BA: Block address
RA: Read address
Flag: Hardware Sequence flag

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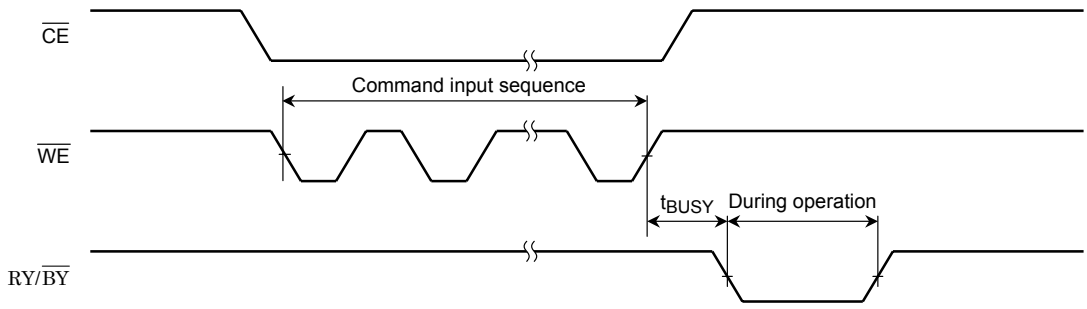
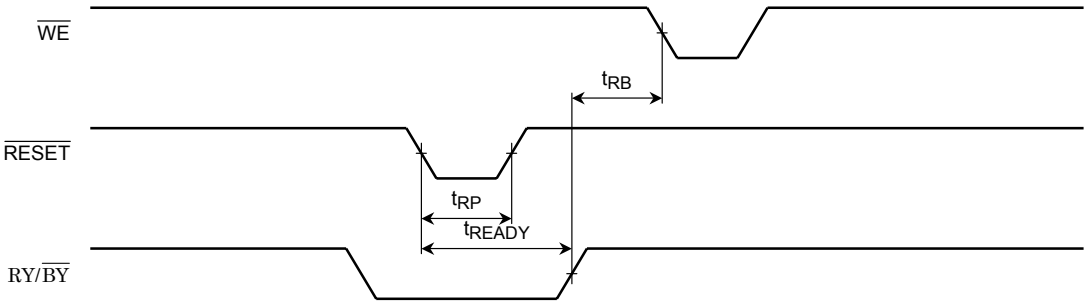
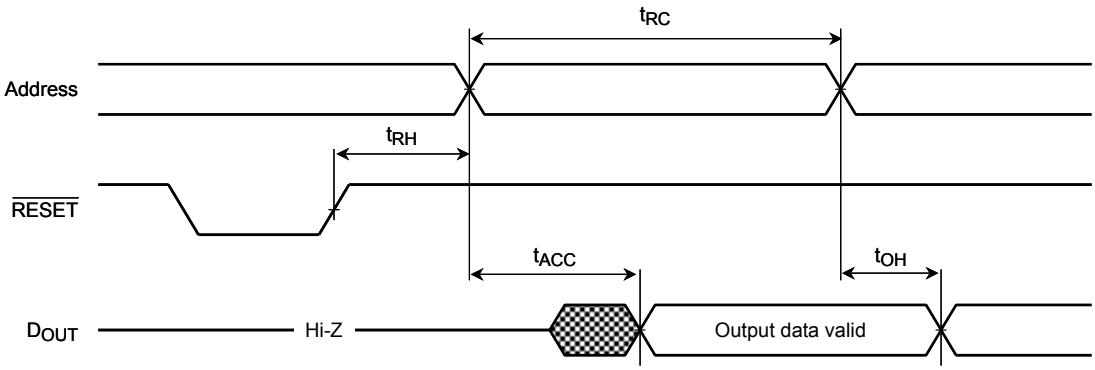
RY/$\overline{BY}$ during Auto Program/Erase Operation



Hardware Reset Operation (At the Auto Operation)



Read after $\overline{RESET}$



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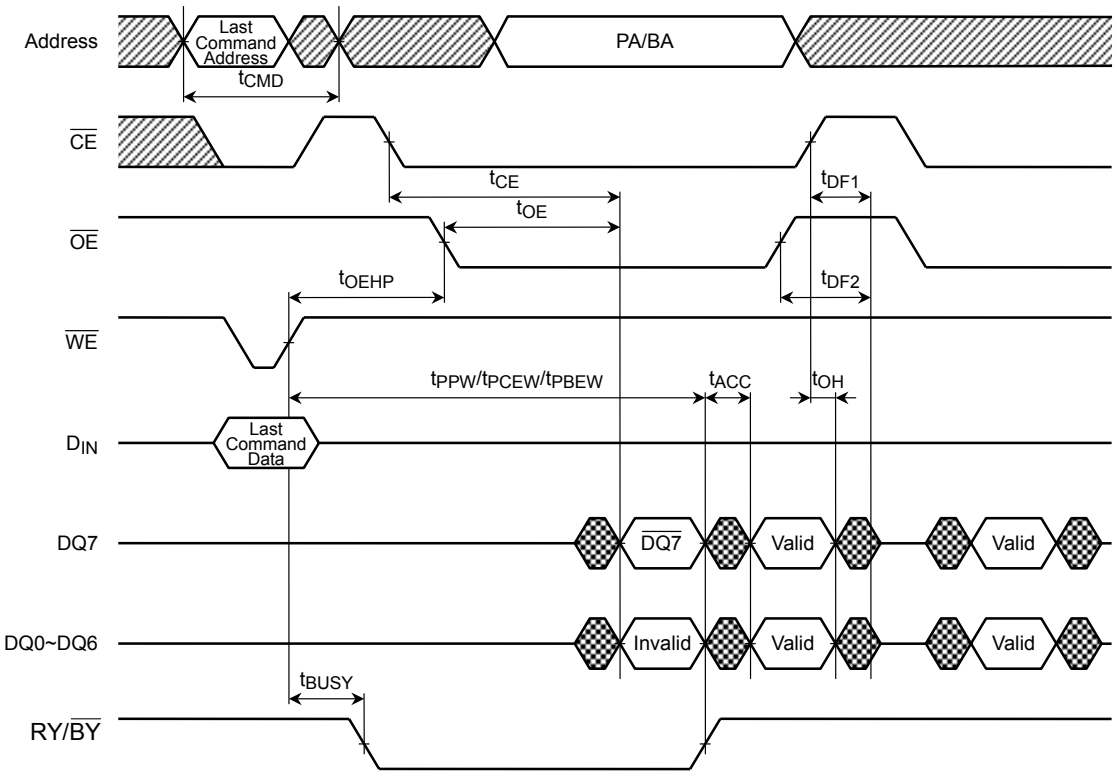
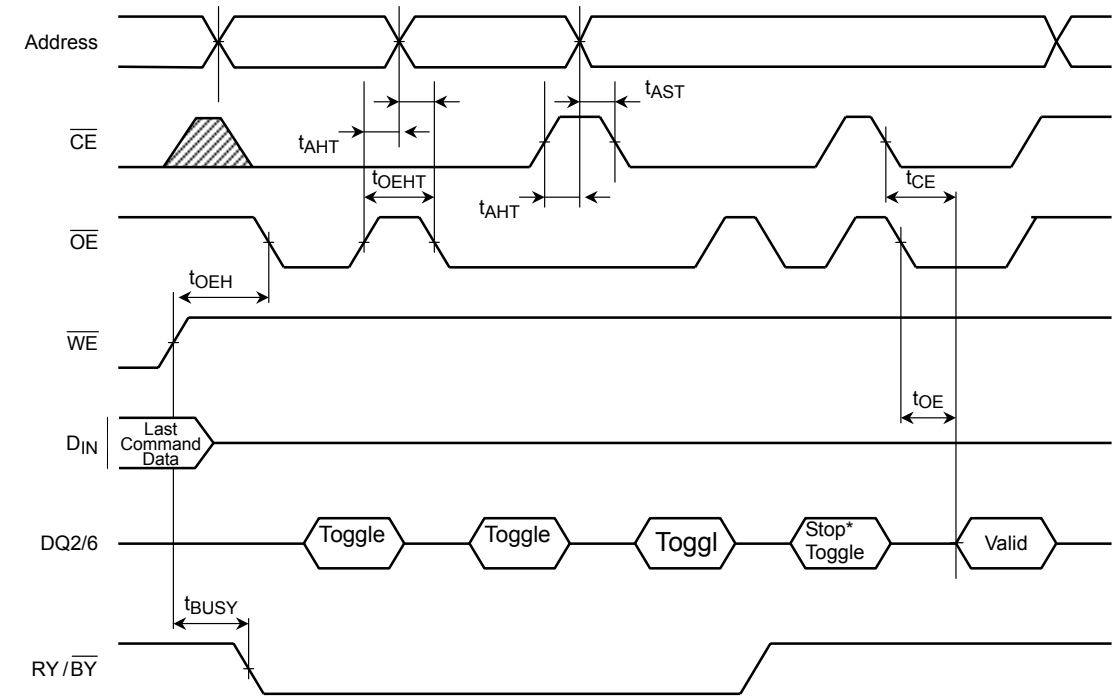
Hardware Sequence Flag ($\overline{DATA}$ Polling)



PA: Program address
BA: Block address

Hardware Sequence Flag (Toggle bit)



*DQ2/DQ6 stops toggling when auto operation has been completed.

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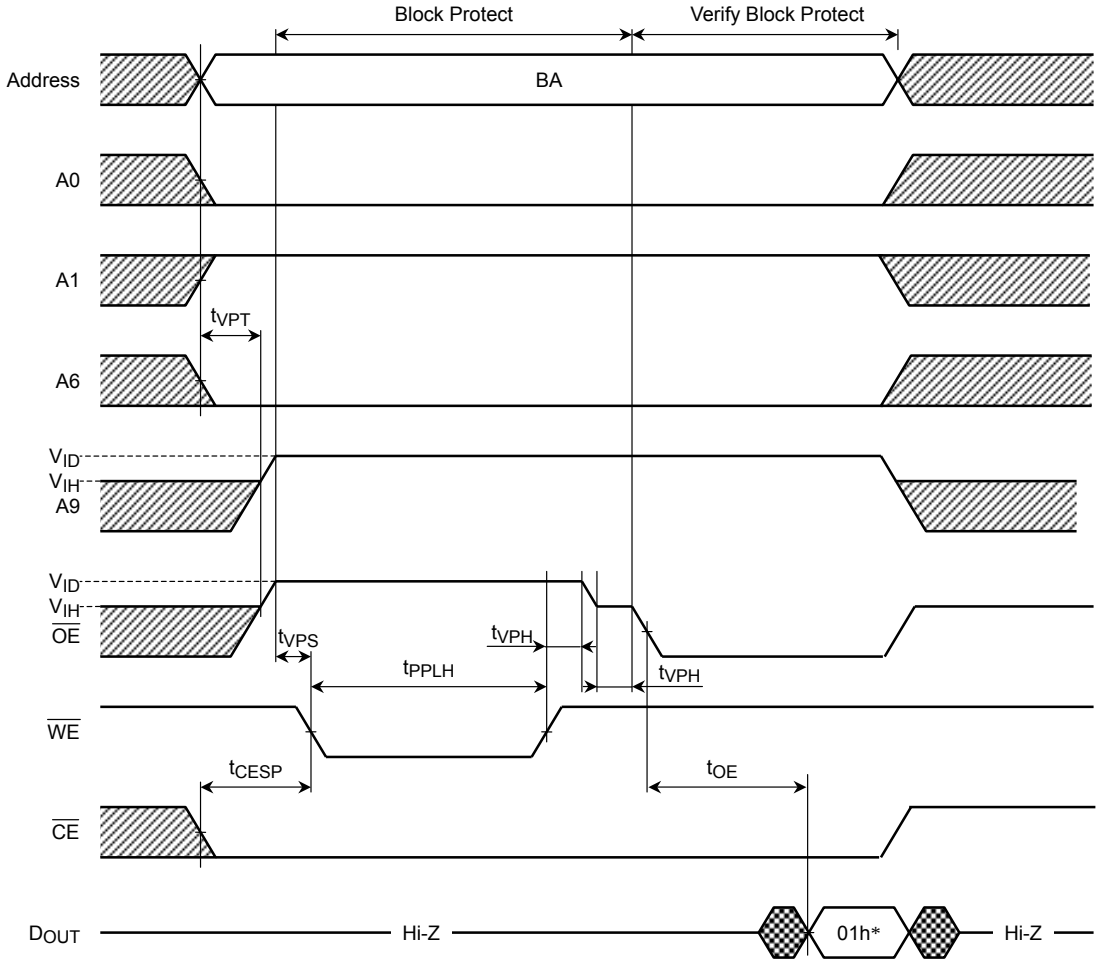
Block Protect 1 Operation (PPB Set)



BA: Block address

*: 01h indicates that block is protected.

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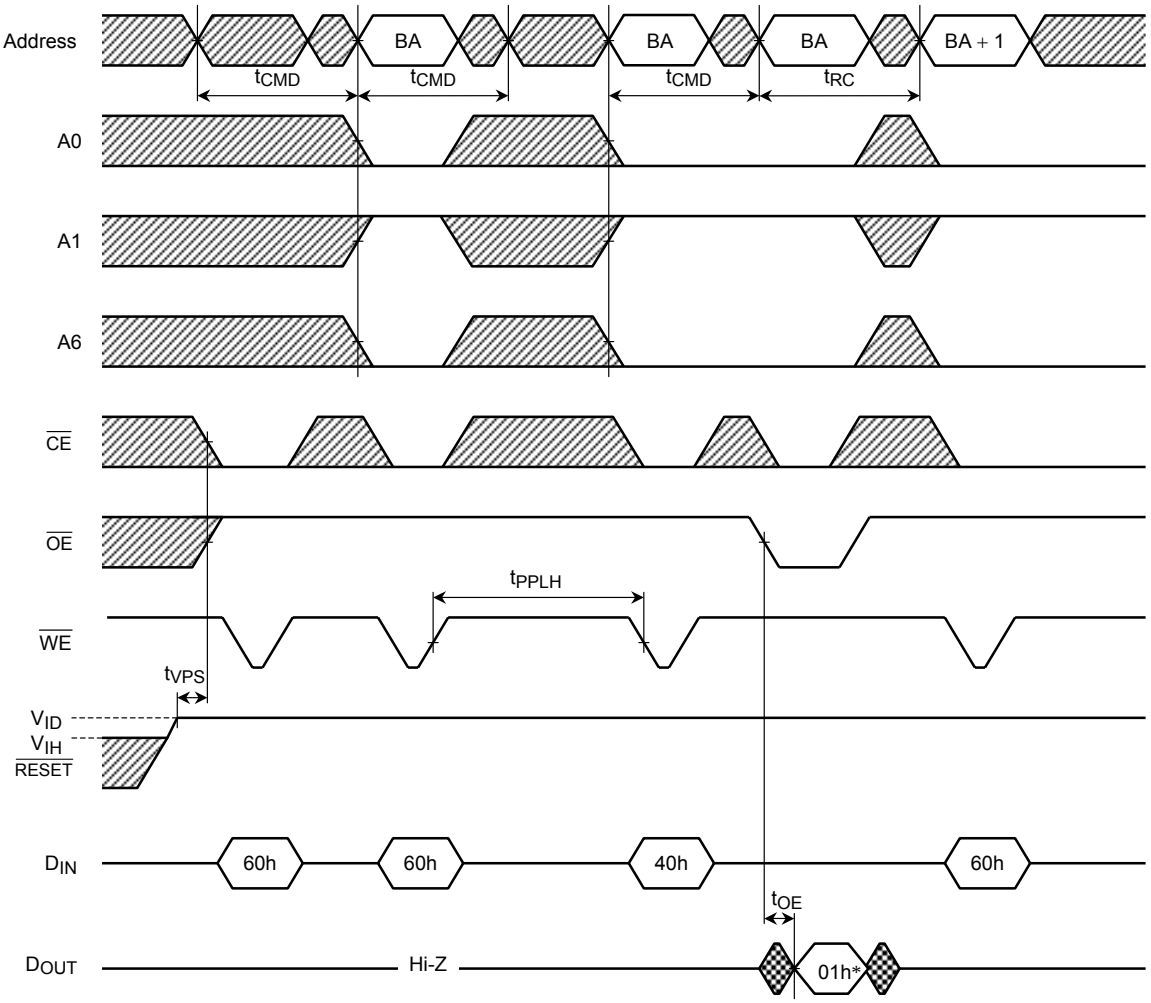
Block Protect 2 Operation (PPB Set)



BA: Block address
BA + 1: Address of next block
*: 01h indicates that block is protected.

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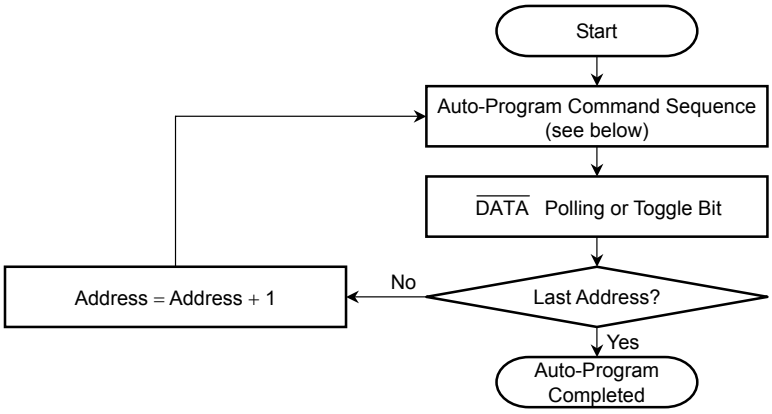
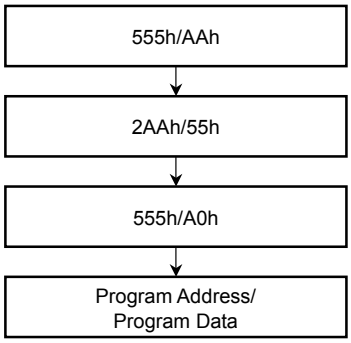
19. FLOWCHARTS

Auto-Program



Auto-Program Command Sequence (address/data)



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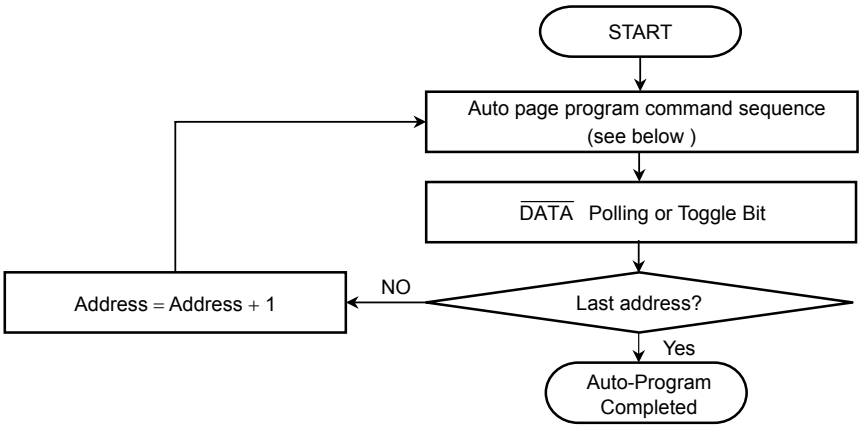
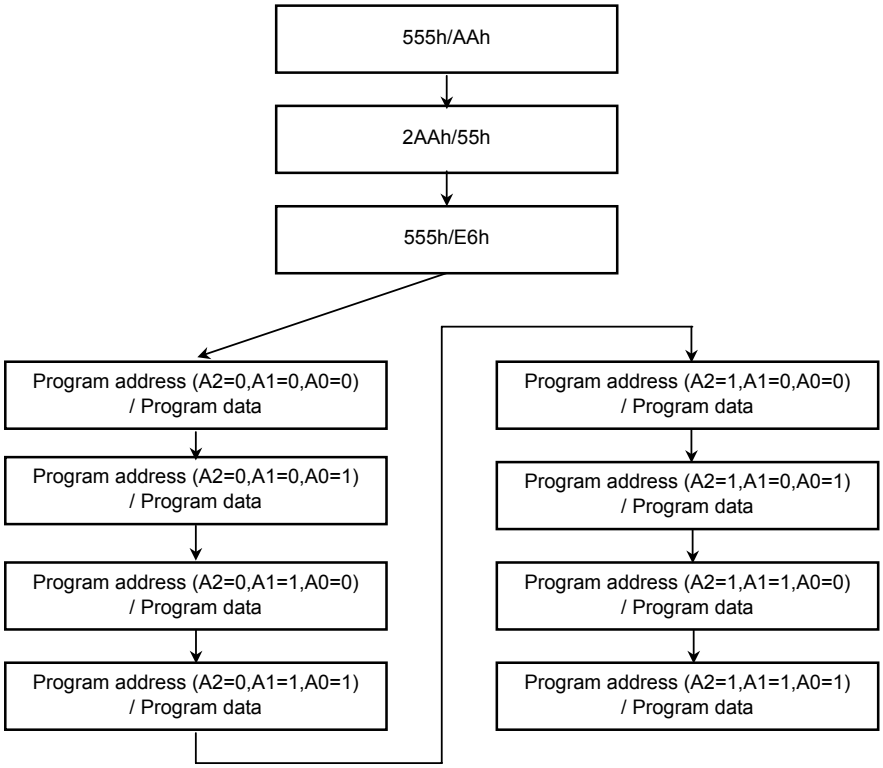
Auto-Page Program





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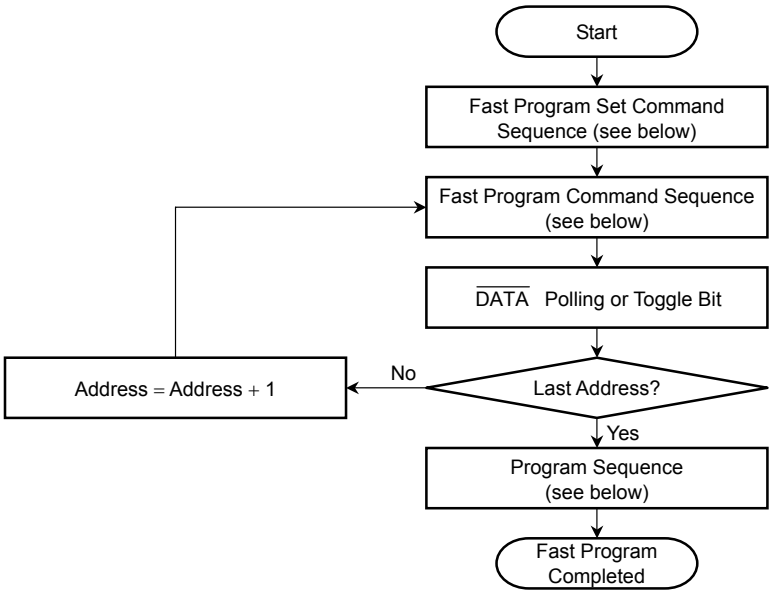
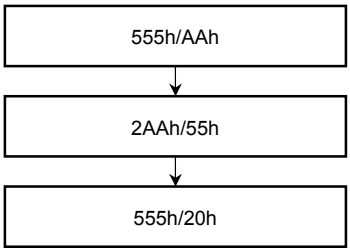
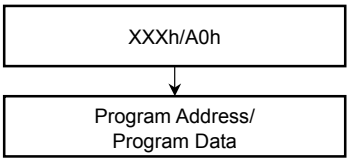
Fast Program



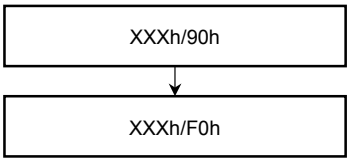
Fast Program Set Command Sequence (address/data)



Fast Program Command Sequence (address/data)



Fast Program Reset Command Sequence (address/data)



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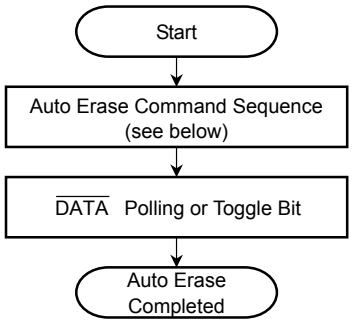
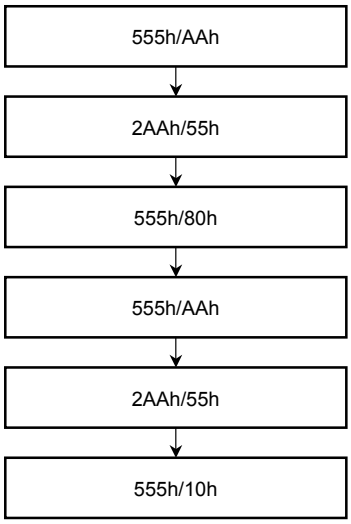
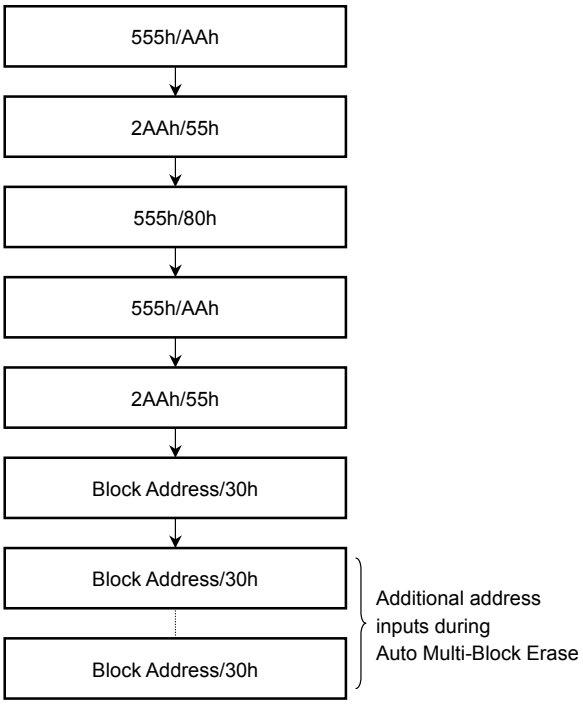
Auto Erase



Auto Chip Erase Command Sequence
(address/data)



Auto Block/Auto Multi-Block Erase Command Sequence
(address/data)



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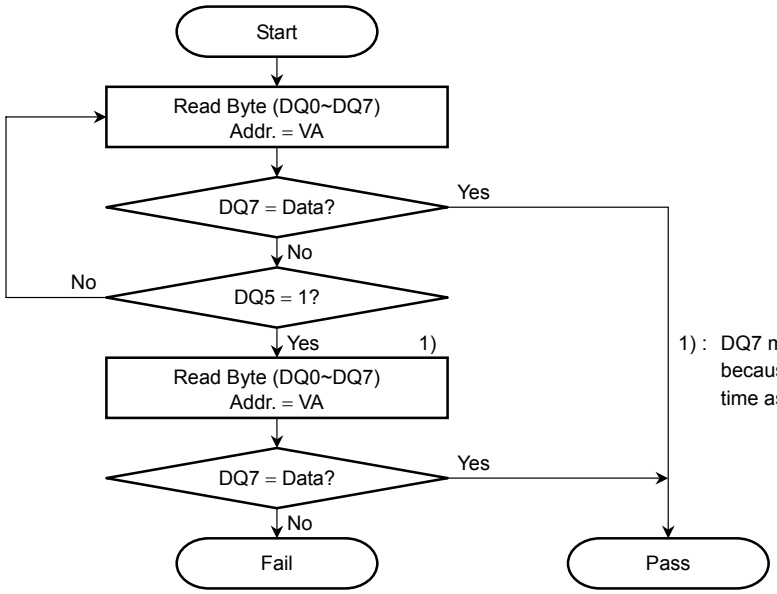
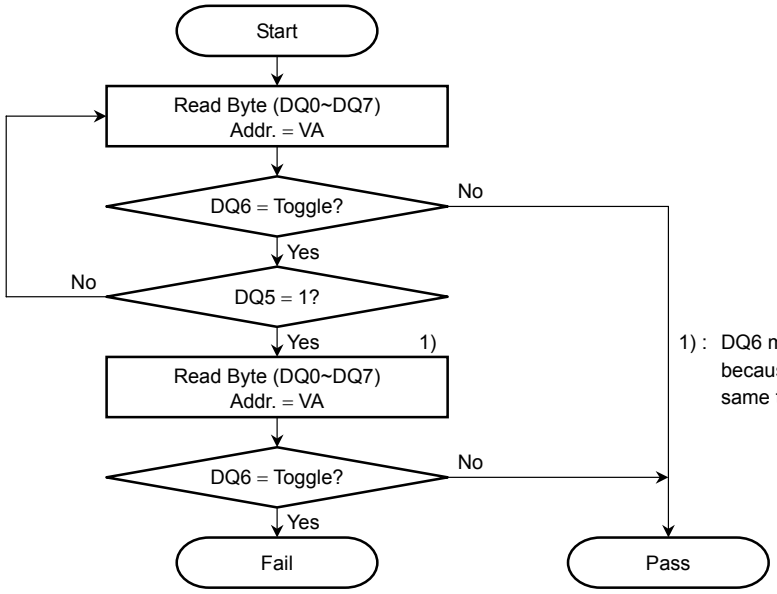
DQ7 $\overline{\text{DATA}}$ Polling



DQ6 Toggle Bit



VA: Valid address for programming
Any of the addresses within the block being erased during a Block Erase operation
"Don't care" during a Chip Erase operation

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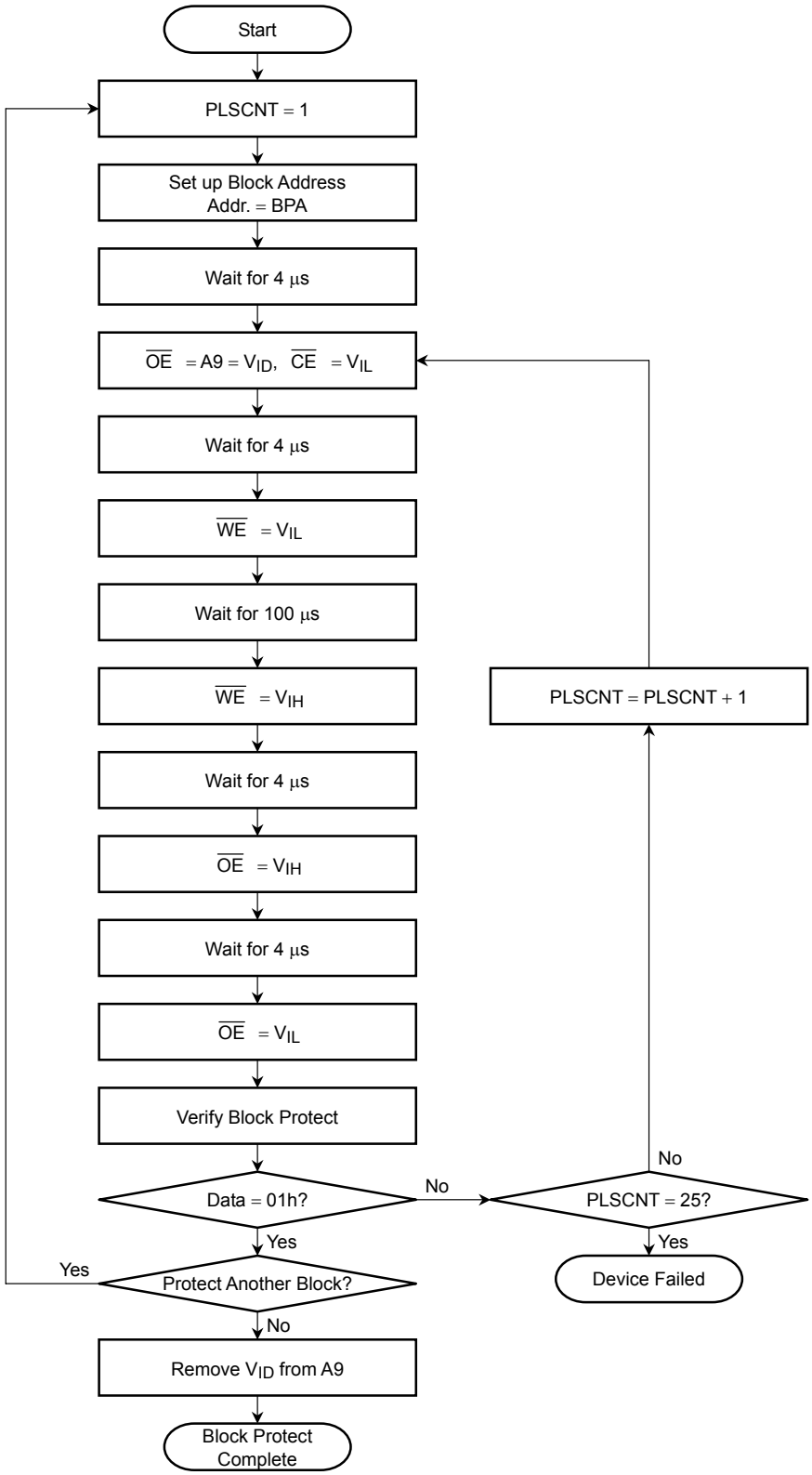
Block Protect 1



BPA: Block Address and ID Read Address (A6, A1, A0)
ID Read Address = (0, 1, 0)

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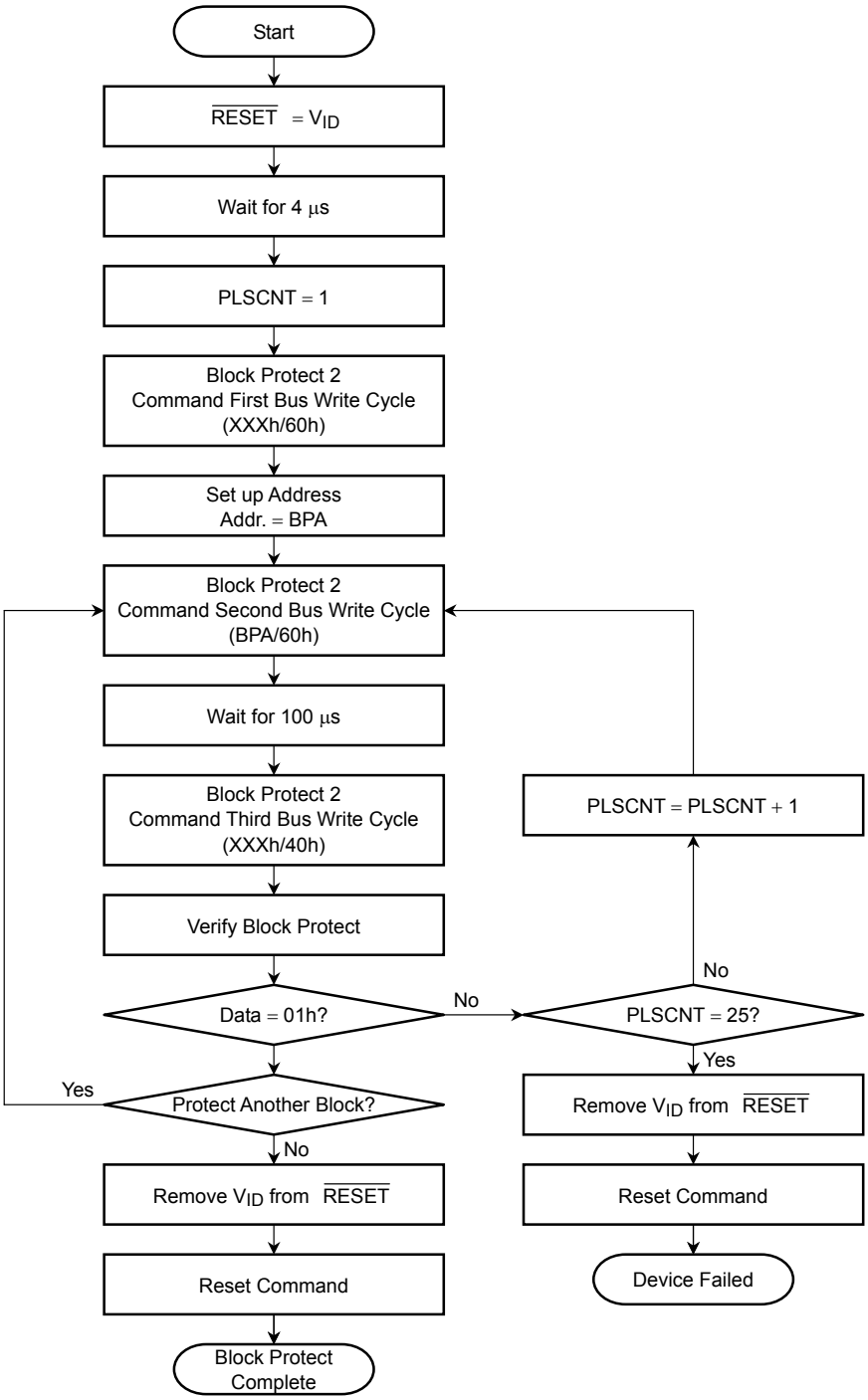
Block Protect 2



BPA: Block Address and ID Read Address (A6, A1, A0)
ID Read Address = (0, 1, 0)

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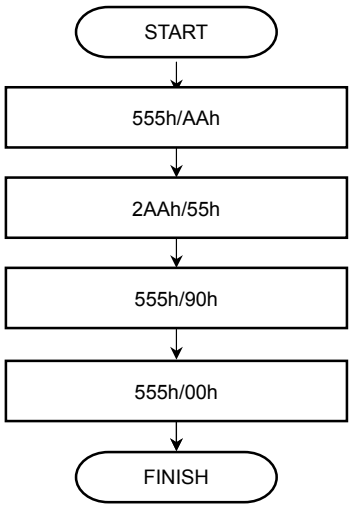
Hidden ROM Exit Command Input



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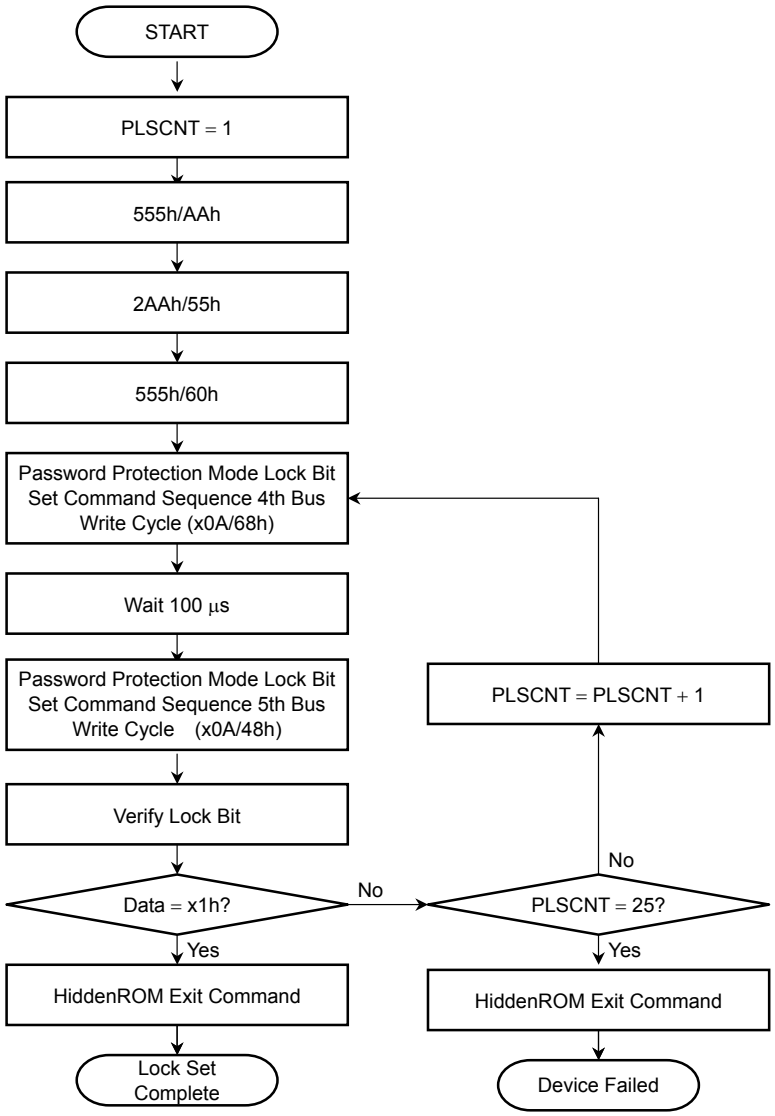
Password Protection Mode Locking Set Operation



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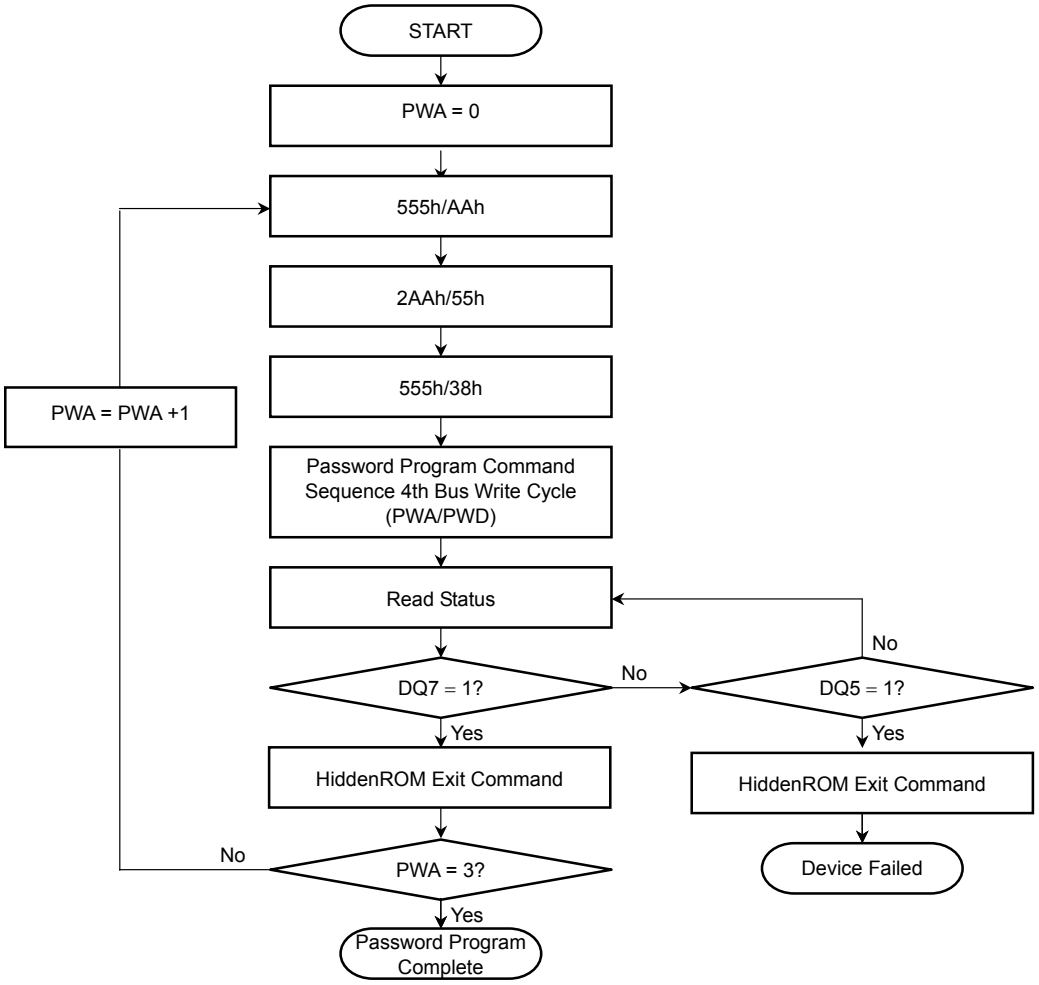
Password Program Operation



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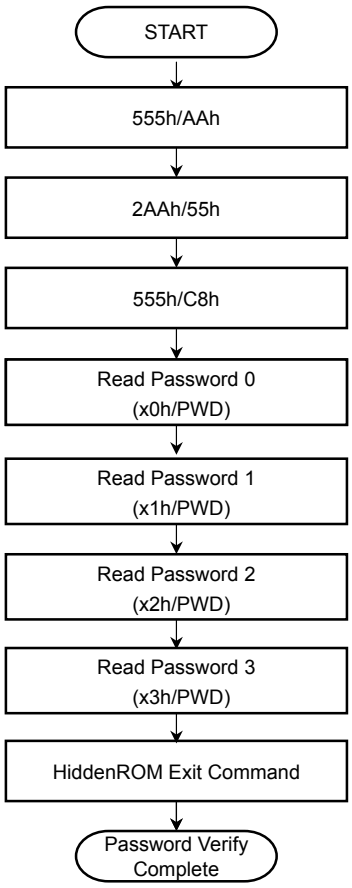
Password Verify Operation



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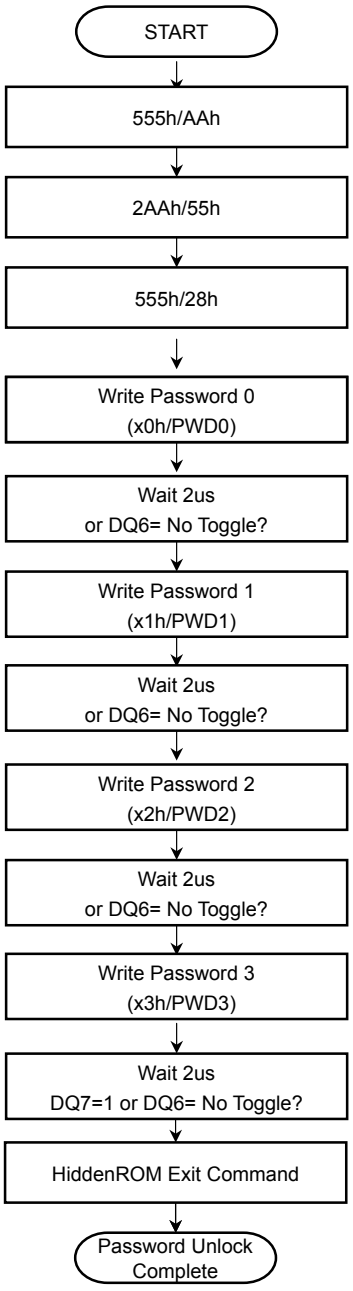
Password Unlock Command Operation



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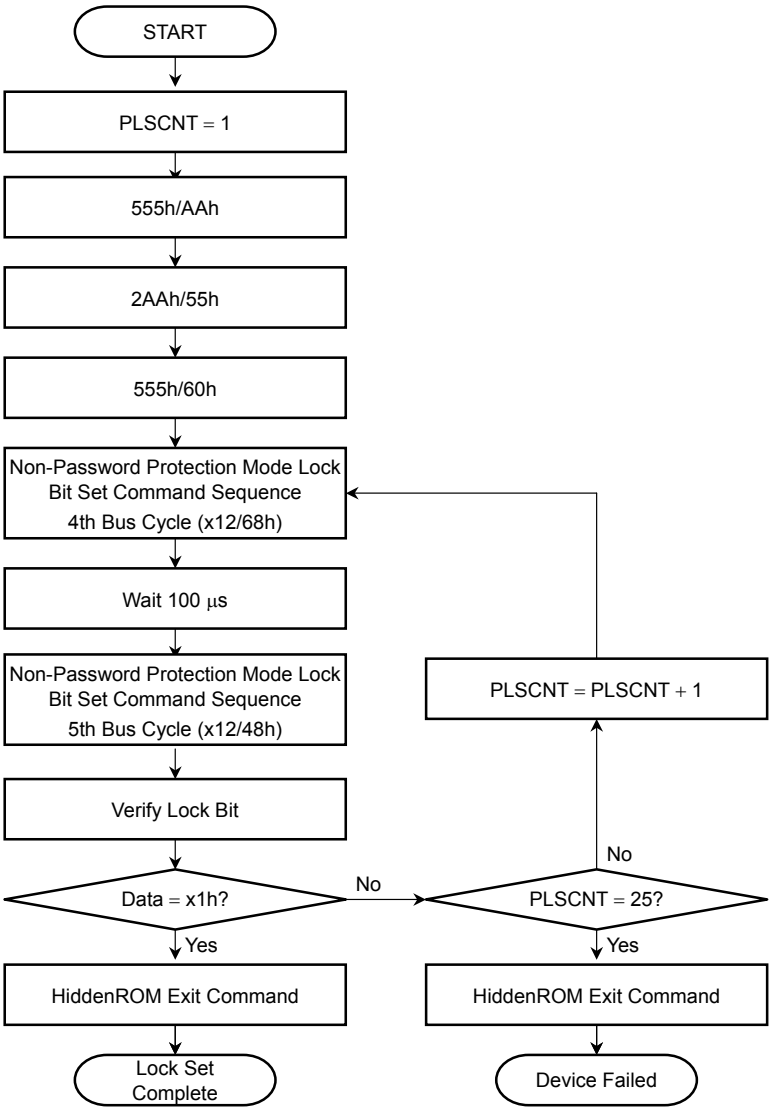
Non-Password Protection Mode Locking Set Operation



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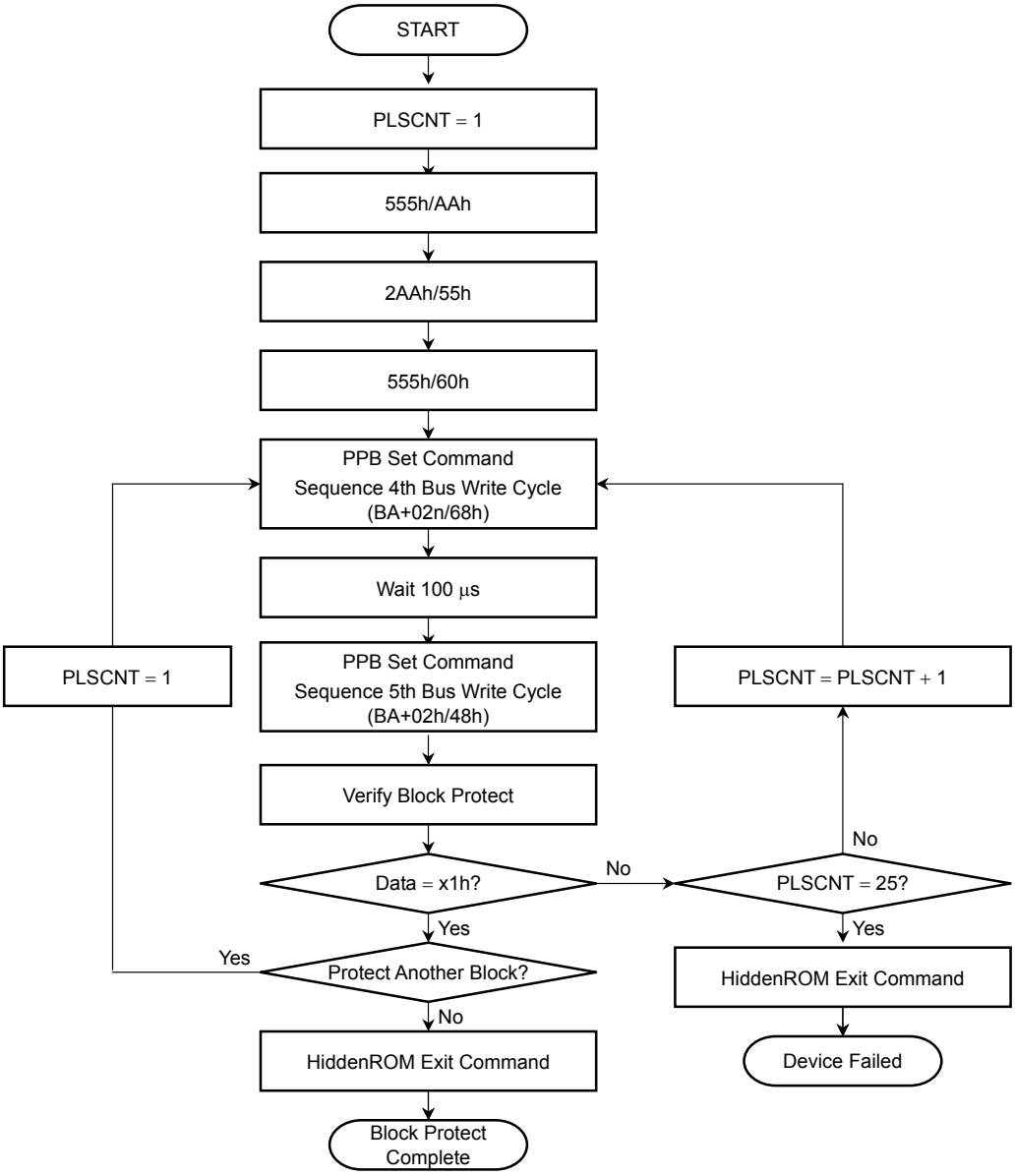
PPB Set Command Sequence



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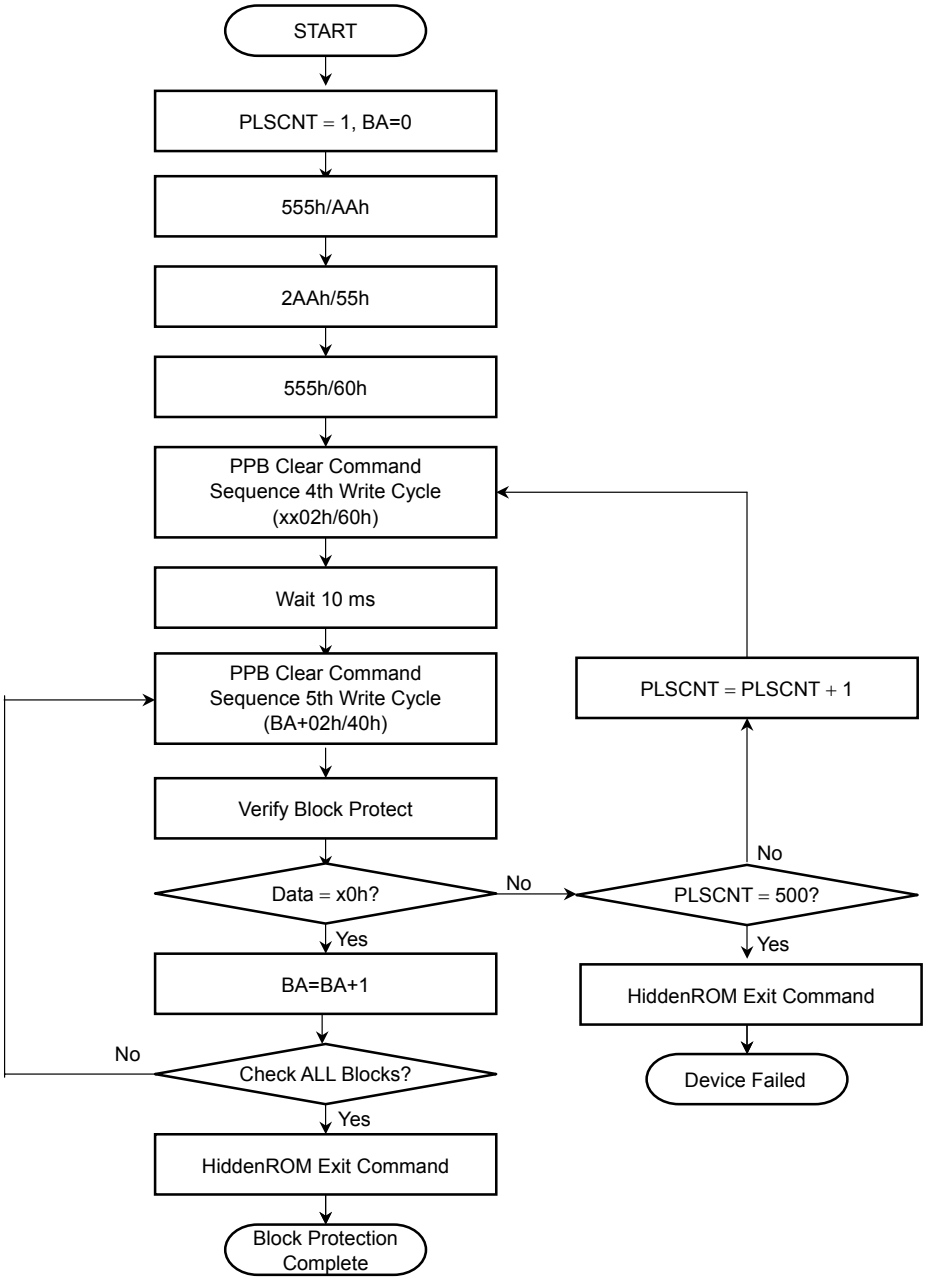
PPB Clear Command Sequence



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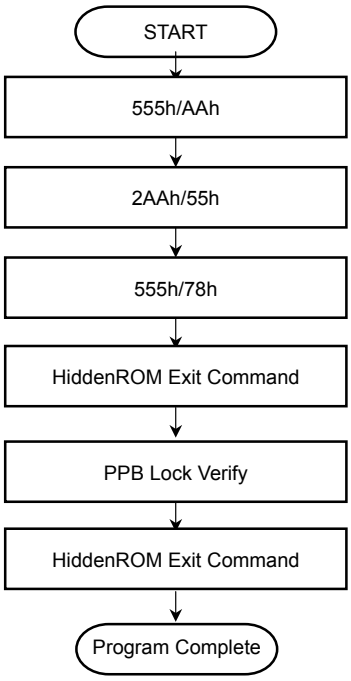
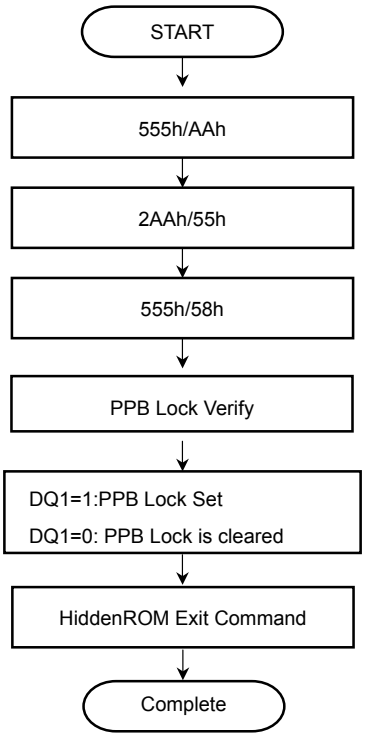
PPB Lock Operation

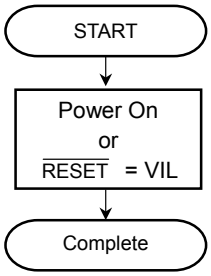
PPB Lock Set



PPB Lock Verify



PPB Lock Clear



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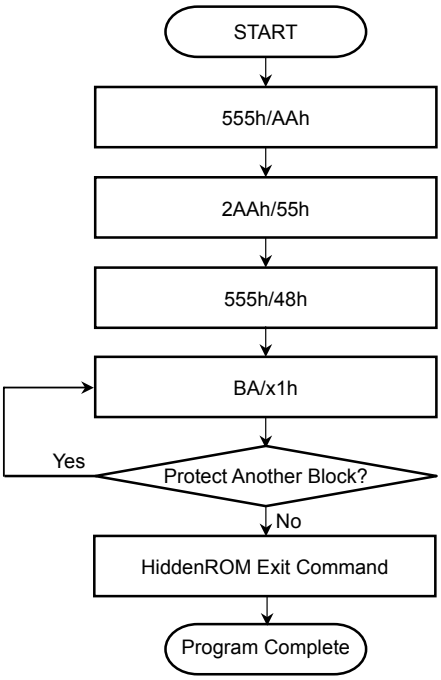
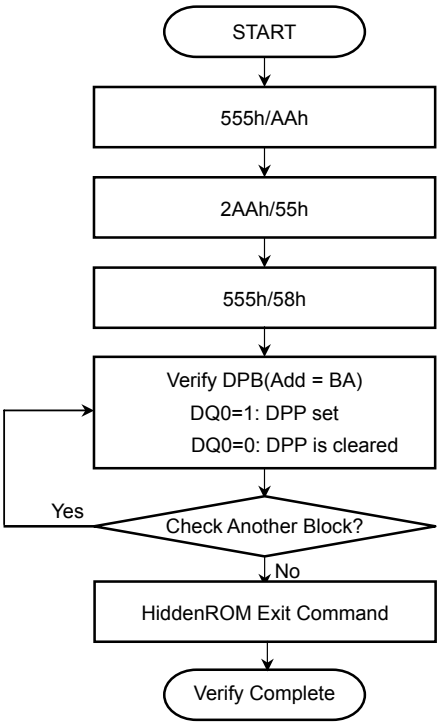
DPB Command Operation

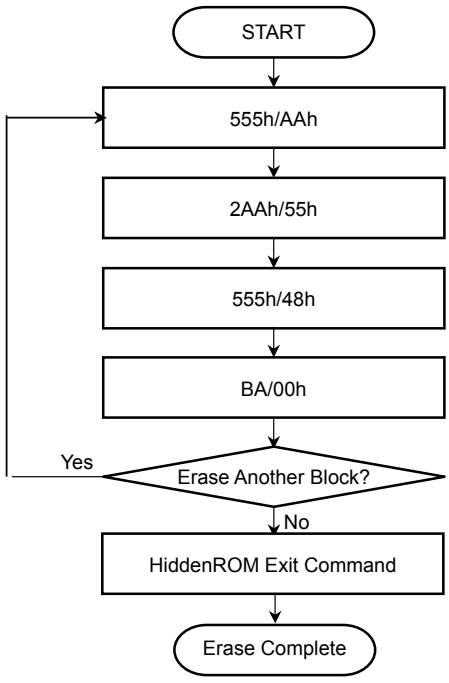
DPB Set



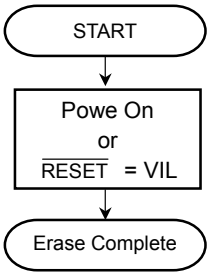
DPB Verify



DPB Clear 1



DPB Clear 2



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20. BLOCK ADDRESS TABLES

* : V_{IH} or V_{IL}

20.1. TC58FVM6T5B (Top Boot Block) 1/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK0	BA0	L	L	L	L	L	L	L	*	*	*	000000h~007FFFh
	BA1	L	L	L	L	L	L	H	*	*	*	008000h~00FFFFh
	BA2	L	L	L	L	L	H	L	*	*	*	010000h~017FFFh
	BA3	L	L	L	L	L	H	H	*	*	*	018000h~01FFFFh
	BA4	L	L	L	L	H	L	L	*	*	*	020000h~027FFFh
	BA5	L	L	L	L	H	L	H	*	*	*	028000h~02FFFFh
	BA6	L	L	L	L	H	H	L	*	*	*	030000h~037FFFh
	BA7	L	L	L	L	H	H	H	*	*	*	038000h~03FFFFh
	BA8	L	L	L	H	L	L	L	*	*	*	040000h~047FFFh
	BA9	L	L	L	H	L	L	H	*	*	*	048000h~04FFFFh
	BA10	L	L	L	H	L	H	L	*	*	*	050000h~057FFFh
	BA11	L	L	L	H	L	H	H	*	*	*	058000h~05FFFFh
	BA12	L	L	L	H	H	L	L	*	*	*	060000h~067FFFh
	BA13	L	L	L	H	H	L	H	*	*	*	068000h~06FFFFh
	BA14	L	L	L	H	H	H	L	*	*	*	070000h~077FFFh
	BA15	L	L	L	H	H	H	H	*	*	*	078000h~07FFFFh
BK1	BA16	L	L	H	L	L	L	L	*	*	*	080000h~087FFFh
	BA17	L	L	H	L	L	L	H	*	*	*	088000h~08FFFFh
	BA18	L	L	H	L	L	H	L	*	*	*	090000h~097FFFh
	BA19	L	L	H	L	L	H	H	*	*	*	098000h~09FFFFh
	BA20	L	L	H	L	H	L	L	*	*	*	0A0000h~0A7FFFh
	BA21	L	L	H	L	H	L	H	*	*	*	0A8000h~0AFFFFh
	BA22	L	L	H	L	H	H	L	*	*	*	0B0000h~0B7FFFh
	BA23	L	L	H	L	H	H	H	*	*	*	0B8000h~0BFFFFh
	BA24	L	L	H	H	L	L	L	*	*	*	0C0000h~0C7FFFh
	BA25	L	L	H	H	L	L	H	*	*	*	0C8000h~0CFFFFh
	BA26	L	L	H	H	L	H	L	*	*	*	0D0000h~0D7FFFh
	BA27	L	L	H	H	L	H	H	*	*	*	0D8000h~0DFFFFh
	BA28	L	L	H	H	H	L	L	*	*	*	0E0000h~0E7FFFh
	BA29	L	L	H	H	H	L	H	*	*	*	0E8000h~0EFFFFh
	BA30	L	L	H	H	H	H	L	*	*	*	0F0000h~0F7FFFh
	BA31	L	L	H	H	H	H	H	*	*	*	0F8000h~0FFFFFh

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20.1. TC58FVM6T5B (Top Boot Block) 2/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK2	BA32	L	H	L	L	L	L	L	*	*	*	100000h~107FFFh
	BA33	L	H	L	L	L	L	H	*	*	*	108000h~10FFFFh
	BA34	L	H	L	L	L	H	L	*	*	*	110000h~117FFFh
	BA35	L	H	L	L	L	H	H	*	*	*	118000h~11FFFFh
	BA36	L	H	L	L	H	L	L	*	*	*	120000h~127FFFh
	BA37	L	H	L	L	H	L	H	*	*	*	128000h~12FFFFh
	BA38	L	H	L	L	H	H	L	*	*	*	130000h~137FFFh
	BA39	L	H	L	L	H	H	H	*	*	*	138000h~13FFFFh
	BA40	L	H	L	H	L	L	L	*	*	*	140000h~147FFFh
	BA41	L	H	L	H	L	L	H	*	*	*	148000h~14FFFFh
	BA42	L	H	L	H	L	H	L	*	*	*	150000h~157FFFh
	BA43	L	H	L	H	L	H	H	*	*	*	158000h~15FFFFh
	BA44	L	H	L	H	H	L	L	*	*	*	160000h~167FFFh
	BA45	L	H	L	H	H	L	H	*	*	*	168000h~16FFFFh
	BA46	L	H	L	H	H	H	L	*	*	*	170000h~177FFFh
	BA47	L	H	L	H	H	H	H	*	*	*	178000h~17FFFFh
BK3	BA48	L	H	H	L	L	L	L	*	*	*	180000h~187FFFh
	BA49	L	H	H	L	L	L	H	*	*	*	188000h~18FFFFh
	BA50	L	H	H	L	L	H	L	*	*	*	190000h~197FFFh
	BA51	L	H	H	L	L	H	H	*	*	*	198000h~19FFFFh
	BA52	L	H	H	L	H	L	L	*	*	*	1A0000h~1A7FFFh
	BA53	L	H	H	L	H	L	H	*	*	*	1A8000h~1AFFFFh
	BA54	L	H	H	L	H	H	L	*	*	*	1B0000h~1B7FFFh
	BA55	L	H	H	L	H	H	H	*	*	*	1B8000h~1BFFFFh
	BA56	L	H	H	H	L	L	L	*	*	*	1C0000h~1C7FFFh
	BA57	L	H	H	H	L	L	H	*	*	*	1C8000h~1CFFFFh
	BA58	L	H	H	H	L	H	L	*	*	*	1D0000h~1D7FFFh
	BA59	L	H	H	H	L	H	H	*	*	*	1D8000h~1DFFFFh
	BA60	L	H	H	H	H	L	L	*	*	*	1E0000h~1E7FFFh
	BA61	L	H	H	H	H	L	H	*	*	*	1E8000h~1EFFFFh
	BA62	L	H	H	H	H	H	L	*	*	*	1F0000h~1F7FFFh
	BA63	L	H	H	H	H	H	H	*	*	*	1F8000h~1FFFFFh

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20.1. TC58FVM6T5B (Top Boot Block) 3/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK4	BA64	H	L	L	L	L	L	L	*	*	*	200000h~207FFFh
	BA65	H	L	L	L	L	L	H	*	*	*	208000h~20FFFFh
	BA66	H	L	L	L	L	H	L	*	*	*	210000h~217FFFh
	BA67	H	L	L	L	L	H	H	*	*	*	218000h~21FFFFh
	BA68	H	L	L	L	H	L	L	*	*	*	220000h~227FFFh
	BA69	H	L	L	L	H	L	H	*	*	*	228000h~22FFFFh
	BA70	H	L	L	L	H	H	L	*	*	*	230000h~237FFFh
	BA71	H	L	L	L	H	H	H	*	*	*	238000h~23FFFFh
	BA72	H	L	L	H	L	L	L	*	*	*	240000h~247FFFh
	BA73	H	L	L	H	L	L	H	*	*	*	248000h~24FFFFh
	BA74	H	L	L	H	L	H	L	*	*	*	250000h~257FFFh
	BA75	H	L	L	H	L	H	H	*	*	*	258000h~25FFFFh
	BA76	H	L	L	H	H	L	L	*	*	*	260000h~267FFFh
	BA77	H	L	L	H	H	L	H	*	*	*	268000h~26FFFFh
	BA78	H	L	L	H	H	H	L	*	*	*	270000h~277FFFh
	BA79	H	L	L	H	H	H	H	*	*	*	278000h~27FFFFh
BK5	BA80	H	L	H	L	L	L	L	*	*	*	280000h~287FFFh
	BA81	H	L	H	L	L	L	H	*	*	*	288000h~28FFFFh
	BA82	H	L	H	L	L	H	L	*	*	*	290000h~297FFFh
	BA83	H	L	H	L	L	H	H	*	*	*	298000h~29FFFFh
	BA84	H	L	H	L	H	L	L	*	*	*	2A0000h~2A7FFFh
	BA85	H	L	H	L	H	L	H	*	*	*	2A8000h~2AFFFFh
	BA86	H	L	H	L	H	H	L	*	*	*	2B0000h~2B7FFFh
	BA87	H	L	H	L	H	H	H	*	*	*	2B8000h~2BFFFFh
	BA88	H	L	H	H	L	L	L	*	*	*	2C0000h~2C7FFFh
	BA89	H	L	H	H	L	L	H	*	*	*	2C8000h~2CFFFFh
	BA90	H	L	H	H	L	H	L	*	*	*	2D0000h~2D7FFFh
	BA91	H	L	H	H	L	H	H	*	*	*	2D8000h~2DFFFFh
	BA92	H	L	H	H	H	L	L	*	*	*	2E0000h~2E7FFFh
	BA93	H	L	H	H	H	L	H	*	*	*	2E8000h~2EFFFFh
	BA94	H	L	H	H	H	H	L	*	*	*	2F0000h~2F7FFFh
	BA95	H	L	H	H	H	H	H	*	*	*	2F8000h~2FFFFFh

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20.1. TC58FVM6T5B (Top Boot Block) 4/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK6	BA96	H	H	L	L	L	L	L	*	*	*	300000h~307FFFh
	BA97	H	H	L	L	L	L	H	*	*	*	308000h~30FFFFh
	BA98	H	H	L	L	L	H	L	*	*	*	310000h~317FFFh
	BA99	H	H	L	L	L	H	H	*	*	*	318000h~31FFFFh
	BA100	H	H	L	L	H	L	L	*	*	*	320000h~327FFFh
	BA101	H	H	L	L	H	L	H	*	*	*	328000h~32FFFFh
	BA102	H	H	L	L	H	H	L	*	*	*	330000h~337FFFh
	BA103	H	H	L	L	H	H	H	*	*	*	338000h~33FFFFh
	BA104	H	H	L	H	L	L	L	*	*	*	340000h~347FFFh
	BA105	H	H	L	H	L	L	H	*	*	*	348000h~34FFFFh
	BA106	H	H	L	H	L	H	L	*	*	*	350000h~357FFFh
	BA107	H	H	L	H	L	H	H	*	*	*	358000h~35FFFFh
	BA108	H	H	L	H	H	L	L	*	*	*	360000h~367FFFh
	BA109	H	H	L	H	H	L	H	*	*	*	368000h~36FFFFh
	BA110	H	H	L	H	H	H	L	*	*	*	370000h~377FFFh
	BA111	H	H	L	H	H	H	H	*	*	*	378000h~37FFFFh
BK7	BA112	H	H	H	L	L	L	L	*	*	*	380000h~387FFFh
	BA113	H	H	H	L	L	L	H	*	*	*	388000h~38FFFFh
	BA114	H	H	H	L	L	H	L	*	*	*	390000h~397FFFh
	BA115	H	H	H	L	L	H	H	*	*	*	398000h~39FFFFh
	BA116	H	H	H	L	H	L	L	*	*	*	3A0000h~3A7FFFh
	BA117	H	H	H	L	H	L	H	*	*	*	3A8000h~3AFFFFh
	BA118	H	H	H	L	H	H	L	*	*	*	3B0000h~3B7FFFh
	BA119	H	H	H	L	H	H	H	*	*	*	3B8000h~3BFFFFh
	BA120	H	H	H	H	L	L	L	*	*	*	3C0000h~3C7FFFh
	BA121	H	H	H	H	L	L	H	*	*	*	3C8000h~3CFFFFh
	BA122	H	H	H	H	L	H	L	*	*	*	3D0000h~3D7FFFh
	BA123	H	H	H	H	L	H	H	*	*	*	3D8000h~3DFFFFh
	BA124	H	H	H	H	H	L	L	*	*	*	3E0000h~3E7FFFh
	BA125	H	H	H	H	H	L	H	*	*	*	3E8000h~3EFFFFh
	BA126	H	H	H	H	H	H	L	*	*	*	3F0000h~3F7FFFh
	BA127	H	H	H	H	H	H	H	*	*	*	3F8000h~3FFFFFh

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20.1. TC58FVM6T5B (Top Boot Block) 5/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK7	BA127	H	H	H	H	H	H	H	L	L	L	3F8000h~3F8FFFh
	BA128	H	H	H	H	H	H	H	L	L	H	3F9000h~3F9FFFh
	BA129	H	H	H	H	H	H	H	L	H	L	3FA000h~3FAFFFh
	BA130	H	H	H	H	H	H	H	L	H	H	3FB000h~3FBFFFh
	BA131	H	H	H	H	H	H	H	H	L	L	3FC000h~3FCFFFh
	BA132	H	H	H	H	H	H	H	H	L	H	3FD000h~3FDFFFh
	BA133	H	H	H	H	H	H	H	H	H	L	3FE000h~3FEFFFh
	BA134	H	H	H	H	H	H	H	H	H	H	3FF000h~3FFFFFh

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20.2. TC58FVM6B5B (Bottom Boot Block) 1/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK0	BA0	L	L	L	L	L	L	L	L	L	L	000000h~000FFFh
	BA1	L	L	L	L	L	L	L	L	L	H	001000h~001FFFh
	BA2	L	L	L	L	L	L	L	L	H	L	002000h~002FFFh
	BA3	L	L	L	L	L	L	L	L	H	H	003000h~003FFFh
	BA4	L	L	L	L	L	L	L	H	L	L	004000h~004FFFh
	BA5	L	L	L	L	L	L	L	H	L	H	005000h~005FFFh
	BA6	L	L	L	L	L	L	L	H	H	L	006000h~006FFFh
	BA7	L	L	L	L	L	L	L	H	H	H	007000h~007FFFh

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20.2. TC58FVM6B5B (Bottom Boot Block) 2/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK0	BA8	L	L	L	L	L	L	H	*	*	*	008000h~00FFFFh
	BA9	L	L	L	L	L	H	L	*	*	*	010000h~017FFFh
	BA10	L	L	L	L	L	H	H	*	*	*	018000h~01FFFFh
	BA11	L	L	L	L	H	L	L	*	*	*	020000h~027FFFh
	BA12	L	L	L	L	H	L	H	*	*	*	028000h~02FFFFh
	BA13	L	L	L	L	H	H	L	*	*	*	030000h~037FFFh
	BA14	L	L	L	L	H	H	H	*	*	*	038000h~03FFFFh
	BA15	L	L	L	H	L	L	L	*	*	*	040000h~047FFFh
	BA16	L	L	L	H	L	L	H	*	*	*	048000h~04FFFFh
	BA17	L	L	L	H	L	H	L	*	*	*	050000h~057FFFh
	BA18	L	L	L	H	L	H	H	*	*	*	058000h~05FFFFh
	BA19	L	L	L	H	H	L	L	*	*	*	060000h~067FFFh
	BA20	L	L	L	H	H	L	H	*	*	*	068000h~06FFFFh
	BA21	L	L	L	H	H	H	L	*	*	*	070000h~077FFFh
	BA22	L	L	L	H	H	H	H	*	*	*	078000h~07FFFFh
BK1	BA23	L	L	H	L	L	L	L	*	*	*	080000h~087FFFh
	BA24	L	L	H	L	L	L	H	*	*	*	088000h~08FFFFh
	BA25	L	L	H	L	L	H	L	*	*	*	090000h~097FFFh
	BA26	L	L	H	L	L	H	H	*	*	*	098000h~09FFFFh
	BA27	L	L	H	L	H	L	L	*	*	*	0A0000h~0A7FFFh
	BA28	L	L	H	L	H	L	H	*	*	*	0A8000h~0AFFFFh
	BA29	L	L	H	L	H	H	L	*	*	*	0B0000h~0B7FFFh
	BA30	L	L	H	L	H	H	H	*	*	*	0B8000h~0BFFFFh
	BA31	L	L	H	H	L	L	L	*	*	*	0C0000h~0C7FFFh
	BA32	L	L	H	H	L	L	H	*	*	*	0C8000h~0CFFFFh
	BA33	L	L	H	H	L	H	L	*	*	*	0D0000h~0D7FFFh
	BA34	L	L	H	H	L	H	H	*	*	*	0D8000h~0DFFFFh
	BA35	L	L	H	H	H	L	L	*	*	*	0E0000h~0E7FFFh
	BA36	L	L	H	H	H	L	H	*	*	*	0E8000h~0EFFFFh
	BA37	L	L	H	H	H	H	L	*	*	*	0F0000h~0F7FFFh
	BA38	L	L	H	H	H	H	H	*	*	*	0F8000h~0FFFFFh

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20.2. TC58FVM6B5B (Bottom Boot Block) 3/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK2	BA39	L	H	L	L	L	L	L	*	*	*	100000h~107FFFh
	BA40	L	H	L	L	L	L	H	*	*	*	108000h~10FFFFh
	BA41	L	H	L	L	L	H	L	*	*	*	110000h~117FFFh
	BA42	L	H	L	L	L	H	H	*	*	*	118000h~11FFFFh
	BA43	L	H	L	L	H	L	L	*	*	*	120000h~127FFFh
	BA44	L	H	L	L	H	L	H	*	*	*	128000h~12FFFFh
	BA45	L	H	L	L	H	H	L	*	*	*	130000h~137FFFh
	BA46	L	H	L	L	H	H	H	*	*	*	138000h~13FFFFh
	BA47	L	H	L	H	L	L	L	*	*	*	140000h~147FFFh
	BA48	L	H	L	H	L	L	H	*	*	*	148000h~14FFFFh
	BA49	L	H	L	H	L	H	L	*	*	*	150000h~157FFFh
	BA50	L	H	L	H	L	H	H	*	*	*	158000h~15FFFFh
	BA51	L	H	L	H	H	L	L	*	*	*	160000h~167FFFh
	BA52	L	H	L	H	H	L	H	*	*	*	168000h~16FFFFh
	BA53	L	H	L	H	H	H	L	*	*	*	170000h~177FFFh
	BA54	L	H	L	H	H	H	H	*	*	*	178000h~17FFFFh
BK3	BA55	L	H	H	L	L	L	L	*	*	*	180000h~187FFFh
	BA56	L	H	H	L	L	L	H	*	*	*	188000h~18FFFFh
	BA57	L	H	H	L	L	H	L	*	*	*	190000h~197FFFh
	BA58	L	H	H	L	L	H	H	*	*	*	198000h~19FFFFh
	BA59	L	H	H	L	H	L	L	*	*	*	1A0000h~1A7FFFh
	BA60	L	H	H	L	H	L	H	*	*	*	1A8000h~1AFFFFh
	BA61	L	H	H	L	H	H	L	*	*	*	1B0000h~1B7FFFh
	BA62	L	H	H	L	H	H	H	*	*	*	1B8000h~1BFFFFh
	BA63	L	H	H	H	L	L	L	*	*	*	1C0000h~1C7FFFh
	BA64	L	H	H	H	L	L	H	*	*	*	1C8000h~1CFFFFh
	BA65	L	H	H	H	L	H	L	*	*	*	1D0000h~1D7FFFh
	BA66	L	H	H	H	L	H	H	*	*	*	1D8000h~1DFFFFh
	BA67	L	H	H	H	H	L	L	*	*	*	1E0000h~1E7FFFh
	BA68	L	H	H	H	H	L	H	*	*	*	1E8000h~1EFFFFh
	BA69	L	H	H	H	H	H	L	*	*	*	1F0000h~1F7FFFh
	BA70	L	H	H	H	H	H	H	*	*	*	1F8000h~1FFFFFh

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20.2. TC58FVM6B5B (Bottom Boot Block) 4/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK4	BA71	H	L	L	L	L	L	L	*	*	*	200000h~207FFFh
	BA72	H	L	L	L	L	L	H	*	*	*	208000h~20FFFFh
	BA73	H	L	L	L	L	H	L	*	*	*	210000h~217FFFh
	BA74	H	L	L	L	L	H	H	*	*	*	218000h~21FFFFh
	BA75	H	L	L	L	H	L	L	*	*	*	220000h~227FFFh
	BA76	H	L	L	L	H	L	H	*	*	*	228000h~22FFFFh
	BA77	H	L	L	L	H	H	L	*	*	*	230000h~237FFFh
	BA78	H	L	L	L	H	H	H	*	*	*	238000h~23FFFFh
	BA79	H	L	L	H	L	L	L	*	*	*	240000h~247FFFh
	BA80	H	L	L	H	L	L	H	*	*	*	248000h~24FFFFh
	BA81	H	L	L	H	L	H	L	*	*	*	250000h~257FFFh
	BA82	H	L	L	H	L	H	H	*	*	*	258000h~25FFFFh
	BA83	H	L	L	H	H	L	L	*	*	*	260000h~267FFFh
	BA84	H	L	L	H	H	L	H	*	*	*	268000h~26FFFFh
	BA85	H	L	L	H	H	H	L	*	*	*	270000h~277FFFh
	BA86	H	L	L	H	H	H	H	*	*	*	278000h~27FFFFh
BK5	BA87	H	L	H	L	L	L	L	*	*	*	280000h~287FFFh
	BA88	H	L	H	L	L	L	H	*	*	*	288000h~28FFFFh
	BA89	H	L	H	L	L	H	L	*	*	*	290000h~297FFFh
	BA90	H	L	H	L	L	H	H	*	*	*	298000h~29FFFFh
	BA91	H	L	H	L	H	L	L	*	*	*	2A0000h~2A7FFFh
	BA92	H	L	H	L	H	L	H	*	*	*	2A8000h~2AFFFFh
	BA93	H	L	H	L	H	H	L	*	*	*	2B0000h~2B7FFFh
	BA94	H	L	H	L	H	H	H	*	*	*	2B8000h~2BFFFFh
	BA95	H	L	H	H	L	L	L	*	*	*	2C0000h~2C7FFFh
	BA96	H	L	H	H	L	L	H	*	*	*	2C8000h~2CFFFFh
	BA97	H	L	H	H	L	H	L	*	*	*	2D0000h~2D7FFFh
	BA98	H	L	H	H	L	H	H	*	*	*	2D8000h~2DFFFFh
	BA99	H	L	H	H	H	L	L	*	*	*	2E0000h~2E7FFFh
	BA100	H	L	H	H	H	L	H	*	*	*	2E8000h~2EFFFFh
	BA101	H	L	H	H	H	H	L	*	*	*	2F0000h~2F7FFFh
	BA102	H	L	H	H	H	H	H	*	*	*	2F8000h~2FFFFFh

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20.2. TC58FVM6B5B (Bottom Boot Block) 5/5

BANK #	BLOCK #	BLOCK ADDRESS										ADDRESS RANGE
		BANK ADDRESS										
		A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	
BK6	BA103	H	H	L	L	L	L	L	*	*	*	300000h~307FFFh
	BA104	H	H	L	L	L	L	H	*	*	*	308000h~30FFFFh
	BA105	H	H	L	L	L	H	L	*	*	*	310000h~317FFFh
	BA106	H	H	L	L	L	H	H	*	*	*	318000h~31FFFFh
	BA107	H	H	L	L	H	L	L	*	*	*	320000h~327FFFh
	BA108	H	H	L	L	H	L	H	*	*	*	328000h~32FFFFh
	BA109	H	H	L	L	H	H	L	*	*	*	330000h~337FFFh
	BA110	H	H	L	L	H	H	H	*	*	*	338000h~33FFFFh
	BA111	H	H	L	H	L	L	L	*	*	*	340000h~347FFFh
	BA112	H	H	L	H	L	L	H	*	*	*	348000h~34FFFFh
	BA113	H	H	L	H	L	H	L	*	*	*	350000h~357FFFh
	BA114	H	H	L	H	L	H	H	*	*	*	358000h~35FFFFh
	BA115	H	H	L	H	H	L	L	*	*	*	360000h~367FFFh
	BA116	H	H	L	H	H	L	H	*	*	*	368000h~36FFFFh
	BA117	H	H	L	H	H	H	L	*	*	*	370000h~377FFFh
	BA118	H	H	L	H	H	H	H	*	*	*	378000h~37FFFFh
BK7	BA119	H	H	H	L	L	L	L	*	*	*	380000h~387FFFh
	BA120	H	H	H	L	L	L	H	*	*	*	388000h~38FFFFh
	BA121	H	H	H	L	L	H	L	*	*	*	390000h~397FFFh
	BA122	H	H	H	L	L	H	H	*	*	*	398000h~39FFFFh
	BA123	H	H	H	L	H	L	L	*	*	*	3A0000h~3A7FFFh
	BA124	H	H	H	L	H	L	H	*	*	*	3A8000h~3AFFFFh
	BA125	H	H	H	L	H	H	L	*	*	*	3B0000h~3B7FFFh
	BA126	H	H	H	L	H	H	H	*	*	*	3B8000h~3BFFFFh
	BA127	H	H	H	H	L	L	L	*	*	*	3C0000h~3C7FFFh
	BA128	H	H	H	H	L	L	H	*	*	*	3C8000h~3CFFFFh
	BA129	H	H	H	H	L	H	L	*	*	*	3D0000h~3D7FFFh
	BA130	H	H	H	H	L	H	H	*	*	*	3D8000h~3DFFFFh
	BA131	H	H	H	H	H	L	L	*	*	*	3E0000h~3E7FFFh
	BA132	H	H	H	H	H	L	H	*	*	*	3E8000h~3EFFFFh
	BA133	H	H	H	H	H	H	L	*	*	*	3F0000h~3F7FFFh
	BA134	H	H	H	H	H	H	H	*	*	*	3F8000h~3FFFFFh

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21. BLOCK SIZE TABLE

21.1. TC58FVM6T5B (Top Boot Block)

BLOCK #	BLOCK SIZE	BANK #	BANK SIZE	BLOCK COUNT
BA0~BA15	32 Kwords x 16	BK0	512 Kwords	16
BA16~BA31	32 Kwords x 16	BK1	512 Kwords	16
BA32~BA47	32 Kwords x 16	BK2	512 Kwords	16
BA48~BA63	32 Kwords x 16	BK3	512 Kwords	16
BA64~BA79	32 Kwords x 16	BK4	512 Kwords	16
BA80~BA95	32 Kwords x 16	BK5	512 Kwords	16
BA96~BA111	32 Kwords x 16	BK6	512 Kwords	16
BA112~BA134	32 Kwords x 15 + 4 Kwords x 8	BK7	512 Kwords	23

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21.2. TC58FVM6B5B (Bottom Boot Block)

BLOCK #	BLOCK SIZE	BANK #	BANK SIZE	BLOCK COUNT
BA0~BA22	32 Kwords x 15 + 4 Kwords x 8	BK0	512 Kwords	23
BA23~BA38	32 Kwords x 16	BK1	512 Kwords	16
BA39~BA54	32 Kwords x 16	BK2	512 Kwords	16
BA55~BA70	32 Kwords x 16	BK3	512 Kwords	16
BA71~BA86	32 Kwords x 16	BK4	512 Kwords	16
BA87~BA102	32 Kwords x 16	BK5	512 Kwords	16
BA103~BA118	32 Kwords x 16	BK6	512 Kwords	16
BA119~BA134	32 Kwords x 16	BK7	512 Kwords	16

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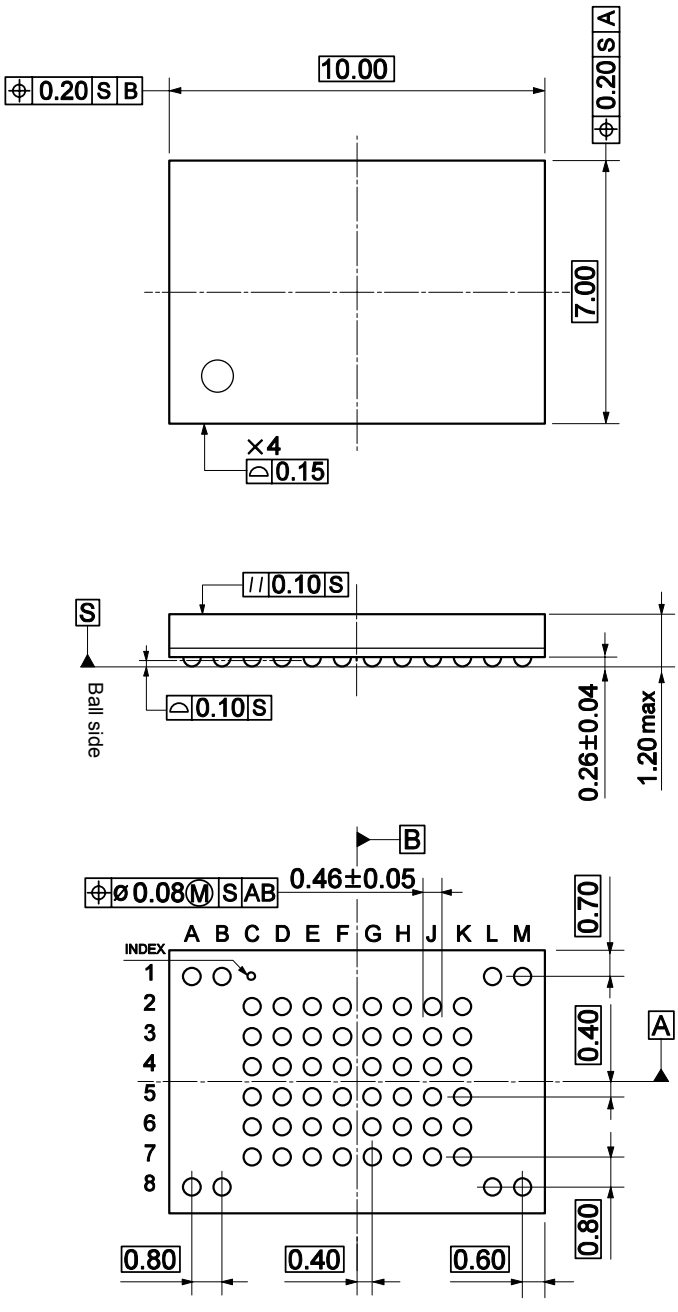
22. PACKAGE DIMENSIONS

Unit: mm

P-TFBGA56-0710-0.80DZ



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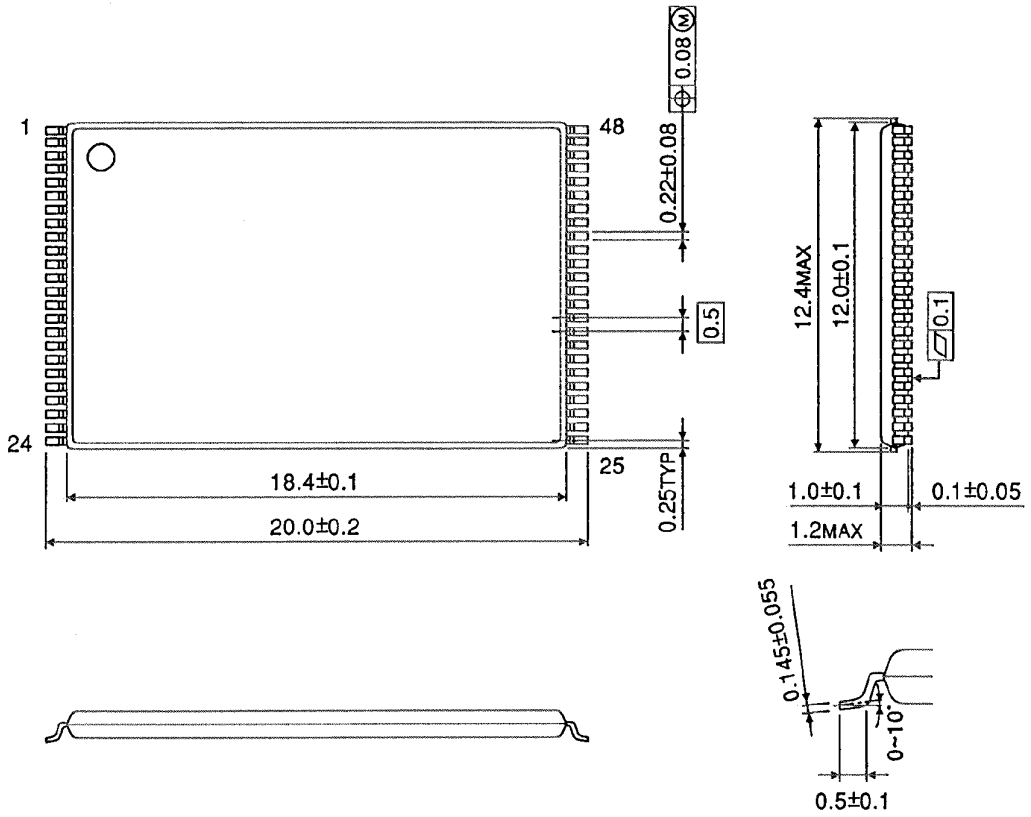
Unit: mm

TSOPI48-P-1220-0.50



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23. REVISION HISTORY

Date	Rev.	Description
2004-07-22	1.00	Original version
2004-09-06	1.01	Change of the address which makes password unlock possible.
2004-10-04	1.02	The state of the RDY pin in password mode is added.
2004-11-08	1.03	Changed Specification (tSUSP)
2004-11-17	1.04	Changed the Hidden Rom Exit Address.
2005-01-11	1.05	Changed Specification (tSUSE/tREADY/tPPAW)
2005-02-28	1.06	Changed an explanation of Simultaneous Read/Write Operation (p.9), and Package Dimensions of TFGBA.
2005-06-24	1.07	Changed Specification (VDD)
2005-08-02	1.08	Added Specification of Pin Capacitance. ($\overline{\text{WP}}$/ACC)
2005-08-22	1.09	Added timing diagrams.
2005-08-29	1.10	Changed TSOP package name. (p.1)
2006-02-23	1.11	Comment addition of "Lead-Free". (p.1)
2006-05-10	1.12	Correct comment of Program Suspend/Resume and Erase Suspend/Resume.

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