3 Volt Intel StrataFlash® Memory

28F128J3A, 28F640J3A, 28F320J3A

Specification Update

April 2002

Notice: The 28F128J3A, 28F640J3A, and 28F320J3A may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in this specification update.

Order Number: 298130-014

Downloaded from Elcodis.com electronic components distributor

Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at http://www.intel.com.

Copyright © Intel Corporation, 2002

AlertVIEW, i960, AnyPoint, AppChoice, BoardWatch, BunnyPeople, CablePort, Celeron, Chips, Commerce Cart, CT Connect, CT Media, Dialogic, DM3, EtherExpress, ETOX, FlashFile, GatherRound, i386, i486, iCat, iCOMP, Insight960, InstantIP, Intel, Intel logo, Intel386, Intel486, Intel740, IntelDX2, IntelDX4, IntelSX2, Intel ChatPad, Intel Create&Share, Intel Dot.Station, Intel GigaBlade, Intel InBusiness, Intel Inside, Intel Inside logo, Intel NetBurst, Intel NetStructure, Intel Play, Intel Play logo, Intel Pocket Concert, Intel SingleDriver, Intel SpeedStep, Intel StrataFlash, Intel TeamStation, Intel WebOutfitter, Intel Xeon, Intel XScale, Itanium, JobAnalyst, LANDesk, LanRover, MCS, MMX, MMX logo, NetPort, NetportExpress, Optimizer logo, OverDrive, Paragon, PC Dads, PC Parents, Pentium, Pentium II Xeon, Pentium III Xeon, Performance at Your Command, ProShare, RemoteExpress, Screamline, Shiva, SmartDie, Solutions960, Sound Mark, StorageExpress, The Computer Inside, The Journey Inside, This Way In, TokenExpress, Trillium, Vivonic, and VTune are trademarks or registered trademarks of Intel Corporation or its subsidiaries in the United States and other countries.

*Other names and brands may be claimed as the property of others.

Downloaded from Elcodis.com electronic components distributor

Contents

Downloaded from Elcodis.com electronic components distributor

Downloaded from Elcodis.com electronic components distributor

Revision History

Date	Version	Description
07/07/99	-001	Original version
07/27/99	-002	First public release (Document includes all known errata and specification changes to date.)
10/28/99	-003	Added A-3 Stepping and Errata Added: Erratum #6, *Read Parameter* t_{ELQX} Added: Erratum #7, *Read Parameter* t_{ELAV} Added: Erratum #8, *Read Parameter* t_{ELQV} deleted
12/09/99	-004	Specification Change: 5 Volt I/O operation removed
03/21/00	-005	Changed: Component Ordering Specifications Added: FPO Mark Identification Added: Erratum #9, *Write Parameter* t_{WHRL} Added: Erratum #10, *Erase Suspend Latency* t_{WHRH} Added: Erratum #11, *Erase Suspend* Changed: Erratum #5 Operating Temperature Range Added: Specification Change #6, *Operating Temperature Range* Added: Specification Change #7, I_{CCR} Added: Specification Change #8, *Program and Erase Time* with changes to Write Buffer, Block Program, Byte Program and Max Erase Time specifications Added: Specification Change #9, *Block Lock-Bit and Clear Times* with changes to the Clear Lock-Bit and Set Lock-Bit specifications Added: Specification Clarification #1, *Set Read Configuration Command*
04/17/00	-006	Split Erratum #11 into two Errata Added: Erratum #12, *Erase Suspend 2* Updated Errata tables to reflect correct Errata conditions based on FPO mark Updated Component Ordering Specifications
07/17/00	-007	Changed: Component Ordering Specifications Added: Erratum #13, *Program Suspend Latency* t_{WHRH1} Corrected Specification Change #2, typical erase time should be 1.0 sec Corrected Specification Change #8, max program time value should be 2.4 sec, typical erase time should be 1.0 sec.
10/15/00	-008	Changed: Separated Errata table 28F640J3A/28F320J3A into two tables– 28F640J3A and 28F320J3A Added: Erratum #14, *Erase Suspend to Program* Added: Erratum #15, *Program Suspend* Added: Erratum #16, *110ns Read Speed*
11/06/00	-009	Added: Erratum #17, *Standby Current* (I_{CCS}) Minor text edits for clarification of Errata Nos. 14, 15, 16, 17
12/04/00	-010	Added component ordering information for the 32M errata #16 and #17
2/12/01	-011	Updated Errata #9, #13 and #16 status from Fix to NoFix Updated Errata #14, #15 and #17 status from Fix to Fixed Added Specification Changes #10, #11 and #12 Added B0 stepping to 128M errata table; added B0 stepping to 32M errata table Minor text edits for clarification of Errata #6

Downloaded from Elcodis.com electronic components distributor

Date	Version	Description
07/25/01	-012	Updated Errata #5 status from Eval to Fixed Added latest S-Spec information Added Specification Changes #13 – #17 Added Documentation Changes #1 and #2
10/29/01	-013	Added Specification Changes #18 and #19
04/16/02	-014	Added Specification Change #20 and updated Ordering and Errata information

Downloaded from Elcodis.com electronic components distributor

Preface

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata and specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

Affected Documents/Related Documents

Title	Order
3 Volt Intel StrataFlash® Memory; 28F128J3A, 28F640J3A, 28F320J3A (x8/x16) datasheet	290667-011

Nomenclature

Errata are design defects or errors. These may cause the 3 Volt Intel® StrataFlash™ Memory's behavior to deviate from published specifications. Hardware and software designed to be used with any given stepping must assume that all errata documented for that stepping are present on all devices.

Specification Changes are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

Documentation Changes include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

Downloaded from Elcodis.com electronic components distributor

Summary Table of Changes

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the 3 Volt Intel StrataFlash memory components. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

Codes Used in Summary Table

Stepping

X:	Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping.
(No mark) or (Blank box):	This erratum is fixed in listed stepping or specification change does not apply to listed stepping.

Page

(Page):	Page location of item in this document.

Status

Doc:	Document change or update will be implemented.
Fix:	This erratum is intended to be fixed in a future step of the component.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Eval:	Plans to fix this erratum are under evaluation.

Row

|	Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document.

Downloaded from Elcodis.com electronic components distributor

Errata

28F128J3A (128Mbit)											
Number	**Stepping**				**FPO Mark (9th digit)**				**Page**	**Status**	**Errata**
	A1	**A2**	**A3**	**B0**	**A**	**B**	**C**	**D**			
1	X	X							14	Fixed	Programming Time Parameters
2	X	X							14	Fixed	Block Erase Time
3	X								14	Fixed	Electrostatic Discharge Protection
4	X	X	X	X	X	X	X	X	15	NoFix	5-Volt I/O Operation
5		X			X	X			15	Fixed	Operating Temperature Range
6	X	X							15	Fixed	Read Parameter t_{ELQX}
7	X	X							15	Fixed	Read Parameter t_{ELAV}
8	X	X							15	Fixed	Read Parameter t_{ELQV} Deleted
9	X	X	X	X	X	X	X	X	16	NoFix	Write Parameter t_{WHRL}
10	X	X	X		X				16	Fixed	Erase Suspend Latency t_{WHRH}
11	X	X	X		X				17	Fixed	Erase Suspend Command
12	X	X	X						17	Fixed	Erase Suspend Command 2
13	X	X	X	X	X	X	X	X	17	NoFix	Program Suspend Latency t_{WHRH1}
14	X	X	X		X	X			17	Fixed	Erase Suspend to Program

28F640J3A (64Mbit)							
Number	**Steppings**		**FPO Mark (9th digit)**		**Page**	**Status**	**Errata**
	A0	**A1**	**B**	**C**			
9	X	X	X	X	16	NoFix	Write Parameter t_{WHRL}
10	X				16	Fixed	Erase Suspend Latency t_{WHRH}
11	X				17	Fixed	Erase Suspend
13	X	X	X	X	17	NoFix	Program Suspend Latency t_{WHRH1}
15	X				18	Fixed	Program Suspend

Downloaded from Elcodis.com electronic components distributor

28F320J3A (32Mbit)						
Number	Steppings			Page	Status	Errata
	A0	B0				
9	X	X		16	NoFix	Write Parameter t_{WHRL}
10	X			16	Fixed	Erase Suspend Latency t_{WHRH}
11	X			17	Fixed	Erase Suspend
13	X	X		17	NoFix	Program Suspend Latency t_{WHRH1}
16	X	X		18	NoFix	110ns Read Speed
17	X			18	Fixed	Standby Current (I_{CCS})

Specification Changes

Number	Page	Specification Changes
1	19	Read Parameters for the 28F320J3A Have Been Changed to 100 ns
2	19	Block Erase Time Increased
3	19	Block Lock and Unlock Latencies Have Been Increased
4	19	Maximum Standby Current (I_{CCS} Max) Increased to 120 µA
5	20	5 Volt I/O Operation Removed
6	20	Operating Temperature Range
7	20	I_{CCR}
8	20	Program and Erase Time
9	21	Block Lock-Bit Set and Clear Times
10	21	Write Parameter t_{WHRL} increased to 500ns
11	21	Program Suspend Latency t_{WHRH1} increased to 75µs
12	21	Read speed access increased to 110ns for 28F320J3
13	21	Operating Temperature Range
14	21	Read Parameter t_{EHQZ} reduced to 35 ns
15	21	Write Parameter t_{WHEH} reduced to 0 ns
16	22	Lock-Bit and Suspend Latency parameter adjustments for –40°C added
17	22	Lockout Voltage increased to 2.2 V
18	22	Read Parameter t_{APA} reduced to 25 ns for 2.7 V - 3.6 V range
19	22	Read Parameter t_{GLQV} reduced to 25 ns for 2.7 V - 3.6 V range
20	22	Clear Block Lock-Bits Time parameter adjustment for –40°C added

Specification Clarifications

Number	Page	Specification Clarifications
1	23	Set Read Configuration Command

Downloaded from Elcodis.com electronic components distributor

Documentation Changes

Number	Page	Document Revision	Documentation Changes
1	23	-012	Error in Section 6.6, Note #4
2	23	-012	Error in Section 6.4, Note #4

Identification Information

Component Ordering Specifications

128-Mb A-1 Stepping: Errata #1–5; Specification Change #4		
E28F128J3A-150	N/A	N/A
128-Mb A-2 Stepping: Errata #1, 2, 4–7; Specification Change #4		
E28F128J3A-150	Q588	2-piece tape/tube
	Q589	100-piece tape and reel
RC28F128J3A-150	Q594	2-piece tape/tube
	Q595	100-piece tape and reel
128-Mb A-3 Stepping: Errata #4, 9–12; Specification Change #2–9		
E28F128J3A-150	B93	2-piece tape/tube
	SL3ZK	72-piece tray
	SL3ZL	96-piece tape/tube
RC28F128J3A-150	SB93	2-piece tape/tube
	Q679	100-piece tape and reel
128-Mb A-3 Stepping: Errata #4, 9 10,11; Specification Change #2–9		
E28F128J3A-150 **RC28F128J3A-150**	SB48	Tape/tube, ninth letter in FPO mark will have “A”
		Tray, ninth letter in FPO mark will have “A”
128-Mb A-3 Stepping: Errata # 9; Specification Change #2–9		
E28F128J3A-150 **RC28F128J3A-150**	SB48	Tape/tube, ninth letter in FPO mark will have “B”
		Tray, ninth letter in FPO mark will have “B”
128-Mb A-3 Stepping: Errata #9,13; Specification Change #2-11, 17		
E28F128J3A-150	SL56C	2-pc tube
	833865	96-pc tray
	SL56D	1600-pc tape & reel
RC28F128J3A-150	SL56C	2-pc tube
	SL56J	144-pc tray
	SL56D	2000-pc tape & reel

Downloaded from Elcodis.com electronic components distributor

128-Mb B-0 Stepping: Errata #9,13; Specification Change #2-5, 7-11, 13-20 *MOST RECENT*		
E28F128J3A-150	SL56L	2-pc tube
	SL56K	96-pc tray
	SL56D	1600-pc tape & reel
RC28F128J3A-150	SL56L	2-pc tube
	SL56K	144-pc tray
	SL56M	2000-pc tape & reel
64-Mb A-0 Stepping: Errata #9–11; Specification Change #1–9		
E28F640J3A-120	Q684	2-piece tape/tube
	Q685	100-piece tape/reel
RC28F640J3A-120	Q686	2-piece tape/tube
	Q687	100-piece tape/reel

Downloaded from Elcodis.com electronic components distributor

64-Mb A-0 Stepping: Errata #5, #9–11; Specification Change #1–9		
E28F640J3A-120	Default	96 tray
	SB48	1600-piece tape/reel
	SB93	2-piece tube
64-Mb A-0 Stepping: Errata #5, #9; Specification Change #1–9		
RC28F640J3A-120	Default	144 tray
	SB48	2000-piece tape/reel
	SB93	2 piece tube
64-Mb A-1 Stepping: Errata #9, #13; Specification Change #2-5, 7–11, 13-20 *MOST RECENT*		
E28F640J3A-120	SL5AR	2-pc tube
	SL5AQ	96-pc tray
	SL5AS	1600-pc tape & reel
RC28F640J3A-120	SL5AR	2-pc tube
	SL5AQ	144-pc tray
	SL5AS	2000-pc tape & reel
32-Mb A-0 Stepping: Errata #16, #17; Specification Change #1–9		
E28F320J3A-110	Default	96 piece tray
	SB10	1600 piece tape/reel
	Q-A03	2 piece tube
32-Mb B-0 Stepping: Errata #9, #13, #16; Specification Change #2-5, 7-20 *MOST RECENT*		
E28F320J3A-110	SB93	2-pc tube
	834996	96-pc tray
	SB48	1600-pc tape & reel
RC28F320J3A-110	SB93	2-pc tube
	834965	144-pc tray
	SB48	2000-pc tape & reel

NOTES:
1. Q-spec order numbers correspond to sample units.
2. S-spec order numbers correspond to production (qualified) units.

Downloaded from Elcodis.com electronic components distributor

Errata

1. Programming Time Parameters

Problem: The table below summarizes the programming time parameters.

Block Erase, Program, and Lock-Bit Configuration Performance(1,2,3)

#	Sym	Parameter	Notes	Typ	Max	Unit
W16		Write Buffer Byte Program Time (Time to Program 32 bytes/16 words)	4,5,6,7	384	TBD	µs
W16	t_{WHQV3}	Byte Program Time (Using Word/Byte Program Command)	4	360	TBD	µs
	t_{EHQV3}	Block Program Time (Using Write to Buffer Command)	4	1.6	TBD	sec

NOTES:
1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time (t_{WHQV1}, t_{EHQV1}) is 6.8 µs/byte (typical)
7. Effective per-word program time (t_{WHQV2}, t_{EHQV2}) is 13.6 µs/word (typical)
8. Max values are measured at worst case temperature and V_{CC} corner after 100k cycles

Implication: Both methods to program the flash memory are affected by this erratum: using the 32-byte write buffer and using the single byte/word program command.

Workaround: No workaround(s) has been identified for this erratum.

Status: This is intended to be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on A3 and above steppings.

2. Block Erase Time

Problem: The typical time required to erase one 128-Kbyte block is 2.0 sec and the maximum time is 25 sec.

Implication: System designers should be aware of this specification as it could impact system operation or performance.

Workaround: No workaround(s) has been identified for this erratum.

Status: This is intended to be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on A3 and above steppings.

3. Electrostatic Discharge Protection

Problem: Input and I/O pins fail Intel's internal electrostatic discharge (ESD) specification.

Implication: Customers may experience leakage currents on input and I/O pins greater than 1 µA. Parts that have failed Intel's ESD testing exhibited leakage currents greater than 1 µA.

Workaround: Customers should not perform ESD testing on these components. The parts do not require any special handling and may be used in a normal system. However, specific ESD testing on the component should not be performed until a future stepping of the device that corrects this erratum.

Downloaded from Elcodis.com electronic components distributor

Status: This erratum is fixed. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on A2 and above steppings.

4. 5-Volt I/O Operation

Problem: The 5-Volt I/O feature of this flash memory is not supported.

Implication: The flash memory does not support 5 V levels on its outputs or its inputs. This includes address, data, and control pins.

Workaround: Provide a 3 V interface to the flash memory I/O pins of capable systems.

Status: This will not be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

5. Operating Temperature Range

Problem: The operating temperature range for this device is 0 °C to +70 °C. with a –20 °C read only operation.

Implication: Customers that use this part in applications that require full device operation below 0 °C should be aware of this erratum. Full operation of the device below 0 °C is not guaranteed and should not be attempted. The device will read down to –20 °C.

Workaround: No workaround(s) has been identified for this erratum.

Status: This erratum is valid for 128M A-0, A1, and A-2 steppings and was fixed in subsequent steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

6. Read Parameter t_{ELQX}

Problem: Devices need the parameter t_{ELQX} =150 ns minimum. CE low to output in low Z (t_{ELQX}) is designated as R6 in Figure 1, in this Specification Update revision.

Implication: Higher volume prototype testing could experience read failures if this erratum is ignored.

Workaround: Use devices for initial lower volume prototype development.

Status: This is intended to be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on A3 and above steppings.

7. Read Parameter t_{ELAV}

Problem: Devices need the parameter t_{ELAV} = 500 ns maximum. Chip Enable to Address Valid (t_{ELAV}) is designated as R3 in Figure 1, in this Specification Update revision.

Implication: Higher volume prototype testing could experience read failures if this erratum is ignored.

Workaround: Use devices for initial lower volume prototype development.

Status: This is intended to be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on A3 and above steppings.

8. Read Parameter t_{ELQV} Deleted

Problem: The parameter t_{ELQV} has been deleted.

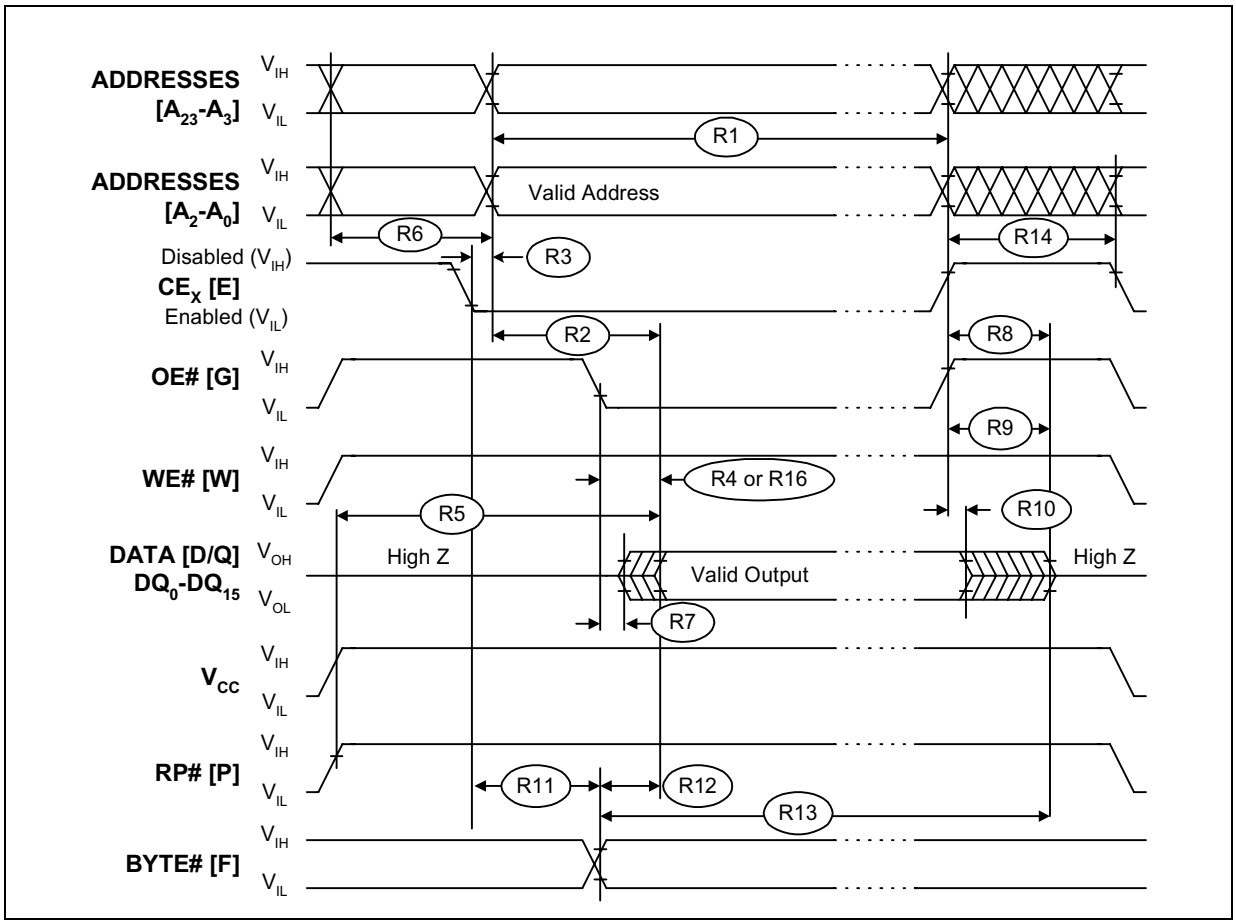
Implication: Higher volume prototype testing could experience read failures if this erratum is ignored.

Workaround: Use devices for initial lower volume prototype development.

Status: This is intended to be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on A3 and above steppings.

Downloaded from Elcodis.com electronic components distributor

Figure 1. AC Waveform for Standard Word/Byte Read Operations



NOTE: CE_X low is defined as the first edge of CE_0, CE_1, or CE_2 that enables the device. CE_X high is defined at the first edge of CE_0, CE_1, or CE_2 that disables the device (see Table 2, *Chip Enable Truth Table*). When reading the flash array, a faster t_{GLQV} (R16) applies. Non-array reads refer to status register reads, query reads, or device identifier reads.

9. Write Parameter t_{WHRL}

Problem: The parameter t_{WHRL} has been extended to 500 ns.

Implication: Customer may not see the device ready when using the STS pin.

Workaround: Customer should allow a minimum of 500 ns before polling the STS pin after WE# goes high when erasing or programming the device.

Status: This will not be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

10. Erase Suspend Latency t_{WHRH}

Problem: The parameter t_{WHRH} has been extended to 120 µs.

Implication: Customer may not be able to read the device after a Erase suspend for up to 120 µs.

Workaround: There is no known work around for this issue.

Downloaded from Elcodis.com electronic components distributor

Status: This is intended to be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on material that has a "B" in the ninth character in the FPO number.

11. Erase Suspend Command

Problem: Device may not complete an erase function if an Erase Suspend Resume command sequence is given to the device.

Implication: Customers may see the suspended block partially programmed when the erase has completed. If the device locks up, the customer may not be able to perform another erase until RP# is toggled to GND.

Workaround: The customer should verify that the erase has completed by executing a read on the array. If the device did not complete the erase, the customer should re-issue the Erase command to finish the erase function.

Status: This is intended to be fixed in a future product release. Refer to *Identification Information* for affected product ordering information. Also refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on material that has a "B" in the 9th character in the FPO number.

12. Erase Suspend Command 2

Problem: Device may lock up during an Erase Suspend command.

Implication: If the device locks up, the customer may not be able to execute another erase until RP# is toggled to GND.

Workaround: The customer should verify that the erase has completed by executing a read on the array. If the device did not complete the erase, the customer should re-issue the Erase command to finish the erase function. If the device locks up, the customer should toggle RP# to GND to recover.

Status: This is intended to be fixed in a future product release. Refer to *Identification Information* for affected product ordering information. Also, refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s). This is fixed on material that has a "B" in the ninth character in the FPO number.

13. Program Suspend Latency t_{WHRH1}

Problem: The parameter t_{WHRH1} has been extended to 75 µs.

Implication: Customer may not be able to read the device after a Program suspend for up to 75 µs.

Workaround: There is no known workaround for this issue.

Status: This will not be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

14. Erase Suspend To Program

Problem: When an erase suspend operation is initiated on block X, where X = 0 to 63, the user will not be able to program any data in block X + 64.

Implication: Customers performing an erase suspend to program operation should be aware that the program portion of this operation will not occur and that it will set status register bit-4 (SR.4 = 1).

Workaround: There is no known work around for this issue.

Status: This is intended to be fixed in a future product release. Refer to *Identification Information* for affected product ordering information. Also, refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

Downloaded from Elcodis.com electronic components distributor

15. Program Suspend

— When a Write to Buffer program operation is suspended, the device can inadvertently reset the data in the write buffer.

Implication: Customers performing a program suspend on a Write to Buffer command should be aware that the data in the write buffer may get reset to FFFFh. Therefore, when the program suspend is resumed, the expected data may not exist in the write buffer. Resulting in incorrect data being programmed to the array.

Workaround: There is no known work around for this issue.

Status: This is intended to be fixed in a future product release. Refer to *Identification Information* for affected product ordering information. Also, refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

16. 110ns Read Speed

Problem: Device is unable to support read accesses at 100ns.

Implication: Customers should be aware that the device read access is 110ns.

Workaround: There is no known work around for this issue.

Status: This will not be fixed in future steppings. Refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

17. Standby Current (I_{CCS})

Problem: Maximum RMS standby current is 170uA.

Implication: Due to the additional maximum current, customers using this device in a battery operated system should be aware of this erratum because the expected battery life may need re-evaluated.

Workaround: There is no known work around for this issue.

Status: This is intended to be fixed in a future product release. Refer to *Identification Information* for affected product ordering information. Also, refer to the *Summary Tables of Changes* to determine affected product(s) and stepping(s).

Downloaded from Elcodis.com electronic components distributor

Specification Changes

1. Read Parameters for the 28F320J3A Have Been Changed to 100 ns

Issue: Several read parameters for the 28F320J3A have been changed from 90 ns to 100 ns.

The 28F320J3A read parameters t_{AVAV} (R1), t_{AVQV} (R2), for 3 V I/O operation have been changed from 90 ns to 100 ns. Customers who designed systems around the 90 ns parameters should be aware of these changes.

2. Block Erase Time Increased

Issue: The block erase time was changed. Typical block erase time is 1.0 sec, and the maximum is 5 sec. Customers should be aware that this is an increase from the 0.7 typical block erase time.

3. Block Lock and Unlock Latencies Have Been Increased

Issue: The table below summarizes the block lock-bit parameters that have been increased.

Block Erase, Program, and Lock-Bit Configuration Performance(1,2,3)

#	Sym	Parameter	Notes	Typ	Max	Unit
W16	t_{WHQV5} t_{EHQV5}	Set Lock-Bit Time	4	64	75	µs
W16	t_{WHQV6} t_{EHQV6}	Clear Block Lock-Bits Time	4	0.5	0.70	sec

NOTES:
1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time (t_{WHQV1}, t_{EHQV1}) is 6.8 µs/byte (typical).
7. Effective per-word program time (t_{WHQV2}, t_{EHQV2}) is 13.6 µs/word (typical).
8. Max values are measured at worst case temperature and V_{CC} corner after 100k cycles.

The time required to set a block lock-bit (i.e., lock a block) and the time required to clear a block lock-bit (i.e., unlock a block) have been increased. System designers should be aware of these changes if these specification increases affect system operation or performance.

4. Maximum Standby Current (I_{CCS} Max) Increased to 120 µA

Issue: The maximum standby current for this device is 120 µA.

Customers should be aware when designing their systems based on the maximum current ratings for this device. This parameter would typically affect power consumption. By definition, the maximum standby current is the highest amount of current drawn by this device, when deselected, under the most extreme/worst conditions.

Downloaded from Elcodis.com electronic components distributor

5. 5 Volt I/O Operation Removed

Issue: 5 Volt I/O operation is removed from all steppings.

Device damage may be experienced if this change is ignored.

6. Operating Temperature Range

Issue: Operating Temperature range is being changed to –25 °C to +85 °C.

7. I_{CCR}

Issue: The table below summarizes the I_{CCR} parameters that have been changed.

Symbol	Parameter	Notes	Typ	Max	Unit	Test Conditions
I_{CCR}	V_{CC} Page Mode Read Current	1,3,4	15	20	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 4 word page mode reads. Device is enabled (see Table 2 in the datasheet) f = 5 MHz, I_{OUT} = 0 mA
			24	29	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard 4 word page mode reads. Device is enabled ((see Table 2 in the datasheet)) f = 33 MHz, I_{OUT} = 0 mA
I_{CCR}	V_{CC} Byte Mode Read Current	1,3,4	40	50	mA	CMOS Inputs, V_{CC} = V_{CC} Max, V_{CCQ} = V_{CCQ} Max using standard word/byte single reads Device is enabled ((see Table 2 in the datasheet)) f = 5 MHz, I_{OUT} = 0 mA

8. Program and Erase Time

Issue: The table below summarizes the Program and Erase parameters that have been changed.

Block Erase, Program, and Lock-Bit Configuration Performance(1,2,3)

#	Sym	Parameter	Notes	Typ	Max	Unit
W16		Write Buffer Byte Program Time (Time to Program 32 bytes/16 words)	4,5,6,7	218	654	µs
W16	t_{WHQV3} t_{EHQV3}	Byte Program Time (Using Word/Byte Program Command)	4	210	630	µs
		Block Program Time (Using Write to Buffer Command)	4	0.8	2.4	sec
W16	t_{WHQV4} t_{EHQV4}	Block Erase Time	4	1.0	5.0	sec

NOTES:
1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time (t_{WHQV1}, t_{EHQV1}) is 6.8 µs/byte (typical).
7. Effective per-word program time (t_{WHQV2}, t_{EHQV2}) is 13.6 µs/word (typical).
8. Max values are measured at worst case temperature and V_{CC} corner after 100k cycles.

Downloaded from Elcodis.com electronic components distributor

9. Block Lock-Bit Set and Clear Times

Problem: The table below summarizes the block lock-bit parameters that have been changed.

Block Erase, Program, and Lock-Bit Configuration Performance(1,2,3)

#	Sym	Parameter	Notes	Typ	Max	Unit
W16	t_{WHQV5} t_{EHQV5}	Set Lock-Bit Time	4	64	75	µs
W16	t_{WHQV6} t_{EHQV6}	Clear Block Lock-Bits Time	4	0.5	0.70	sec

NOTES:
1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time (t_{WHQV1}, t_{EHQV1}) is 6.8 µs/byte (typical)
7. Effective per-word program time (t_{WHQV2}, t_{EHQV2}) is 13.6 µs/word (typical)
8. Max values are measured at worst case temperature and V_{CC} corner after 100k cycles

The time required to set a block lock bit (i.e., lock a block) and the time required to clear a block lock-bit (i.e., unlock a block) have been increased. System designers should be aware of these changes if these specification increases affect system operation or performance.

10. Write parameter t_{WHRL} increased to 500ns

Problem: The maximum t_{WHRL} (W13) time has increased from 90ns to 500ns. Customers using the STS pin should be aware of this change.

11. Program suspend latency t_{WHRH1} increased to 75us

Problem: The maximum t_{WHRH1} (W16) time has increased from 30µs to 75µs. Customers using the program suspend feature should be aware of this change.

12. Read speed access increased to 110ns for 28F320J3

Problem: The 28F320J3 read parameters t_{AVAV} (R1), t_{AVQV} (R2), and t_{ELQV} (R3) have been increased from 100 ns to 110 ns. Customers who designed systems around the 100 ns parameters should be aware of these changes.

13. Operating Temperature Range

Issue: Operating Temperature range is being changed to –40 °C to 85 °C.

14. Read parameter t_{EHQZ} reduced to 35 ns

Issue: Parameter t_{EHQZ} (R8) has been reduced from 55 ns(max) to 35 ns(max). Customers may now take advantage of this reduced timing.

15. Write parameter t_{WHEH} reduced to 0 ns

Issue: Parameter t_{WHEH} (W6) has been reduced from 10 ns(min) to 0 ns(min). Customers may now take advantage of this reduced timing.

Downloaded from Elcodis.com electronic components distributor

16. Lock-Bit and Suspend Latency parameter adjustments for –40°C added

Issue: The table below summarizes the Lock-Bit and Suspend Latency parameters that have been changed.

Block Erase, Program, and Lock-Bit Configuration Performance(1,2,3)

#	Sym	Parameter	Notes	Typ	Max	Unit
W16	t_{WHQV5} t_{EHQV5}	Set Lock-Bit Time	4,9	64	75/85	µs
W16	t_{WHRH1} t_{EHRH1}	Program Suspend Latency Time to Read	9		75/90	µs
W16	t_{WHRH} t_{EHRH}	Erase Suspend Latency Time to Read	9		35/40	µs

NOTES:
1. Typical values measured at T_A = +25 °C and nominal voltages. Assumes corresponding lock-bits are not set. Subject to change based on device characterization.
2. These performance numbers are valid for all speed versions.
3. Sampled but not 100% tested.
4. Excludes system-level overhead.
5. These values are valid when the buffer is full, and the start address is aligned on a 32-byte boundary.
6. Effective per-byte program time (t_{WHQV1}, t_{EHQV1}) is 6.8 µs/byte (typical).
7. Effective per-word program time (t_{WHQV2}, t_{EHQV2}) is 13.6 µs/word (typical).
8. Max values are measured at worst case temperature and V_{CC} corner after 100k cycles (except as noted).
9. Max values are expressed at –25 °C/–40 °C.

17. Lockout Voltage increased to 2.2 V

Issue: V_{PENLK} and V_{LKO} are being changed from 2.0 V to 2.2 V. Customers who use voltages in this range should be aware of these changes.

18. Read parameter t_{APA} reduced to 25 ns

Issue: Parameter t_{APA} (R15) has been reduced from 30 ns(max) to 25 ns(max) on the 2.7 V - 3.6 V range. Previously, 25 ns was only granted on the 3.0 V - 3.6 V range. Customers may now take advantage of this reduced timing.

19. Write parameter t_{GLQV} reduced to 25 ns

Issue: Parameter t_{GLQV} (R16) has been reduced from 30 ns(max) to 25 ns(max) on the 2.7 V - 3.6 V range. Previously, 25 ns was only granted on the 3.0 V - 3.6 V range. Customers may now take advantage of this reduced timing.

20. Clear Block Lock-Bits Time parameter adjustment for –40°C added

Issue: The table below summarizes the Clear Block Lock-bits parameter that has been changed.

#	Sym	Parameter	Notes	Typ	Max	Unit
W16	t_{WHQV6} t_{EHQV6}	Clear Block Lock-Bits Time	4,10	0.5	0.70/ 1.4	sec

Notes:
4. Excludes system-level overhead.
10. Max values are expressed at 25 °C/–40 °C.

Downloaded from Elcodis.com electronic components distributor

Specification Clarifications

1. Set Read Configuration Command

Status: Changed Section 4.11, *Set Read Configuration Command*, and Section 4.11.1, *Read Configuration*, as follows:

4.11: This command is not supported on this product. This device defaults to the asynchronous page mode. If this command is given to the device, it will not affect the operation of the device.

4.11.1: The device supports both asynchronous page mode and standard word/byte reads. No configuration is required.

Status register, and identifier support standard word/byte single read operations.

Documentation Changes

1. Error in Section 6.6, Note #4

Issue: Note #4 in Section 6.6 was changed as follows:

OLD:

4. Write pulse width (t_{WP}) is defined from CE_X or WE# going low (whichever goes low first) to CE_X or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$. If CEx is driven low 10 ns before WE# going low, WE# pulse width requirement decreases to t_{WP} - 10 ns.

NEW:

4. Write pulse width (t_{WP}) is defined from CE_X or WE# going low (whichever goes low last) to CE_X or WE# going high (whichever goes high first). Hence, $t_{WP} = t_{WLWH} = t_{ELEH} = t_{WLEH} = t_{ELWH}$

2. Error in Section 6.4, Note #4

Issue: Note #4 in Section 6.4 was obsoleted by Specification Change #6 and #13 (Operating Temperature Range). It was deleted and the remaining notes were re-numbered.

Downloaded from Elcodis.com electronic components distributor