256 Bit X24C44 16 x 16 Bit

Serial Nonvolatile Static RAM

FEATURES

- **Advanced CMOS version of Xicor's X2444**
- **16 x 16 organization**
- **Single 5V supply**
- **Ideal for use with single chip microcomputers**
  - **—Static timing**
  - **—Minimum I/O interface**
  - **—Serial port compatible (COPS™, 8051)**
  - **—Easily interfaced to microcontroller ports**
- **Software and hardware control of nonvolatile functions**
- **Auto $\overline{\text{RECALL}}$ on power-up**
- **TTL and CMOS compatible**
- **Low power dissipation**
  - **—Active current: 10mA maximum**
  - **—Standby current: 50µA maximum**
- **8-lead PDIP, Cerdip, and 8-lead SOIC packages**
- **High reliability**
  - **—$\overline{\text{STORE}}$ cycles: 1,000,000**
  - **—Data retention: 100 years**

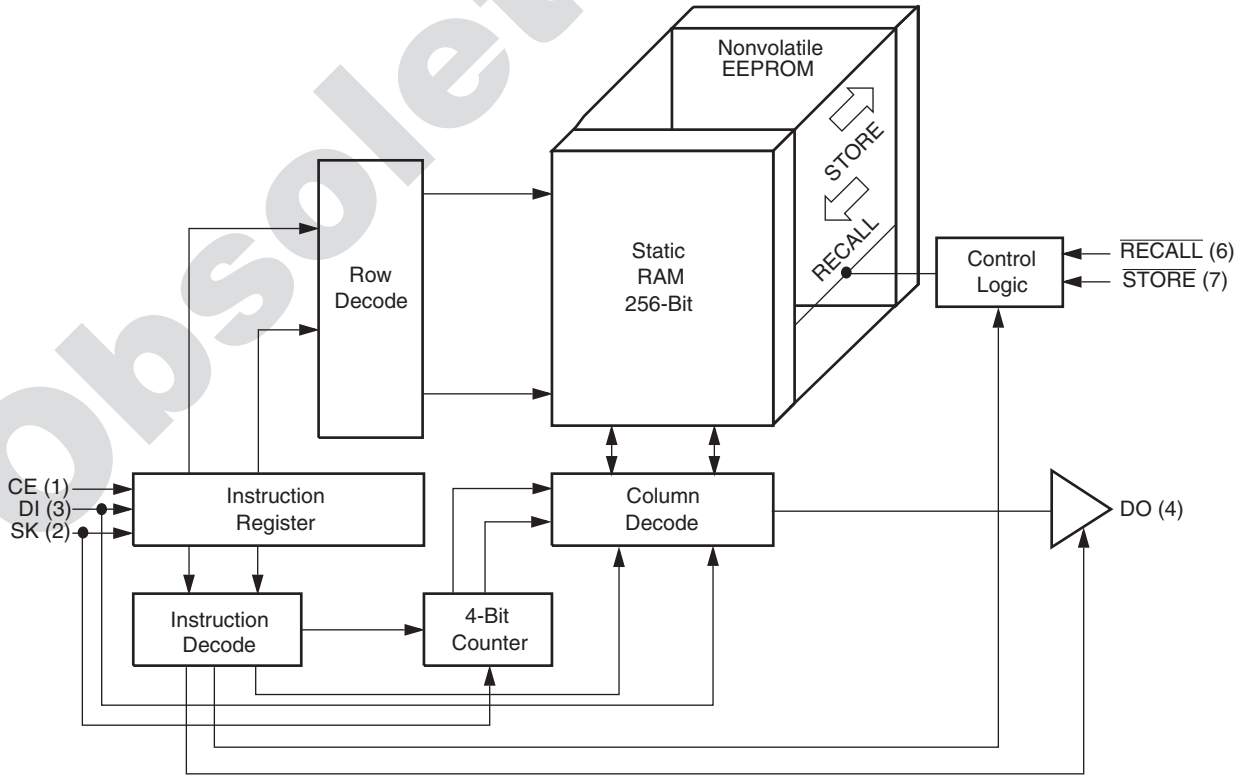
DESCRIPTION

The Xicor X24C44 is a serial 256 bit NOVRAM featuring a static RAM configured 16 x 16, overlaid bit-by-bit with a nonvolatile EEPROM array. The X24C44 is fabricated with Xicor's Advanced CMOS Floating Gate technology.

The Xicor NOVRAM design allows data to be transferred between the two memory arrays by means of software commands or external hardware inputs. A $\overline{\text{STORE}}$ operation (RAM data to EEPROM) is completed in 5ms or less and a $\overline{\text{RECALL}}$ operation (EEPROM data to RAM) is completed in 2µs or less.

Xicor NOVRAMs are designed for unlimited write operations to RAM, either from the host or $\overline{\text{RECALL}}$s from EEPROM and a minimum 1,000,000 $\overline{\text{STORE}}$ operations. Inherent data retention is specified to be greater than 100 years.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Chip Enable (CE)

The Chip Enable input must be HIGH to enable all read/write operations. CE must remain HIGH following a Read or Write command until the data transfer is complete. CE LOW places the X24C44 in the low power standby mode and resets the instruction register. Therefore, CE must be brought LOW after the completion of an operation in order to reset the instruction register in preparation for the next command.

Serial Clock (SK)

The Serial Clock input is used to clock all data into and out of the device.

Data In (DI)

Data In is the serial data input.

Data Out (DO)

Data Out is the serial data output. It is in the high impedance state except during data output cycles in response to a READ instruction.

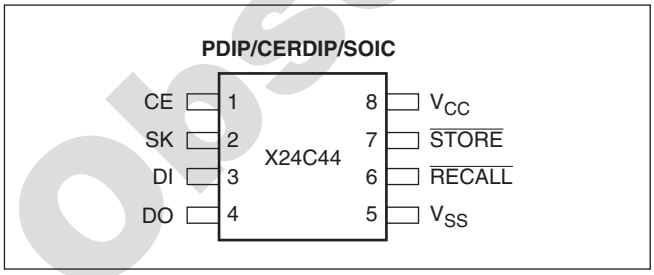
$\overline{\text{STORE}}$

$\overline{\text{STORE}}$ LOW will initiate an internal transfer of data from RAM to the EEPROM array.

$\overline{\text{RECALL}}$

$\overline{\text{RECALL}}$ LOW will initiate an internal transfer of data from EEPROM to the RAM array.

PIN CONFIGURATION



PIN NAMES

Symbol	Description
CE	Chip Enable
SK	Serial Clock
DI	Serial Data In
DO	Serial Data Out
$\overline{\text{RECALL}}$	$\overline{\text{RECALL}}$ Input
$\overline{\text{STORE}}$	$\overline{\text{STORE}}$ Input
V_{CC}	+5V
V_{SS}	Ground

DEVICE OPERATION

The X24C44 contains an 8-bit instruction register. It is accessed via the DI input, with data being clocked in on the rising edge of SK. CE must be HIGH during the entire data transfer operation.

Table 1. contains a list of the instructions and their operation codes. The most significant bit (MSB) of all instructions is a logic one (HIGH), bits 6 through 3 are either RAM address bits (A) or don't cares (X) and bits 2 through 0 are the operation codes. The X24C44 requires the instruction to be shifted in with the MSB first.

After CE is HIGH, the X24C44 will not begin to interpret the data stream until a logic "1" has been shifted in on DI. Therefore, CE may be brought HIGH with SK running and DI LOW. DI must then go HIGH to indicate the start condition of an instruction before the X24C44 will begin any action.

In addition, the SK clock is totally static. The user can completely stop the clock and data shifting will be stopped. Restarting the clock will resume shifting of data.

RCL and $\overline{\text{RECALL}}$

Either a software RCL instruction or a LOW on the $\overline{\text{RECALL}}$ input will initiate a transfer of EEPROM data into RAM. This software or hardware $\overline{\text{RECALL}}$ operation sets an internal "previous recall" latch. This latch is reset upon power-up and must be intentionally set by the user to enable any write or $\overline{\text{STORE}}$ operations. Although a $\overline{\text{RECALL}}$ operation is performed upon power-up, the previous $\overline{\text{RECALL}}$ latch is not set by this operation.

WRDS and WREN

Internally the X24C44 contains a "write enable" latch. This latch must be set for either writes to the RAM or store operations to the EEPROM. The WREN instruction sets the latch and the WRDS instruction resets the latch, disabling both RAM writes and EEPROM stores, effectively protecting the nonvolatile data from corruption. The write enable latch is automatically reset on power-up.

STO and $\overline{\text{STORE}}$

Either the software STO instruction or a LOW on the $\overline{\text{STORE}}$ input will initiate a transfer of data from RAM to EEPROM. In order to safeguard against unwanted store operations, the following conditions must be true:

– STO instruction issued or $\overline{\text{STORE}}$ input is LOW.

– The internal "write enable" latch must be set (WREN instruction issued).

– The "previous recall" latch must be set (either a software or hardware recall operation).

Once the store cycle is initiated, all other device functions are inhibited. Upon completion of the store cycle, the write enable latch is reset. Refer to Figure 4 for a state diagram description of enabling/disabling conditions for store operations.

WRITE

The WRITE instruction contains the 4-bit address of the word to be written. The write instruction is immediately followed by the 16-bit word to be written. CE must remain HIGH during the entire operation. CE must go LOW before the next rising edge of SK. If CE is brought LOW prematurely (after the instruction but before 16 bits of data are transferred), the instruction register will be reset and the data that was shifted-in will be written to RAM.

If CE is kept HIGH for more than 24 SK clock cycles (8-bit instruction plus 16-bit data), the data already shifted-in will be overwritten.

READ

The READ instruction contains the 4-bit address of the word to be accessed. Unlike the other six instructions, I_0 of the instruction word is a "don't care". This provides two advantages. In a design that ties both DI and DO together, the absence of an eighth bit in the instruction allows the host time to convert an I/O line from an output to an input. Secondly, it allows for valid data output during the ninth SK clock cycle.

D0, the first bit output during a read operation, is truncated. That is, it is internally clocked by the falling edge of the eighth SK clock; whereas, all succeeding bits are clocked by the rising edge of SK (refer to Read Cycle Diagram).

LOW POWER MODE

When CE is LOW, non-critical internal devices are powered-down, placing the device in the standby power mode, thereby minimizing power consumption.

SLEEP

Because the X24C44 is a low power CMOS device, the SLEEP instruction implemented on the first generation NMOS device has been deleted. For systems converting from the X2444 to the X24C44 the software need not be changed; the instruction will be ignored.

Table 1. Instruction Set

Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Figure 3)	1XXXX000	Reset Write Enable Latch (Disables Writes and $\overline{\text{STORE}}$s)
STO (Figure 3)	1XXXX001	$\overline{\text{STORE}}$ RAM Data in EEPROM
Reserved	1XXXX010	N/A
WRITE (Figure 2)	1AAAA011	Write Data into RAM Address AAAA
WREN (Figure 3)	1XXXX100	Set Write Enable Latch (Enables Writes and $\overline{\text{STORE}}$s)
RCL (Figure 3)	1XXXX101	Recall EEPROM Data into RAM
READ (Figure 1)	1AAAA11X	Read Data from RAM Address AAAA

Notes: X = Don't Care
A = Address

WRITE PROTECTION

The X24C44 provides two software write protection mechanisms to prevent inadvertent stores of unknown data.

Power-Up Condition

Upon power-up the “write enable” latch is in the reset state, disabling any store operation.

Unknown Data Store

The “previous recall” latch must be set after power-up. It may be set only by performing a software or hardware recall operation, which assures that data in all RAM locations is valid.

SYSTEM CONSIDERATIONS

Power-Up Recall

The X24C44 performs a power-up recall that transfers the EEPROM contents to the RAM array. Although the data may be read from the RAM array, this recall does not set the “previous recall” latch. During this power-up recall operation, all commands are ignored. Therefore, the host should delay any operations with the X24C44 a minimum of t_{PUR} after V_{CC} is stable.

Power-Down Data Protection

Because the X24C44 is a 5V only nonvolatile memory device it may be susceptible to inadvertent $\overline{\text{STORE}}$s to the EEPROM array during power-down cycles. Power-up cycles are not a problem because the “previous recall” latch and “write enable” latch are reset, preventing any possible corruption of EEPROM data.

Software Power-Down Protection

If the $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ pins are tied to V_{CC} through a pull-up resistor and only software operations are performed to initiate stores, there is little likelihood of an inadvertent store. However, if these two lines are under microprocessor control, positive action should be employed to negate the possibility of these control lines bouncing and generating an unwanted store. The safest method is to issue the WRDS command after a write sequence and also following store operations. Note: an internal store may take up to 5ms; therefore, the host microprocessor should delay 5ms after initiating the store prior to issuing the WRDS command.

Hardware Power-Down Protection

(when the “write enable” latch and “previous recall” latch are not in the reset state):

Holding either $\overline{\text{RECALL}}$ LOW, CE LOW or $\overline{\text{STORE}}$ HIGH during power-down will prevent an inadvertent store.

Figure 1. RAM Read

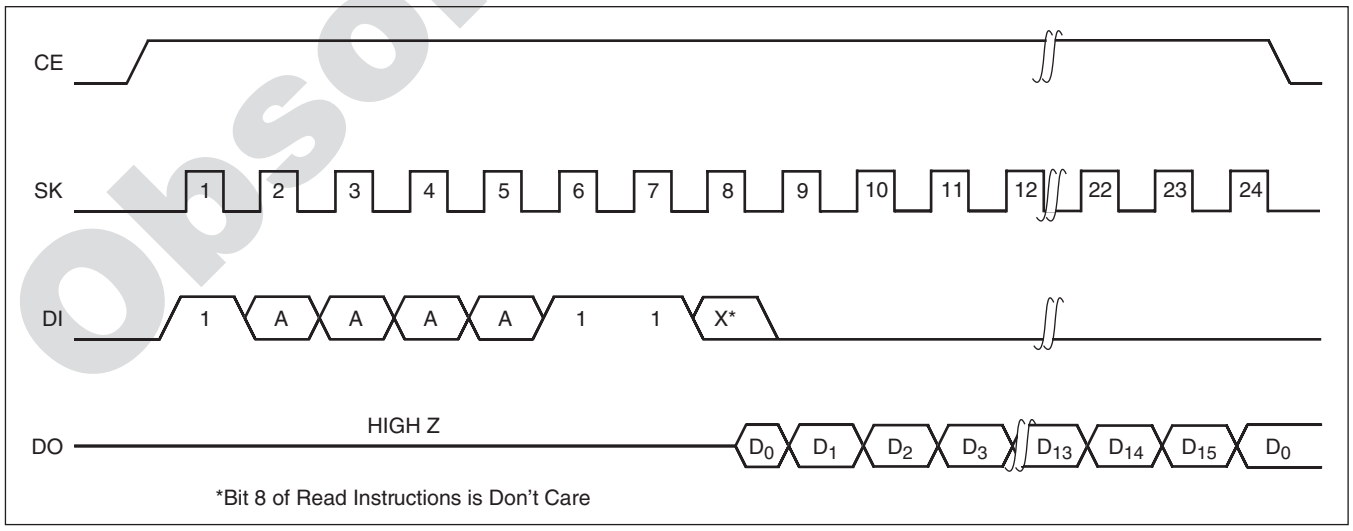


Figure 2. RAM Write

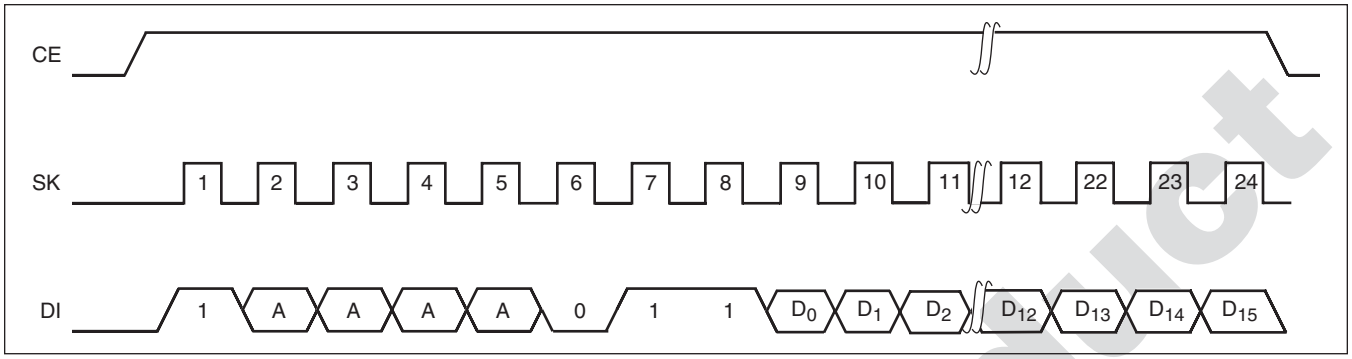


Figure 3. Non-Data Operations

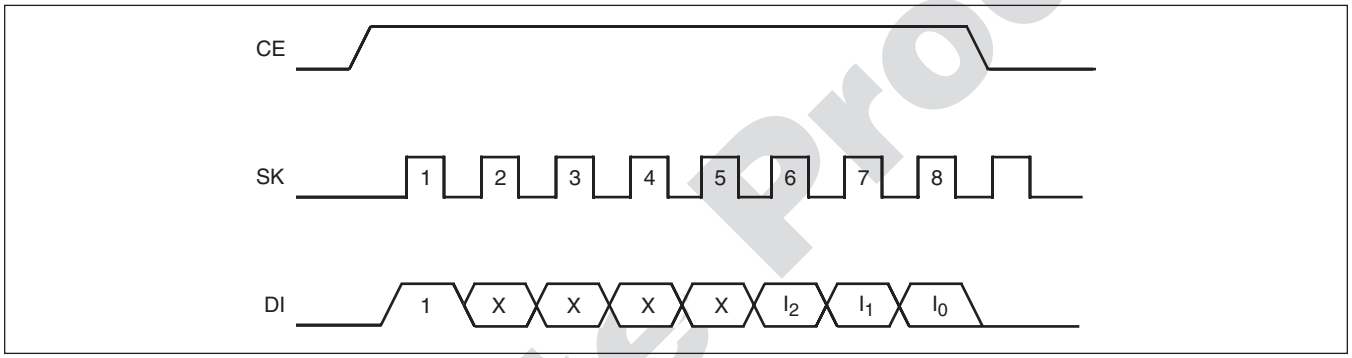
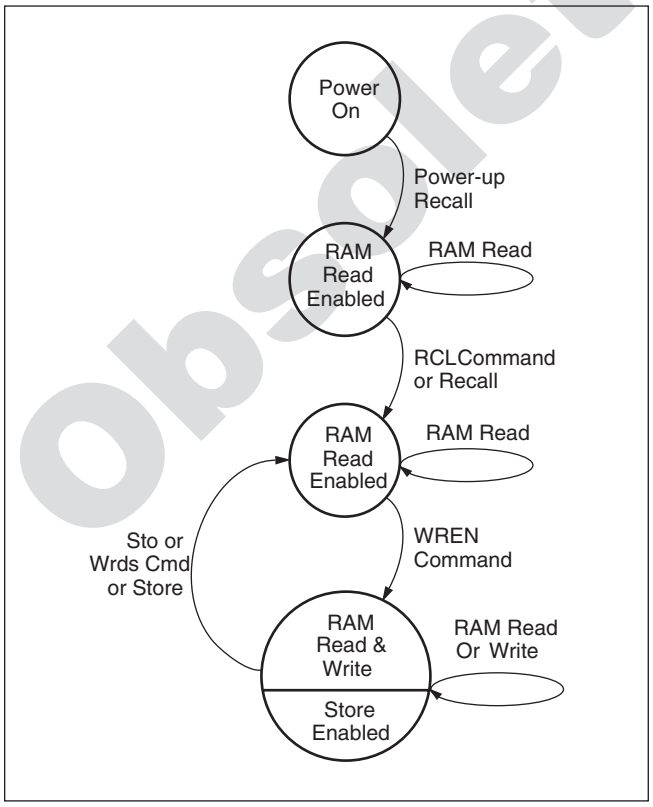


Figure 4. X24C44 State Diagram



ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... –65°C to +135°C
Storage Temperature..... –65°C to +150°C
Voltage on any pin with
respect to V_{SS} .....–1V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10 seconds)..... 300°C

COMMENT

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	–40°C	+85°C
Military	–55°C	+125°C

Supply Voltage	Limits
X24C44	5V ±10%

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits		Unit	Test Conditions
		Min.	Max.		
I_{CC}	V_{CC} supply current (TTL inputs)		10	mA	SK = 0.4V/2.4V levels @ 1MHz, DO = open, all other inputs = V_{IH}
I_{SB1}	V_{CC} standby current (TTL inputs)		1	mA	DO = open, $\overline{CE}$ = V_{IL} All other inputs = V_{IH}
I_{SB2}	V_{CC} standby current (CMOS inputs)		50	µA	DO = open, $\overline{CE}$ = V_{SS} All other inputs = V_{CC} – 0.3V
I_{LI}	Input load current		10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current		10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW voltage	–1	0.8	V	
V_{IH}(1)	Input HIGH voltage	2	V_{CC} + 1	V	
V_{OL}	Output LOW voltage		0.4	V	I_{OL} = 4.2mA
V_{OH}	Output HIGH voltage	2.4		V	I_{OH} = –2mA

ENDURANCE AND DATA RETENTION

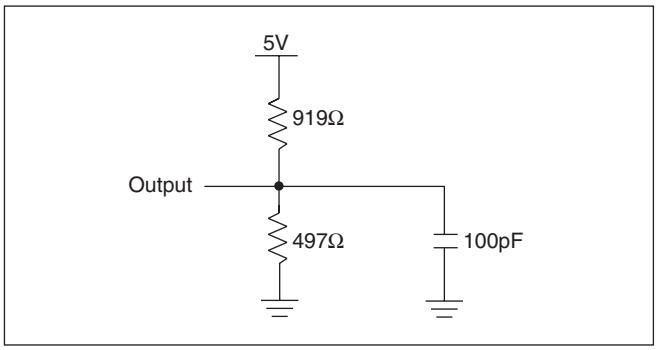
Parameter	Min.	Unit
Endurance	100,000	Data changes per bit
Store cycles	1,000,000	Store cycles
Data retention	100	Years

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Test Conditions
C_{OUT}(2)	Output capacitance	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input capacitance	6	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. CONDITIONS OF TEST

Input pulse levels	0V to 3V
Input rise and fall times	10ns
Input and output timing levels	1.5V

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read and Write Cycle Limits

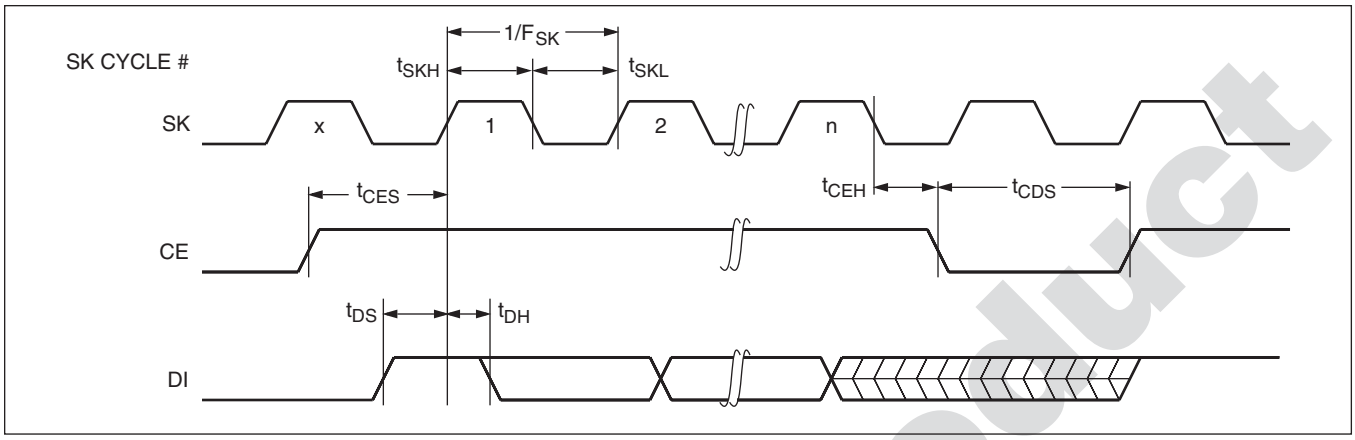
Symbol	Parameter	Min.	Max.	Unit
F_{SK}[3]	SK frequency		1	MHz
t_{SKH}	SK positive pulse width	400		ns
t_{SKL}	SK negative pulse width	400		ns
t_{DS}	Data setup time	400		ns
t_{DH}	Data hold time	80		ns
t_{PD1}	SK to data bit 0 valid		375	ns
t_{PD}	SK to data valid		375	ns
t_{Z}	Chip enable to output high Z		1	µs
t_{CES}	Chip enable setup	800		ns
t_{CEH}	Chip enable hold	350		ns
t_{CDS}	Chip deselect	800		ns

POWER-UP TIMING

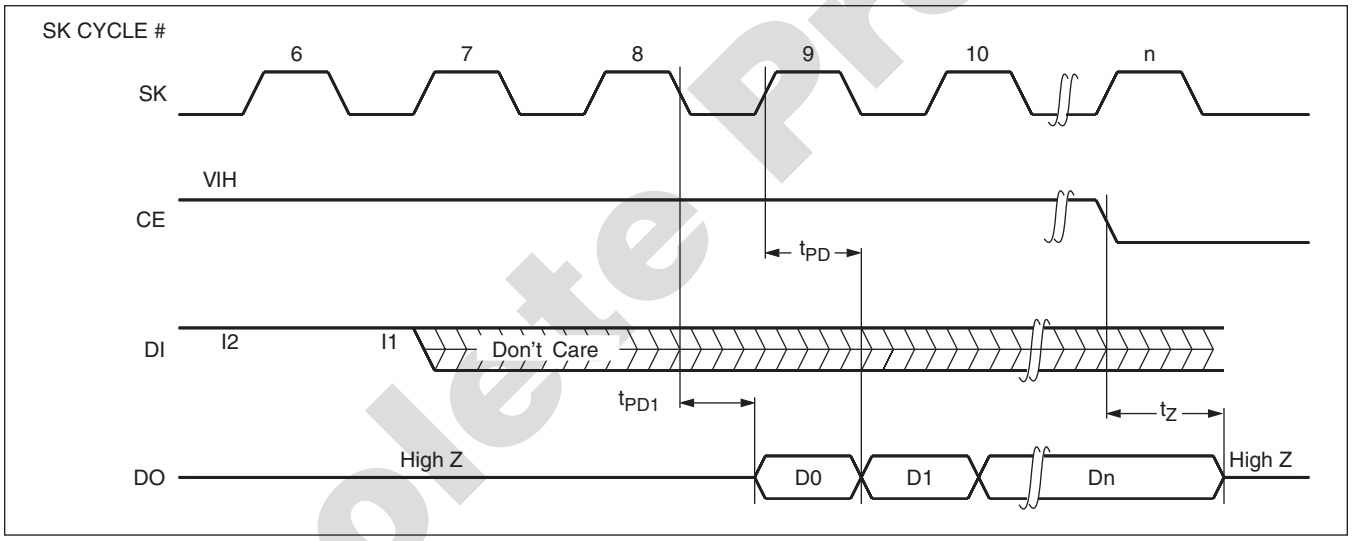
Symbol	Parameter	Max.	Unit
t_{PUR}[4]	Power-up to read operation	200	µs
t_{PUW}[4]	power-up to write or store operation	5	ms

Notes: (3) SK rise and fall times must be less than 50ns.
(4) t_{PUR} and t_{PUW} are the delays required from the time V_{CC} is stable until the specified operation can be initiated. These parameters are periodically sampled and not 100% tested.

Write Cycle



Read Cycle



NONVOLATILE OPERATIONS

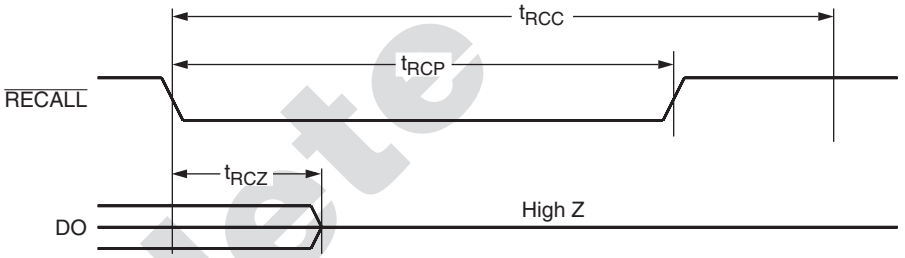
Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	Software Instruction	Write Enable Latch State	Previous Recall Latch State
Hardware recall	1	0	NOP(5)	X	X
Software recall	1	1	RCL	X	X
Hardware store	0	1	NOP(5)	SET	SET
Software store	1	1	STO	SET	SET

ARRAY RECALL LIMITS

Symbol	Parameter	Min.	Max.	Unit
t_{RCC}	Recall cycle time	2		µs
t_{RCP}	Recall pulse width(6)	500		ns
t_{RCZ}	Recall to output in high Z		500	ns

Notes: (5) NOP designates when the X24C44 is not currently executing an instruction.
(6) $\overline{\text{RECALL}}$ rise time must be <10µs.

Recall Timing

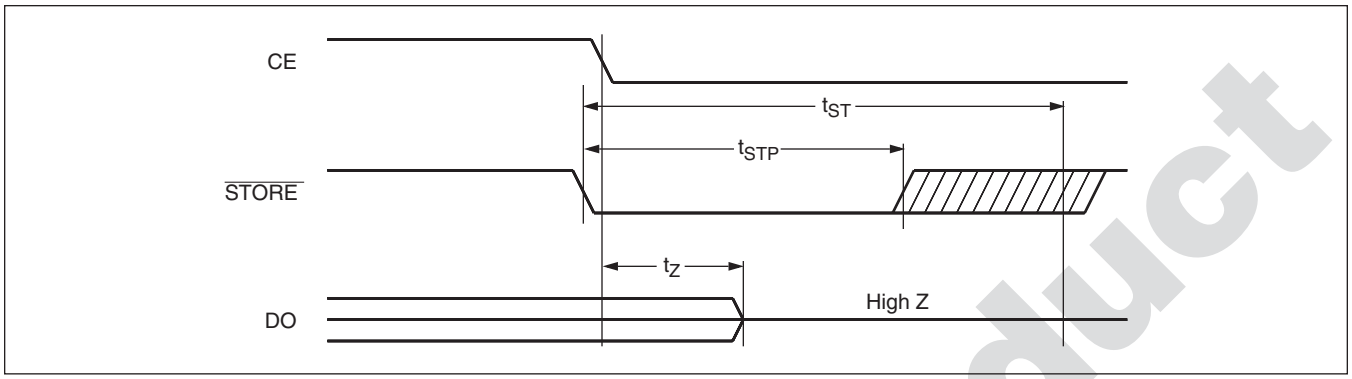


STORE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(7)	Max.	Unit
t_{ST}	Store time		2	5	ms
t_{STP}	Store pulse width	200			ns
t_Z	CE to output in high Z			1	µs
V_{CC}	Store inhibit		3		V

Note: (7) Typical values are for T_A = 25°C and nominal supply voltage.

Store Timing

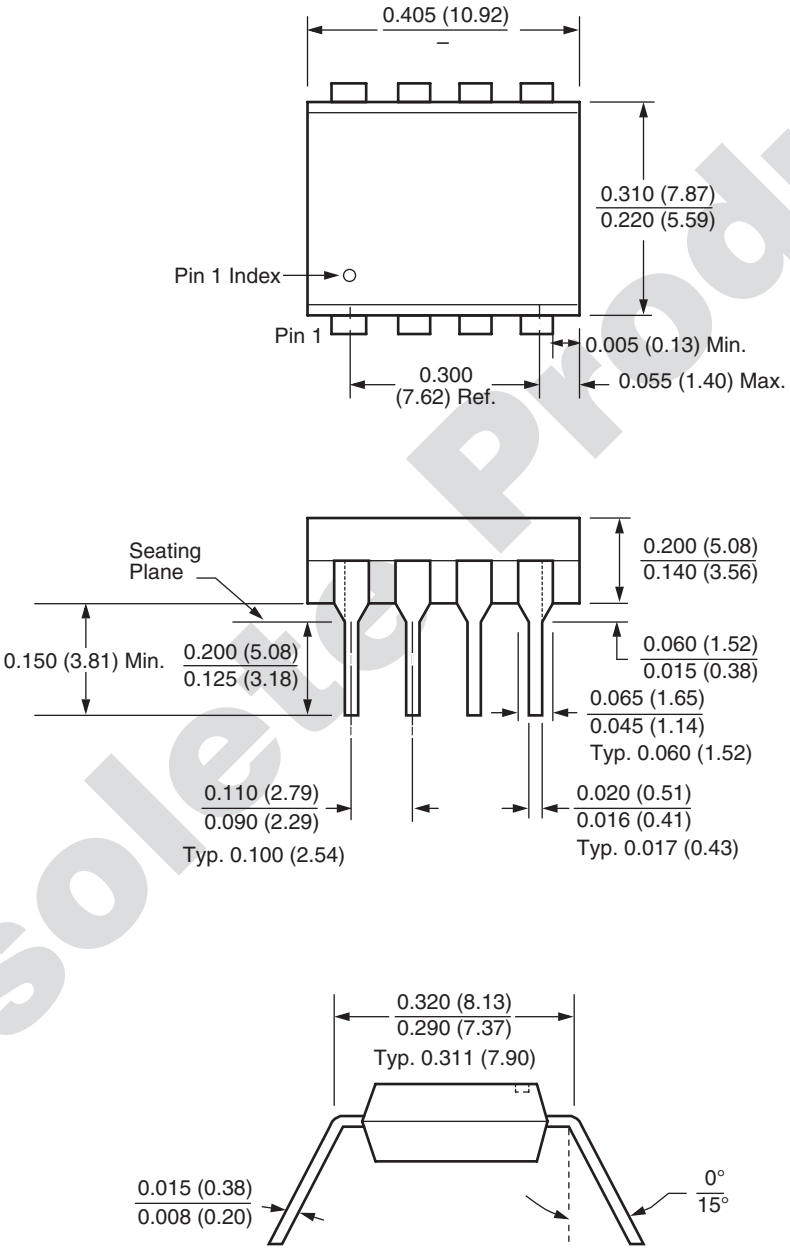


SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

PACKAGING INFORMATION

8-Lead Hermetic, DIP, Package Type D8

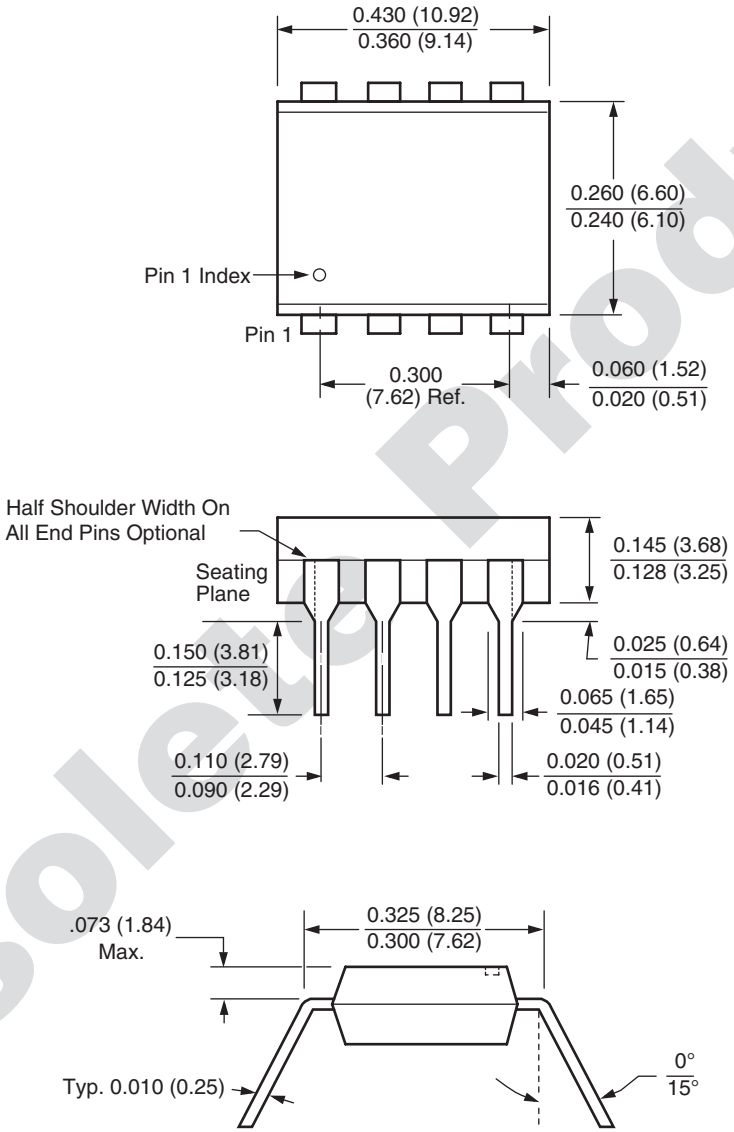


NOTE:

1. ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

PACKAGING INFORMATION

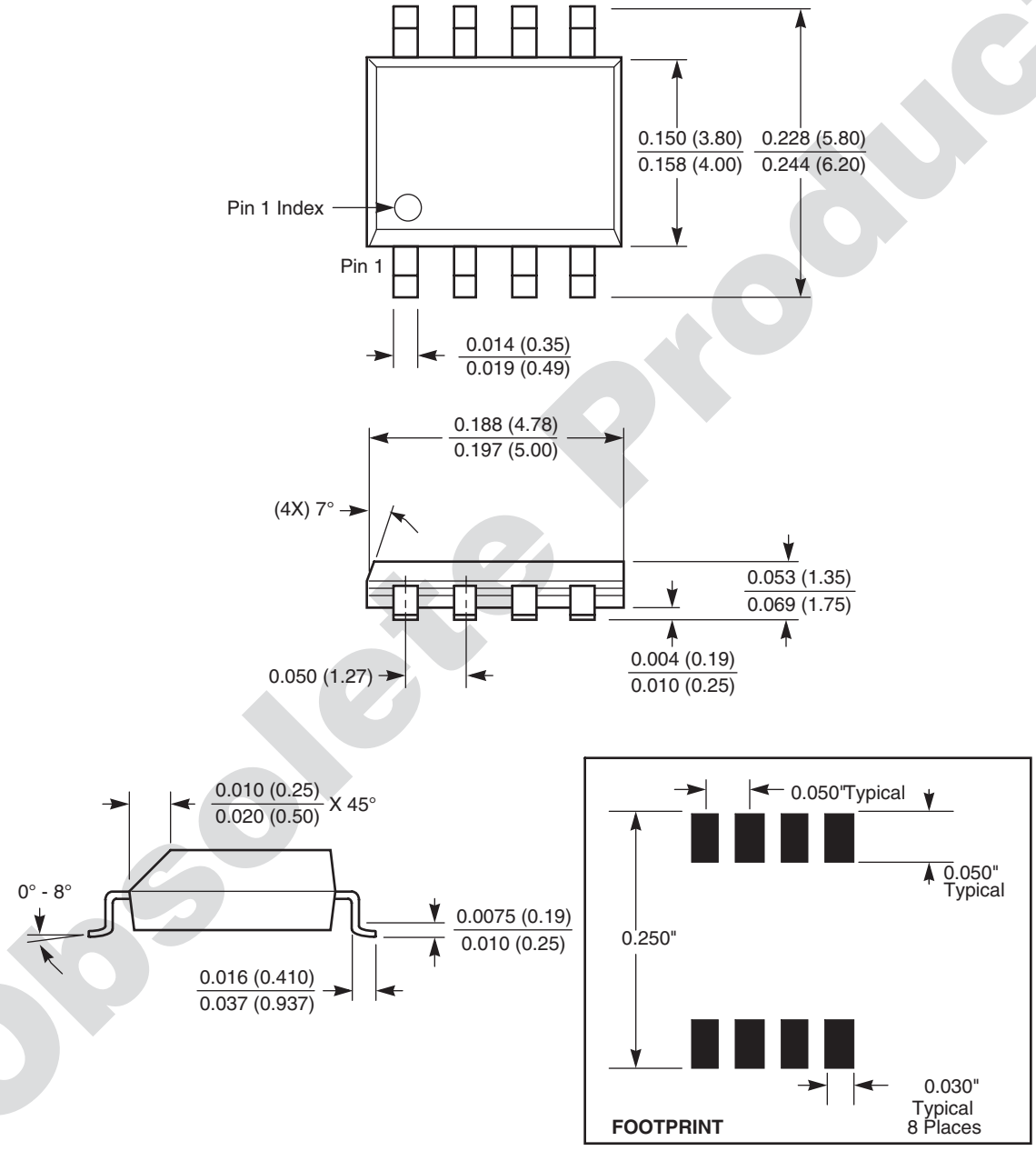
8-Lead Plastic, PDIP, Package Code P8



NOTE:
1. **ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)**
2. **PACKAGE DIMENSIONS EXCLUDE MOLDING FLASH**

PACKAGING INFORMATION

8-Lead Plastic, SOIC, Package Code S8



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)

Ordering Information