

Mobile LPDDR SDRAM AT Addendum

MT46H8M16LF – 2 Meg x 16 x 4 banks

MT46H4M32LF – 1 Meg x 32 x 4 banks

Features

- Vdd/Vddq = 1.70–1.95V
- Bidirectional data strobe per byte of data (DQS)
- Internal, pipelined double data rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- Four internal banks for concurrent operation
- Data masks (DM) for masking write data—one mask per byte
- Programmable burst lengths (BL): 2, 4, 8, or 16
- Concurrent auto precharge option is supported
- Auto refresh mode
- 1.8V LVCMOS-compatible inputs
- Deep power-down (DPD)
- Status read register (SRR)
- Selectable output drive strength (DS)
- Clock stop capability

Options

- Vdd/Vddq
 - 1.8V/1.8V
- Configuration
 - 8 Meg x 16 (2 Meg x 16 x 4 banks)
 - 4 Meg x 32 (1 Meg x 32 x 4 banks)
- Row-size option
 - JEDEC-standard option
- Plastic “green” package
 - 60-ball VFBGA (8mm x 9mm)¹
 - 90-ball VFBGA (10mm x 13mm)²
- Timing – cycle time
 - 5ns @ CL = 3
 - 5.4ns @ CL = 3
 - 6ns @ CL = 3
 - 7.5ns @ CL = 3
- Operating temperature range³
 - Automotive (–40°C to +105°C)
- Design revision

Marking

H

8M16

4M32

LF

BF

B5

-5

-54

-6

-75

AT

:K

Table 1: Key Timing Parameters (CL = 3)

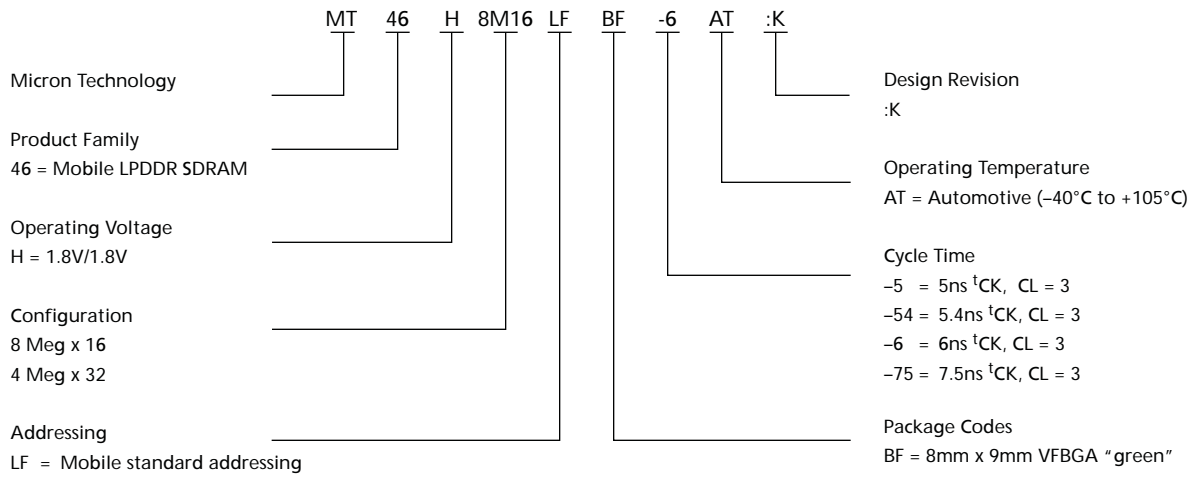
Speed Grade	Clock Rate (MHz)	Access Time
-5	200	5ns
-54	185	5ns
-6	166	5ns
-75	133	6ns

- Notes: 1. Available only for x16 configuration.
 2. Available only for x32 configuration.
 3. Specified as ambient temperature (T_A).

Table 2: Configuration Addressing

Architecture	8 Meg x 16	4 Meg x 32
Configuration	2 Meg x 16 x 4 banks	1 Meg x 32 x 4 banks
Refresh count	4K	4K
Row addressing	4K A[11:0]	4K A[11:0]
Column addressing	512 A[8:0]	256 A[7:0]

Figure 1: 128Mb Mobile DDR Part Numbering



FBGA Part Marking

Due to space limitations, FBGA-packaged components have an abbreviated part marking that is different from the part number. Micron's FBGA part marking decoder is available at www.micron.com/decoder.

General Description

The information in this addendum is specific to the 128Mb, 8 Meg x 16 and 4 Meg x 32 Mobile DDR SDRAM, VFBGA-packaged part. For detailed specification information, refer to the product data sheet available on Micron's Web site: www.micron.com.

Note: Any values specified in this addendum replace the same values listed in the data sheet for this product.

Electrical Specifications

The values listed in tables 3 and 4 reflect all specification relaxations necessary to support device operation in the automotive temperature range of -40°C to 105°C.

Table 3: Idd Specifications and Conditions (x16/x32)

Notes: 1–5 apply to all parameters/conditions in this table; see the general market product data sheet for applicable notes; Vdd/Vddq = 1.70–1.95V

Parameter/Condition	Symbol	-5, -54, -6, -75	Unit	
Self Refresh: CKE = LOW; tCK = tCK (MIN); Address and control inputs are stable; Data bus inputs are stable	Full array, 105°C	Idd6A	550	µA
	Half array, 105°C	Idd6A	335	µA
	1/4 array, 105°C	Idd6A	235	µA
	1/8 array, 105°C	Idd6A	160	µA
	1/16 array, 105°C	Idd6A	120	µA

Table 4: Electrical Characteristics and Recommended AC Operating Conditions

Notes: 1–9 apply to all parameters in this table; see the general market product data sheet for applicable notes; Vdd/Vddq = 1.70–1.95V

Parameter	Symbol	-5		-54		-6		-75		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Refresh period	tREF	–	32	–	32	–	32	–	32	ms
Average periodic refresh interval	tREFI	–	7.8	–	7.8	–	7.8	–	7.8	µs

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.



Revision History

Rev. D	1/09
<ul style="list-style-type: none">• “Options” on page 1: For automotive operating temperature range, added note 3.• Changed document status to Production.	
Rev. C	09/08
<ul style="list-style-type: none">• Table 3, “Idd Specifications and Conditions (x16/x32),” on page 3: Changed text from 85°C to 105°C.	
Rev. B	07/08
<ul style="list-style-type: none">• Corrected first-page addressing and part-numbering section header information.	
Rev. A	07/08
<ul style="list-style-type: none">• Initial release.	