

Features

- Serial Peripheral Interface (SPI) Compatible
- Supports SPI Modes 0 (0,0) and 3 (1,1)
- Data Sheet Describes Mode 0 Operation
- Low-voltage and Standard-voltage Operation
 - 1.8 (VCC = 1.8V to 5.5V)
- 20 MHz Clock Rate (5V)
- 64-byte Page Mode and Byte Write Operation
- Block Write Protection
 - Protect 1/4, 1/2, or Entire Array
- Write Protect (WP) Pin and Write Disable Instructions for Both Hardware and Software Data Protection
- Self-timed Write Cycle (5 ms Max)
- High-reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: >100 Years
- Green (Pb/Halide-free/RoHS Compliant) Packaging Options
- Die Sales: Wafer Form, Waffle Pack, and Bumped Die

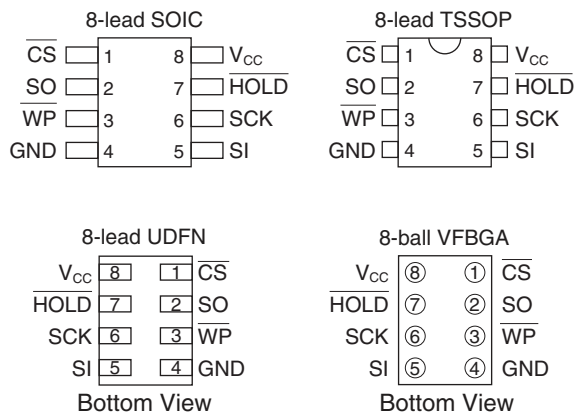
Description

The AT25128B/256B provides 131,072/262,144 bits of serial electrically-erasable programmable read only memory (EEPROM) organized as 16,384/32,768 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low-power and low-voltage operation are essential. The devices are available in space saving 8-lead SOIC, 8-lead TSSOP, 8-ball VFBGA and 8-lead UDFN packages. In addition, the entire family is available in 1.8V (1.8V to 5.5V).

The AT25128B/256B is enabled through the Chip Select pin (\overline{CS}) and accessed via a 3-wire interface consisting of Serial Data Input (SI), Serial Data Output (SO), and Serial Clock (SCK). All programming cycles are completely self-timed, and no separate Erase cycle is required before Write.

Table 0-1. Pin Configurations

| Pin | Function |
|-----------------|-----------------------|
| \overline{CS} | Chip Select |
| SCK | Serial Data Clock |
| SI | Serial Data Input |
| SO | Serial Data Output |
| GND | Ground |
| V _{CC} | Power Supply |
| WP | Write Protect |
| HOLD | Suspends Serial Input |



Block Write protection is enabled by programming the status register with top 1/4, top 1/2 or entire array of write protection. Separate Program Enable and Program Disable instructions are provided for additional data protection. Hardware data protection is provided via the WP pin to protect against inadvertent write attempts to the status register. The HOLD pin may be used to suspend any serial communication without resetting the serial sequence.



SPI Serial EEPROMS

128K (16,384 x 8)

256K (32,768 x 8)

AT25128B AT25256B



1. Absolute Maximum Ratings*

| | |
|---|--|
| Operating Temperature.....-55°C to +125°C | *NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. |
| Storage Temperature-65°C to + 150°C | |
| Voltage on Any Pin with Respect to Ground.....-1.0 V +7.0V | |
| Maximum Operating Voltage..... 6.25V | |
| DC Output Current 5.0 mA | |

Figure 1-1. Block Diagram

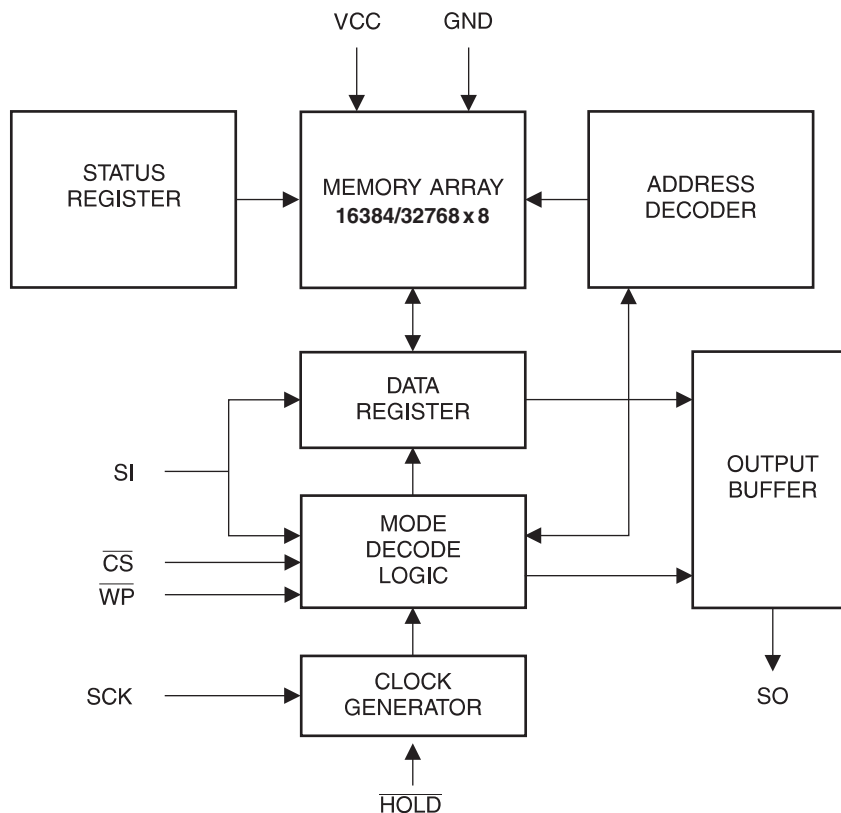


Table 1-1. Pin Capacitance ⁽¹⁾

Applicable over recommended operating range from $T_A = 25^\circ\text{C}$, $f = 1.0\text{ MHz}$, $V_{CC} = +5.0\text{V}$ (unless otherwise noted)

| Symbol | Test Conditions | Max | Units | Conditions |
|-----------|--|-----|-------|-----------------------|
| C_{OUT} | Output Capacitance (SO) | 8 | pF | $V_{OUT} = 0\text{V}$ |
| C_{IN} | Input Capacitance (\overline{CS} , SCK, SI, \overline{WP} , HOLD) | 6 | pF | $V_{IN} = 0\text{V}$ |

Notes: 1. This parameter is characterized and is not 100% tested.

Table 1-2. DC Characteristics

Applicable over recommended operating range from $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$, $V_{CC} = +1.8\text{V}$ to $+5.5\text{V}$ (unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Units |
|----------------|---------------------|---|------------------------------------|-----|---------------------|---------------|
| V_{CC1} | Supply Voltage | | 1.8 | | 5.5 | V |
| V_{CC2} | Supply Voltage | | 2.5 | | 5.5 | V |
| V_{CC3} | Supply Voltage | | 4.5 | | 5.5 | V |
| I_{CC1} | Supply Current | $V_{CC} = 5.0\text{V}$ at 20 MHz, SO = Open, Read | | 9.0 | 10.0 | mA |
| I_{CC2} | Supply Current | $V_{CC} = 5.0\text{V}$ at 10 MHz, SO = Open, Read, Write | | 5.0 | 7.0 | mA |
| I_{CC3} | Supply Current | $V_{CC} = 5.0\text{V}$ at 1 MHz, SO = Open, Read, Write | | 2.2 | 3.5 | mA |
| I_{SB1} | Standby Current | $V_{CC} = 1.8\text{V}$, $\overline{CS} = V_{CC}$ | | 0.2 | 3.0 | μA |
| I_{SB2} | Standby Current | $V_{CC} = 2.5\text{V}$, $\overline{CS} = V_{CC}$ | | 0.5 | 3.0 | μA |
| I_{SB3} | Standby Current | $V_{CC} = 5.0\text{V}$, $\overline{CS} = V_{CC}$ | | 2.0 | 5.0 | μA |
| I_{IL} | Input Current | $V_{IN} = 0\text{V}$ to V_{CC} | -3.0 | | 3.0 | μA |
| I_{OL} | Output Leakage | $V_{IN} = 0\text{V}$ to V_{CC} , $T_{AC} = 0^\circ\text{C}$ to 70°C | -3.0 | | 3.0 | μA |
| $V_{IL}^{(1)}$ | Input Low-voltage | | -1.0 | | $V_{CC} \times 0.3$ | V |
| $V_{IH}^{(1)}$ | Input High-voltage | | $V_{CC} \times 0.7$ | | $V_{CC} + 0.5$ | V |
| V_{OL1} | Output Low-voltage | $3.6\text{V} \leq V_{CC} \leq 5.5\text{V}$ | $I_{OL} = 3.0\text{ mA}$ | | 0.4 | V |
| V_{OH1} | Output High-voltage | | $I_{OH} = -1.6\text{ mA}$ | | $V_{CC} - 0.8$ | V |
| V_{OL2} | Output Low-voltage | $1.8\text{V} \leq V_{CC} \leq 3.6\text{V}$ | $I_{OL} = 0.15\text{ mA}$ | | 0.2 | V |
| V_{OH2} | Output High-voltage | | $I_{OH} = -100\text{ }\mu\text{A}$ | | $V_{CC} - 0.2$ | V |

Notes: 1. V_{IL} min and V_{IH} max are reference only and are not tested.

Table 1-3. AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$,
 $CL = 1$ TTL Gate and 30 pF (unless otherwise noted)

| Symbol | Parameter | Voltage | Min | Max | Units |
|------------------|-------------------------------------|-------------------------------|-------------------|----------------|---------------|
| f_{SCK} | SCK Clock Frequency | 4.5–5.5 2.5–5.5 1.8–5.5 | 0 0 0 | 20 10 5 | MHz |
| t_{RI} | Input Rise Time | 4.5–5.5 2.5–5.5 1.8–5.5 | | 2 2 2 | μs |
| t_{FI} | Input Fall Time | 4.5–5.5 2.5–5.5 1.8–5.5 | | 2 2 2 | μs |
| t_{WH} | SCK High Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 20 40 80 | | ns |
| t_{WL} | SCK Low Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 20 40 80 | | ns |
| t_{CS} | $\overline{\text{CS}}$ High Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 100 100 200 | | ns |
| t_{CSS} | $\overline{\text{CS}}$ Setup Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 100 100 200 | | ns |
| t_{CSH} | $\overline{\text{CS}}$ Hold Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 100 100 200 | | ns |
| t_{SU} | Data In Setup Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 5 10 20 | | ns |
| t_{H} | Data In Hold Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 5 10 20 | | ns |
| t_{HD} | $\overline{\text{HOLD}}$ Setup Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 5 10 20 | | ns |
| t_{CD} | $\overline{\text{HOLD}}$ Hold Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 5 10 20 | | ns |
| t_{V} | Output Valid | 4.5–5.5 2.5–5.5 1.8–5.5 | 0 0 0 | 20 40 80 | ns |
| t_{HO} | Output Hold Time | 4.5–5.5 2.5–5.5 1.8–5.5 | 0 0 0 | | ns |

Table 1-3. AC Characteristics (Continued)

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = \text{As Specified}$,
CL = 1 TTL Gate and 30 pF (unless otherwise noted)

| Symbol | Parameter | Voltage | Min | Max | Units |
|------------------|---|---------|-----|-----|--------------|
| t_{LZ} | $\overline{\text{HOLD}}$ to Output Low Z | 4.5–5.5 | 0 | 25 | ns |
| | | 2.5–5.5 | 0 | 50 | |
| | | 1.8–5.5 | 0 | 100 | |
| t_{HZ} | $\overline{\text{HOLD}}$ to Output High Z | 4.5–5.5 | | 25 | ns |
| | | 2.5–5.5 | | 50 | |
| | | 1.8–5.5 | | 100 | |
| t_{DIS} | Output Disable Time | 4.5–5.5 | | 25 | ns |
| | | 2.5–5.5 | | 50 | |
| | | 1.8–5.5 | | 100 | |
| t_{WC} | Write Cycle Time | 4.5–5.5 | | 5 | ms |
| | | 2.5–5.5 | | 5 | |
| | | 1.8–5.5 | | 5 | |
| Endurance (1) | 3.3V, 25°C , Page Mode | | 1M | | Write Cycles |

Notes: 1. This parameter is characterized and is not 100% tested. Contact Atmel for further information.

2. Serial Interface Description

MASTER: The device that generates the serial clock.

SLAVE: Because the serial clock pin (SCK) is always an input, the AT25128B/256B always operates as a slave.

TRANSMITTER/RECEIVER: The AT25128B/256B has separate pins designated for data transmission (SO) and reception (SI).

MSB: The Most Significant Bit (MSB) is the first bit transmitted and received.

SERIAL-OP CODE: After the device is selected with $\overline{\text{CS}}$ going low, the first byte will be received. This byte contains the op-code that defines the operations to be performed.

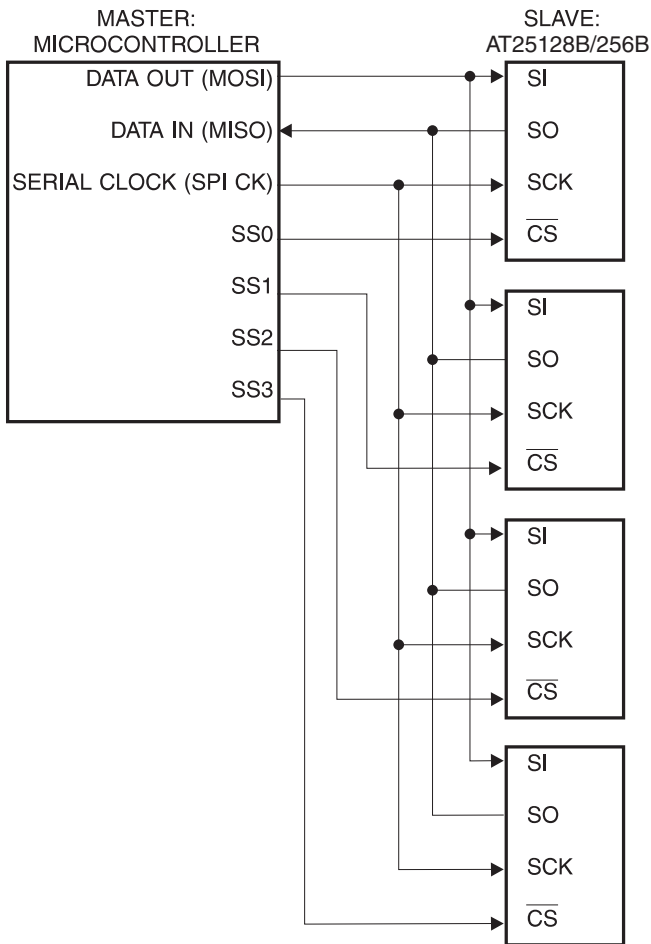
INVALID OP-CODE: If an invalid op-code is received, no data will be shifted into the AT25128B/256B, and the serial output pin (SO) will remain in a high impedance state until the falling edge of $\overline{\text{CS}}$ is detected again. This will reinitialize the serial communication.

CHIP SELECT: The AT25128B/256B is selected when the $\overline{\text{CS}}$ pin is low. When the device is not selected, data will not be accepted via the SI pin, and the serial output pin (SO) will remain in a high impedance state.

HOLD: The $\overline{\text{HOLD}}$ pin is used in conjunction with the $\overline{\text{CS}}$ pin to select the AT25128B/256B. When the device is selected and a serial sequence is underway, $\overline{\text{HOLD}}$ can be used to pause the serial communication with the master device without resetting the serial sequence. To pause, the $\overline{\text{HOLD}}$ pin must be brought low while the SCK pin is low. To resume serial communication, the $\overline{\text{HOLD}}$ pin is brought high while the SCK pin is low (SCK may still toggle during $\overline{\text{HOLD}}$). Inputs to the SI pin will be ignored while the SO pin is in the high impedance state.

WRITE PROTECT: The write protect pin ($\overline{\text{WP}}$) will allow normal read/write operations when held high. When the $\overline{\text{WP}}$ pin is brought low and WPEN bit is "1", all write operations to the status register are inhibited. $\overline{\text{WP}}$ going low while $\overline{\text{CS}}$ is still low will interrupt a write to the status register. If the internal write cycle has already been initiated, $\overline{\text{WP}}$ going low will have no effect on any write operation to the status register. The $\overline{\text{WP}}$ pin function is blocked when the WPEN bit in the status register is "0". This will allow the user to install the AT25128B/256B in a system with the $\overline{\text{WP}}$ pin tied to ground and still be able to write to the status register. All $\overline{\text{WP}}$ pin functions are enabled when the WPEN bit is set to "1".

Figure 2-1. SPI Serial Interface



3. Functional Description

The AT25128B/256B is designed to interface directly with the synchronous serial peripheral interface (SPI) of the 6800 type series of microcontrollers.

The AT25128B/256B utilizes an 8-bit instruction register. The list of instructions and their operation codes are contained in [Table 3-1](#). All instructions, addresses, and data are transferred with the MSB first and start with a high-to-low \overline{CS} transition.

Table 3-1. Instruction Set for the AT25128B/256B

| Instruction Name | Instruction Format | Operation |
|------------------|--------------------|-----------------------------|
| WREN | 0000 X110 | Set Write Enable Latch |
| WRDI | 0000 X100 | Reset Write Enable Register |
| RDSR | 0000 X101 | Read Status Register |
| WRSR | 0000 X001 | Write Status Register |
| READ | 0000 X011 | Read Data from Memory Array |
| WRITE | 0000 X 010 | Write Data to Memory Array |

WRITE ENABLE (WREN): The device will power-up in the write disable state when VCC is applied. All programming instructions must therefore be preceded by a Write Enable instruction.

WRITE DISABLE (WRDI): To protect the device against inadvertent writes, the Write Disable instruction disables all programming modes. The WRDI instruction is independent of the status of the \overline{WP} pin.

READ STATUS REGISTER (RDSR): The Read Status Register instruction provides access to the status register. The Ready/Busy and Write Enable status of the device can be determined by the RDSR instruction. Similarly, the Block Write Protection bits indicate the extent of protection employed. These bits are set by using the WRSR instruction.

Table 3-2. Status Register Format

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|------------------|
| WPEN | X | X | X | BP1 | BP0 | WEN | \overline{RDY} |

Table 3-3. Read Status Register Bit Definition

| Bit | Definition |
|---|--|
| Bit 0 (\overline{RDY}) | Bit 0 = "0" (\overline{RDY}) indicates the device is ready. Bit 0 = "1" indicates the write cycle is in progress. |
| Bit 1 (WEN) | Bit 1 = 0 indicates the device is not write enabled. Bit 1 = "1" indicates the device is write enabled. |
| Bit 2 (BP0) | See Table 2-4 on page 9 . |
| Bit 3 (BP1) | See Table 2-4 on page 9 . |
| Bits 4 – 6 are 0s when device is not an internal write cycle. | |
| Bit 7 (WPEN) | See Table 3-5 on page 8 |
| Bits 0 – 7 are "1"s during an internal write cycle. | |

WRITE STATUS REGISTER (WRSR): The WRSR instruction allows the user to select one of four levels of protection. The AT25128B/256B is divided into four array segments. Top quarter (1/4), top half (1/2), or all of the memory segments can be protected. Any of the data within any selected segment will therefore be read only. The block write protection levels and corresponding status register control bits are shown in Table 2-4.

The three bits, BP0, BP1, and WPEN are nonvolatile cells that have the same properties and functions as the regular memory cells (e.g. WREN, tWC, RDSR)

Table 3-4. Block Write Protect Bits.

| Level | Status Register Bits | | Array Addresses Protected | |
|---------|----------------------|-----|---------------------------|-------------|
| | BP1 | BP0 | AT25128B | AT25256B |
| 0 | 0 | 0 | None | None |
| 1 (1/4) | 0 | 1 | 3000 – 3FFF | 6000 – 7FFF |
| 2 (1/2) | 1 | 0 | 2000 – 3FFF | 4000 – 7FFF |
| 3 (All) | 1 | 1 | 0000 – 3FFF | 0000 – 7FFF |

The WRSR instruction also allows the user to enable or disable the write protect (\overline{WP}) pin through the use of the write protect enable (WPEN) bit. Hardware write protection is enabled when the \overline{WP} pin is low and the WPEN bit is “1”. Hardware write protection is disabled when either the \overline{WP} pin is high or the WPEN bit is “0”. When the device is hardware write protected, writes to the Status Register, including the Block Protect bits and the WPEN bit, and the blockprotected sections in the memory array are disabled. Writes are only allowed to sections of the memory which are not block-protected.

Note: When the WPEN bit is hardware write protected, it cannot be changed back to “0”, as long as the \overline{WP} pin is held low.

Table 3-5. WPEN Operation

| WPEN | \overline{WP} | WEN | Protected Blocks | Unprotected Blocks | Status Register |
|------|-----------------|-----|------------------|--------------------|-----------------|
| 0 | X | 0 | Protected | Protected | Protected |
| 0 | X | 1 | Protected | Writable | Writable |
| 1 | Low | 0 | Protected | Protected | Protected |
| 1 | Low | 1 | Protected | Writable | Protected |
| X | High | 0 | Protected | Protected | Protected |
| X | High | 1 | Protected | Writable | Writable |

READ SEQUENCE (READ): Reading the AT25128B/256B via the SO pin requires the following sequence. After the \overline{CS} line is pulled low to select a device, the Read op-code is transmitted via the SI line followed by the byte address to be read (Table 2-6). Upon completion, any data on the SI line will be ignored. The data (D7 - D0) at the specified address is then shifted out onto the SO line. If only one byte is to be read, the \overline{CS} line should be driven high after the data comes out. The read sequence can be continued since the byte address is automatically incremented and data will continue to be shifted out. When the highest address is reached, the address counter will roll over to the lowest address allowing the entire memory to be read in one continuous read cycle.

WRITE SEQUENCE (WRITE): In order to program the AT25128B/256B, two separate instructions must be executed. First, the device must be write enabled via the Write Enable (WREN) Instruction. Then a Write instruction may be executed. Also, the address of the memory location(s) to be programmed must be outside the protected address field location selected by the Block Write Protection Level. During an internal write cycle, all commands will be ignored except the RDSR instruction.

A Write Instruction requires the following sequence. After the \overline{CS} line is pulled low to select the device, the Write op-code is transmitted via the SI line followed by the byte address and the data (D7 - D0) to be programmed (see Table 2-6 for the address key). Programming will start after the \overline{CS} pin is brought high. (The Low-to-High transition of the \overline{CS} pin must occur during the SCK low time immediately after clocking in the D0 (LSB) data bit.

The Ready/Busy status of the device can be determined by initiating a Read Status Register (RDSR) Instruction. If Bit 0 = 1, the Write cycle is still in progress. If Bit 0 = 0, the Write cycle has ended. Only the Read Status Register instruction is enabled during the Write programming cycle.

The AT25128B/256B is capable of a 64-byte Page Write operation. After each byte of data is received, the six low order address bits are internally incremented by one; the high order bits of the address will remain constant. If more than 64 bytes of data are transmitted, the address counter will roll over and the previously written data will be overwritten. The AT25128B/256B is automatically returned to the write disable state at the completion of a Write cycle.

Note: If the device is not write enabled (WREN), the device will ignore the Write instruction and will return to the standby state, when \overline{CS} is brought high. A new \overline{CS} falling edge is required to re-initiate the serial communication.

Table 3-6. Address Key

| Address | AT25128B | AT25256B |
|-----------------|-------------------|----------------|
| A_N | $A_{13} - A_0$ | $A_{14} - A_0$ |
| Don't Care Bits | $A_{15} - A_{14}$ | A_{15} |

4. Timing Diagram (for SPI Mode 0 (0,0))

Figure 4-1. Synchronous Data Timing

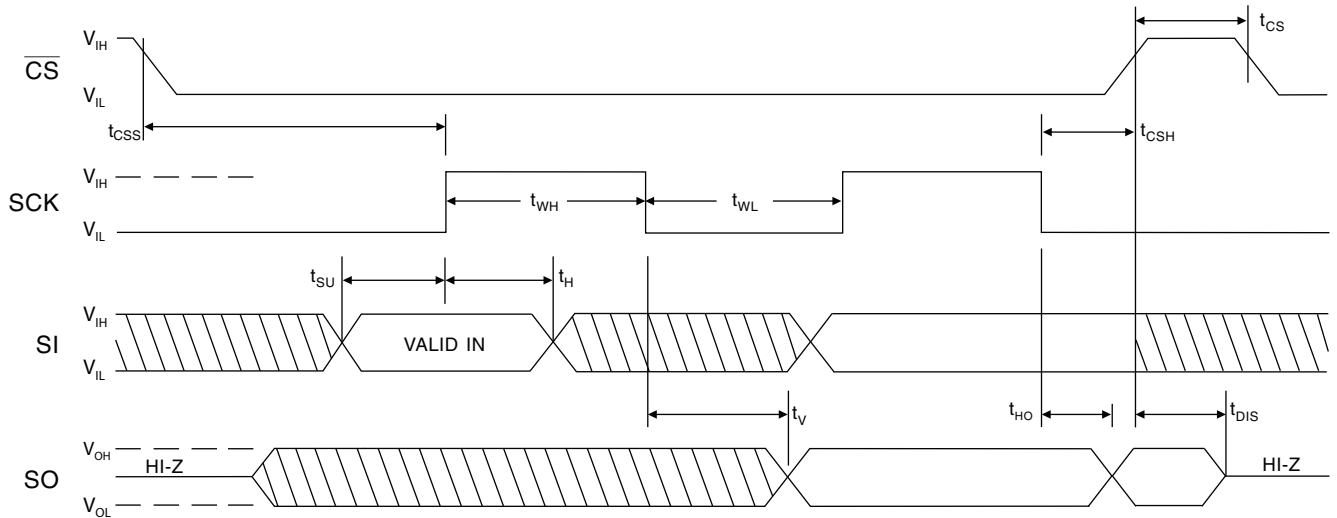


Figure 4-2. WREN Timing

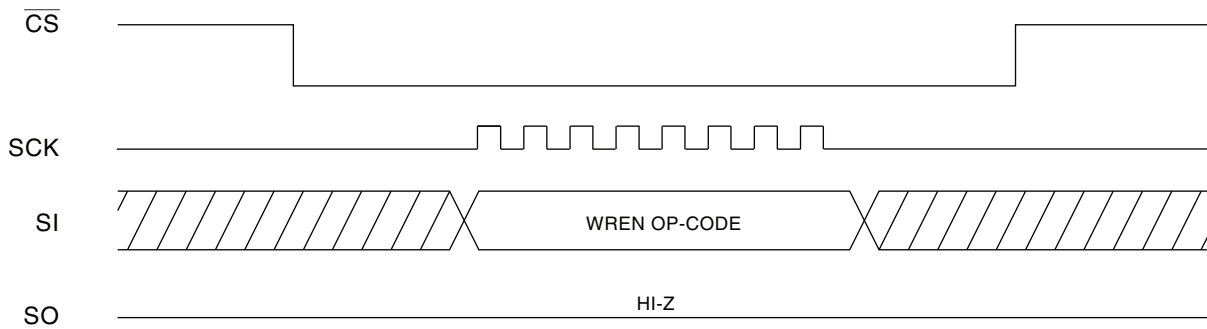


Figure 4-3. WRDI Timing

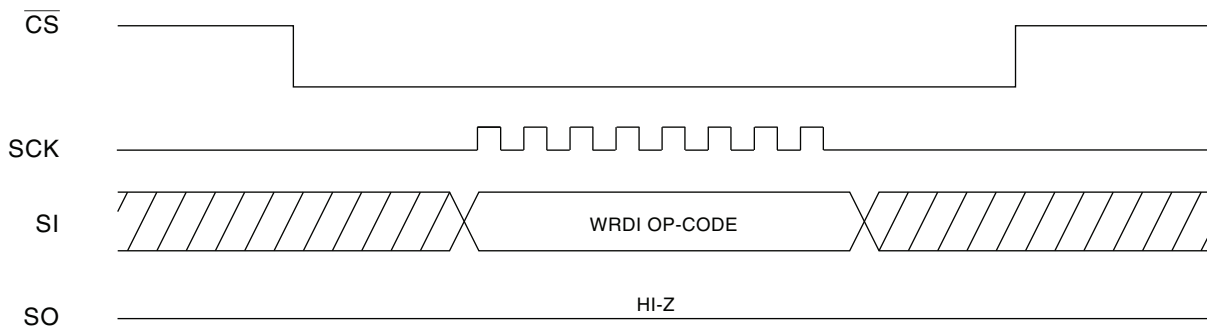


Figure 4-4. RDSR Timing

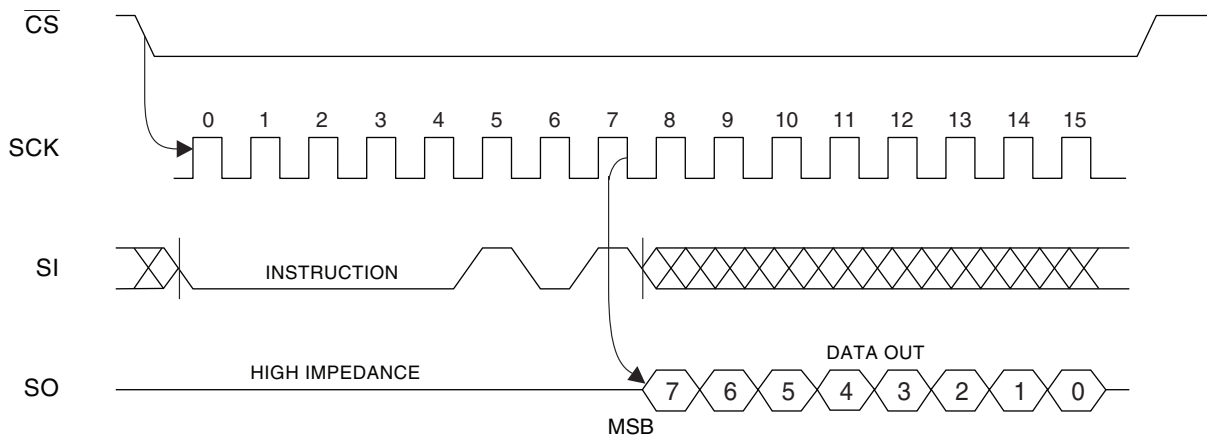


Figure 4-5. WRSR Timing

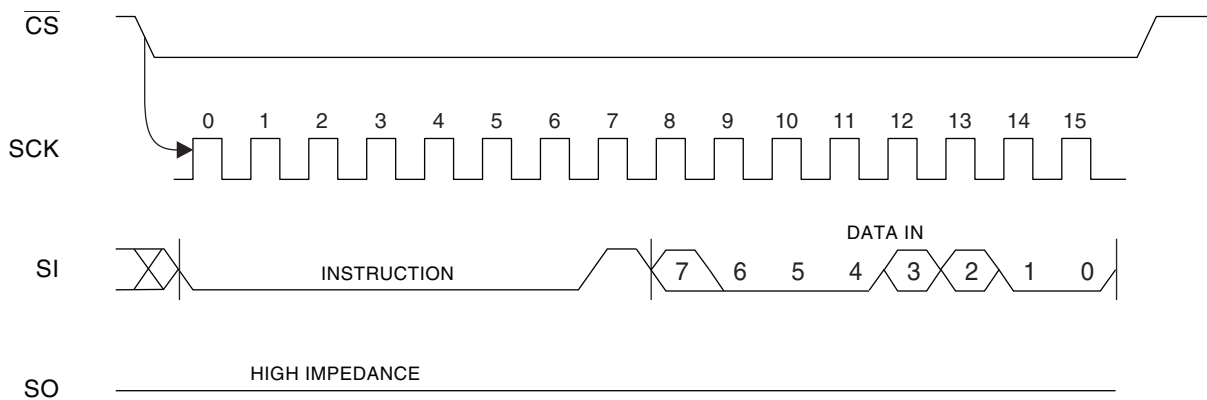


Figure 4-6. READ Timing

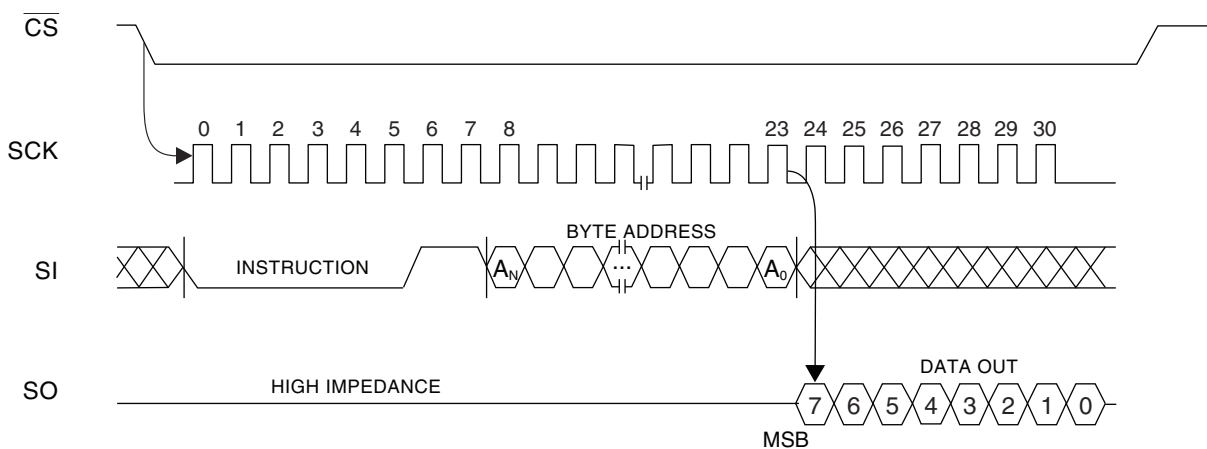


Figure 4-7. WRITE Timing

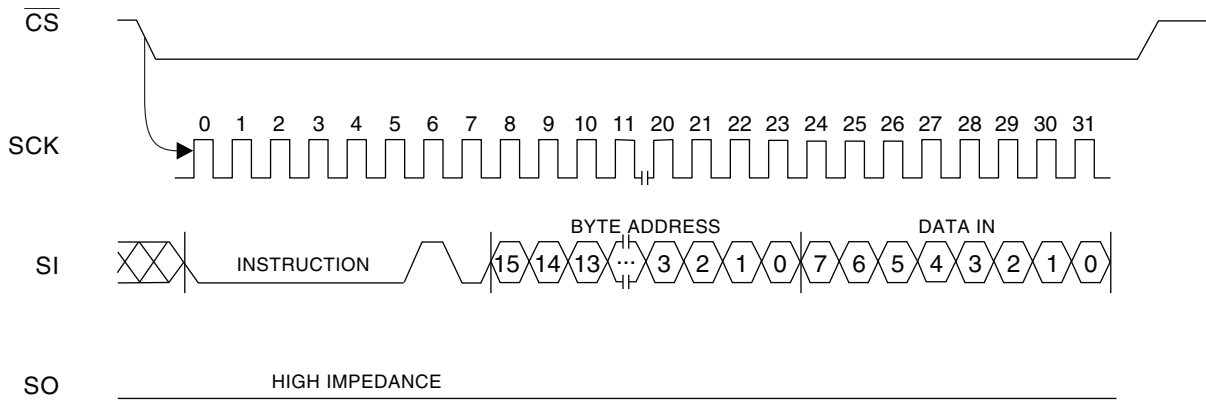
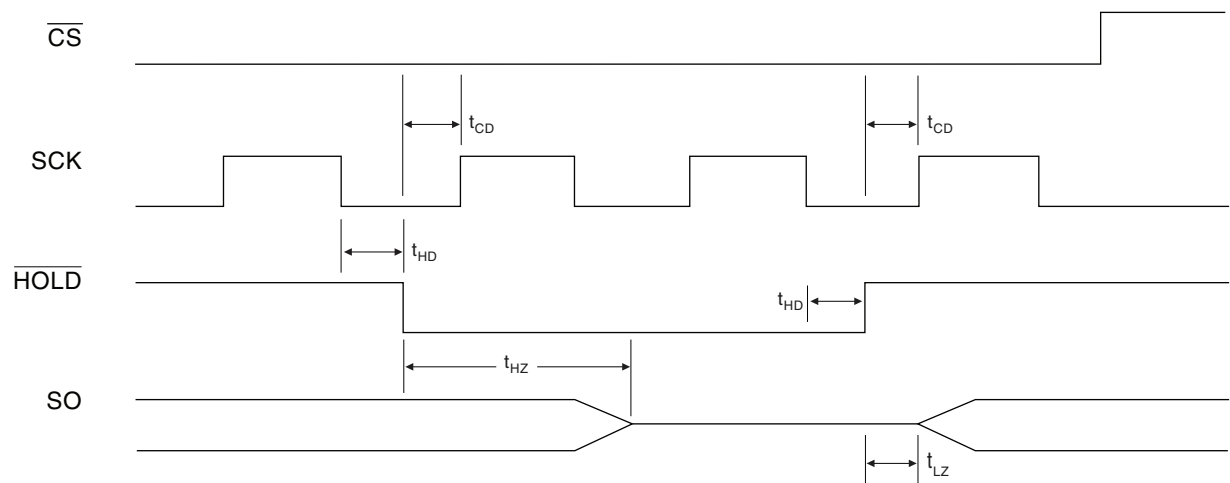
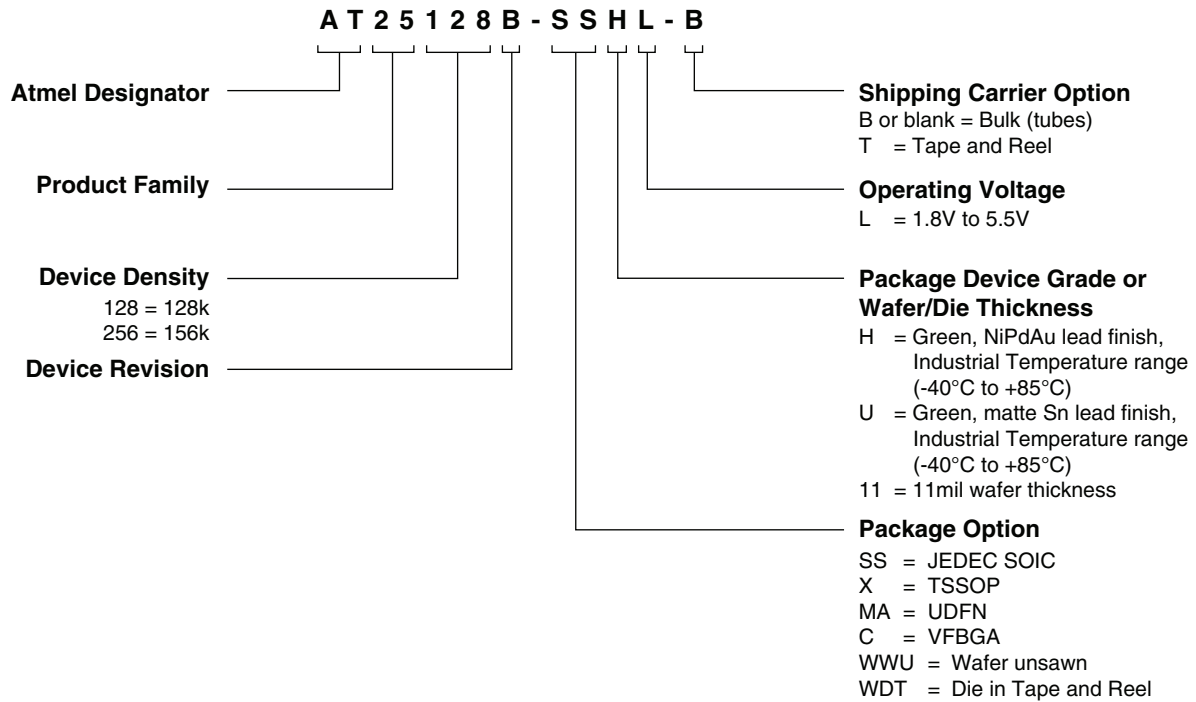


Figure 4-8. $\overline{\text{HOLD}}$ Timing



5. Ordering Code Detail



AT25128B-SSHL

[illegible]

Top Mark

| | | |
|----------------------------|----------------------|----------------|
| PIN 1 INDICATOR (DOT) | @ = Country of Ass'y | |
| | Y = SEAL YEAR | WW = SEAL WEEK |
| * --- --- --- --- --- --- | 8: 2008 | 2: 2012 |
| A T H Y W W | 9: 2009 | 3: 2013 |
| --- --- --- --- --- --- | 0: 2010 | 4: 2014 |
| 5 D B L @ | 1: 2011 | 5: 2015 |
| --- --- --- --- --- --- | | :: : :::: : |
| ATMEL LOT NUMBER | | :: : :::: :: |
| --- --- --- --- --- --- | | 52 = Week 52 |

Top Mark

| | |
|-----------------------|---------------------------------------|
| --- --- --- | Y = YEAR OF ASSEMBLY |
| 5 D B | @ = Country of Ass'y |
| --- --- --- | XX= ATMEL LOT NUMBER TO COORESPOND |
| H L @ | WITH TRACE CODE LOG BOOK. |
| --- --- --- | (e.g. XX = AA, AB, AC,... AX, AY, AZ) |
| Y X X | Y = SEAL YEAR |
| --- --- --- | 6: 2006 0: 2010 |
| * | 7: 2007 1: 2011 |
| | 8: 2008 2: 2012 |
| PIN 1 INDICATOR (DOT) | 9: 2009 3: 2013 |

AT25128B-CUL

Top Mark

```

|---|---|---|---|
 5   D   B   U
|---|---|---|---|
  B   Y   M   X   X
|---|---|---|---|
  * <-- PIN 1 INDICATOR

```

B = Country of Origin
Y = One Digit Year Code
M = One Digit Month Code
XX= TRACE CODE (ATMEL LOT NUMBER TO COORESPOND WITH TRACE CODE LOG BOOK)
(e.g. XX = AA, AB, AC, ... YZ, ZZ)

Y = ONE DIGIT YEAR CODE M = SEAL MONTH
4: 2004 7: 2007 (USE ALPHA DESIGNATOR A-L)
5: 2005 8: 2008 A = JANUARY
6: 2006 9: 2009 B = FEBRUARY
 " " " " " " " " " "
 J = OCTOBER
 K = NOVEMBER
 L = DECEMBER

AT25256B-SSHL

Top Mark Seal Year

```

|---|---|---|---|---|---|---|---|
 A   T   M   L   H   Y   W   W
|---|---|---|---|---|---|---|---|
 5   E   B           L           @
|---|---|---|---|---|---|---|---|
  *   LOT NUMBER
|---|---|---|---|---|---|---|---|
  |
  PIN 1 INDICATOR (DOT)

```

@ = Country of Ass'y
Y = SEAL YEAR WW = SEAL WEEK
6: 2006 0: 2010 02 = Week 2
7: 2007 1: 2011 04 = Week 4
8: 2008 2: 2012 :: : : : :
9: 2009 3: 2013 :: : : : :
 50 = Week 50
 52 = Week 52

AT25256B-XHL

Top Mark

```

PIN 1 INDICATOR (DOT)
|
* |---|---|---|---|---|---|
  A   T   H   Y   W   W
  |---|---|---|---|---|---|
  5   E   B   L           @
|---|---|---|---|---|---|
  ATMEL LOT NUMBER
|---|---|---|---|---|---|

```

@ = Country of Ass'y
Y = SEAL YEAR WW = SEAL WEEK
8: 2008 2: 2012 02 = Week 2
9: 2009 3: 2013 04 = Week 4
0: 2010 4: 2014 :: : : : :
1: 2011 5: 2015 :: : : : :
 52 = Week 52



At25256B-MAHL

Top Mark

```

|---|---|---|
 5   E   B
|---|---|---|
 H   L   @
|---|---|---|
 Y   X   X
|---|---|---|
  *
  |

```

PIN 1 INDICATOR (DOT)

Y = YEAR OF ASSEMBLY
 @ = Country of Ass'y
 XX= ATMEL LOT NUMBER TO COORESPOND
 WITH TRACE CODE LOG BOOK.
 (e.g. XX = AA, AB, AC, ... AX, AY, AZ)
 Y = SEAL YEAR
 6: 2006 0: 2010
 7: 2007 1: 2011
 8: 2008 2: 2012
 9: 2009 3: 2013

AT25256B-CUL

Top Mark

```

|---|---|---|---|
 5   E   B   U
|---|---|---|---|
 B   Y   M   X   X
|---|---|---|---|
 * <-- PIN 1 INDICATOR

```

B = Country of Origin
 Y = One Digit Year Code
 M = One Digit Month Code
 XX= TRACE CODE (ATMEL LOT NUMBER TO
 COORESPOND WITH TRACE CODE LOG BOOK)
 (e.g. XX = AA, AB, AC, ... YZ, ZZ)

| | |
|-------------------------|----------------------------|
| Y = ONE DIGIT YEAR CODE | M = SEAL MONTH |
| 4: 2004 7: 2007 | (USE ALPHA DESIGNATOR A-L) |
| 5: 2005 8: 2008 | A = JANUARY |
| 6: 2006 9: 2009 | B = FEBRUARY |
| | " " " " " " " " " " |
| | J = OCTOBER |
| | K = NOVEMBER |
| | L = DECEMBER |

7. Ordering Codes

AT25128B Ordering Information

| Ordering Code | Voltage Range | Package | Operation Range |
|---|---------------|----------|--|
| AT25128B-SSHL-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8S1 | Lead-free/Halogen-free/ Industrial Temperature (-40°C to 85°C) |
| AT25128B-SSHL-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8S1 | |
| AT25128B-XHL-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8A2 | |
| AT25128B-XHL-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8A2 | |
| AT25128B-MAHL-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8MA2 | |
| AT25128B-CUL-T ⁽²⁾ (SnAgCu Ball Finish) | 1.8V to 5.5V | 8U2-1 | |
| AT25128B-WWU11L ⁽³⁾ | 1.8V to 5.5V | Die Sale | Industrial Temperature (-40°C to 85°C) |

- Notes:
1. Bulk delivery in tubes (SOIC and TSSOP 100/tube).
 2. Tape and reel delivery (SOIC 4k/reel. TSSOP, UDFN and VFBGA 5k/reel).
 3. Contact Atmel Sales for Wafer sales.

| Package Type | |
|--------------|---|
| 8S1 | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC) |
| 8A2 | 8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP) |
| 8MA2 | 8-lead, 2.00mm x 3.00mm Body, 0.50 mm Pitch, Dual No Lead Package (UDFN) |
| 8U2-1 | 8-ball, die Ball Grid Array Package (VFBGA) |



AT25256B Ordering Information

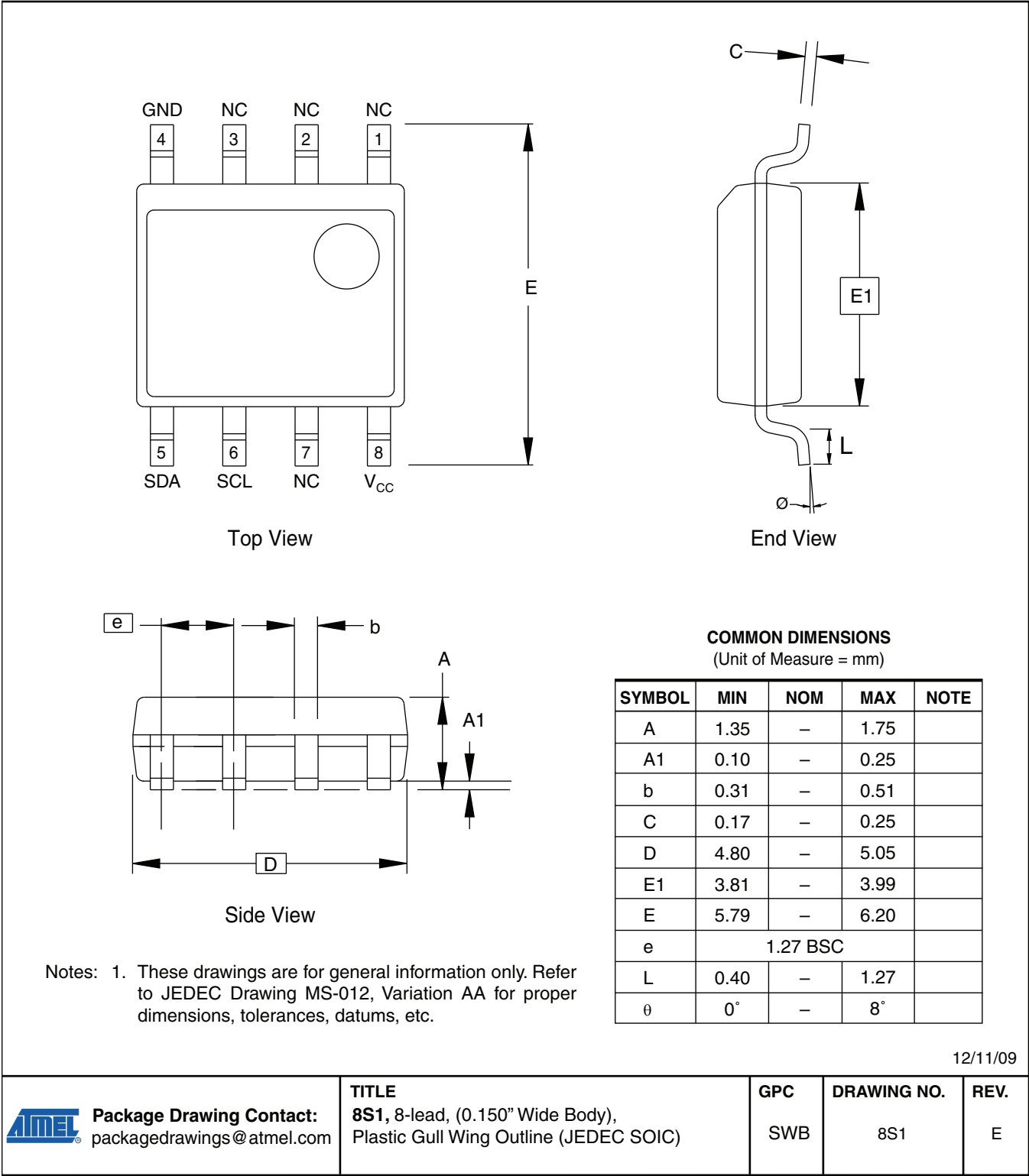
| Ordering Code | Package | Voltage Range | Operation Range |
|---|--------------|---------------|--|
| AT25256B-SSHL-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8S1 | Lead-free/Halogen-free/ Industrial Temperature (–40°C to 85°C) |
| AT25256B-SSHL-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8S1 | |
| AT25256B-XHL-B ⁽¹⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8A2 | |
| AT25256B-XHL-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8A2 | |
| AT25256B-MAHL-T ⁽²⁾ (NiPdAu Lead Finish) | 1.8V to 5.5V | 8MA2 | |
| AT25256B-CUL-T ⁽²⁾ (SnAgCu Ball Finish) | 1.8V to 5.5V | 8U2-1 | |
| AT25256B-WWU11L ⁽³⁾ | 1.8V to 5.5V | Die Sale | Industrial Temperature (–40°C to 85°C) |

- Notes:
1. Bulk delivery in tubes (SOIC and TSSOP 100/tube).
 2. Tape and reel delivery (SOIC 4k/reel. TSSOP, UDFN and VFBGA 5k/reel).
 3. Contact Atmel Sales for Wafer sales.

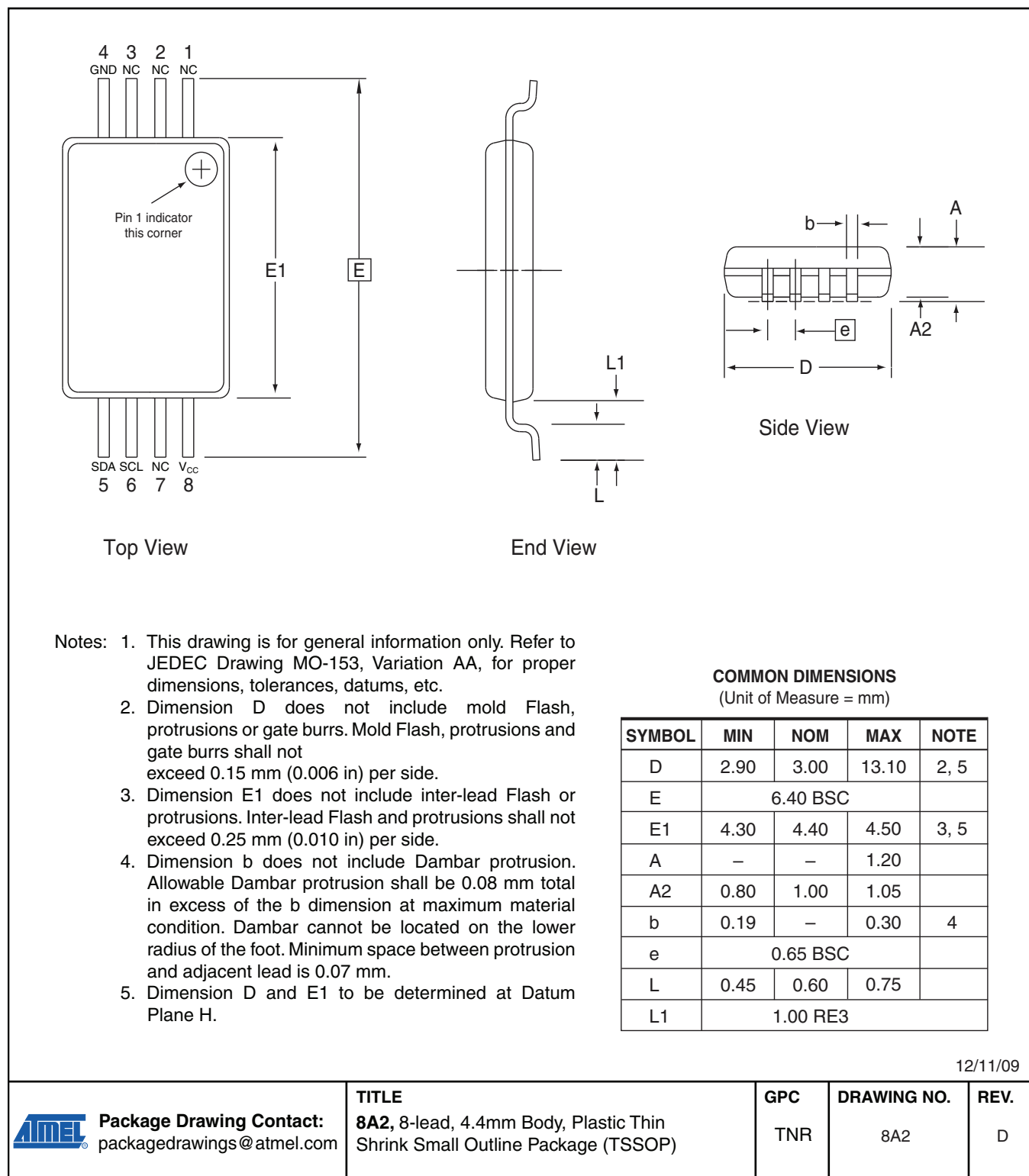
| Package Type | |
|--------------|---|
| 8S1 | 8-lead, 0.150" Wide, Plastic Gull Wing Small Outline Package (JEDEC SOIC) |
| 8A2 | 8-lead, 0.170" Wide, Thin Shrink Small Outline Package (TSSOP) |
| 8MA2 | 8-lead, 2.00mm x 3.00mm Body, 0.50 mm Pitch, Dual No Lead Package (UDFN) |
| 8U2-1 | 8-ball, die Ball Grid Array Package (VFBGA) |

8. Packaging Information

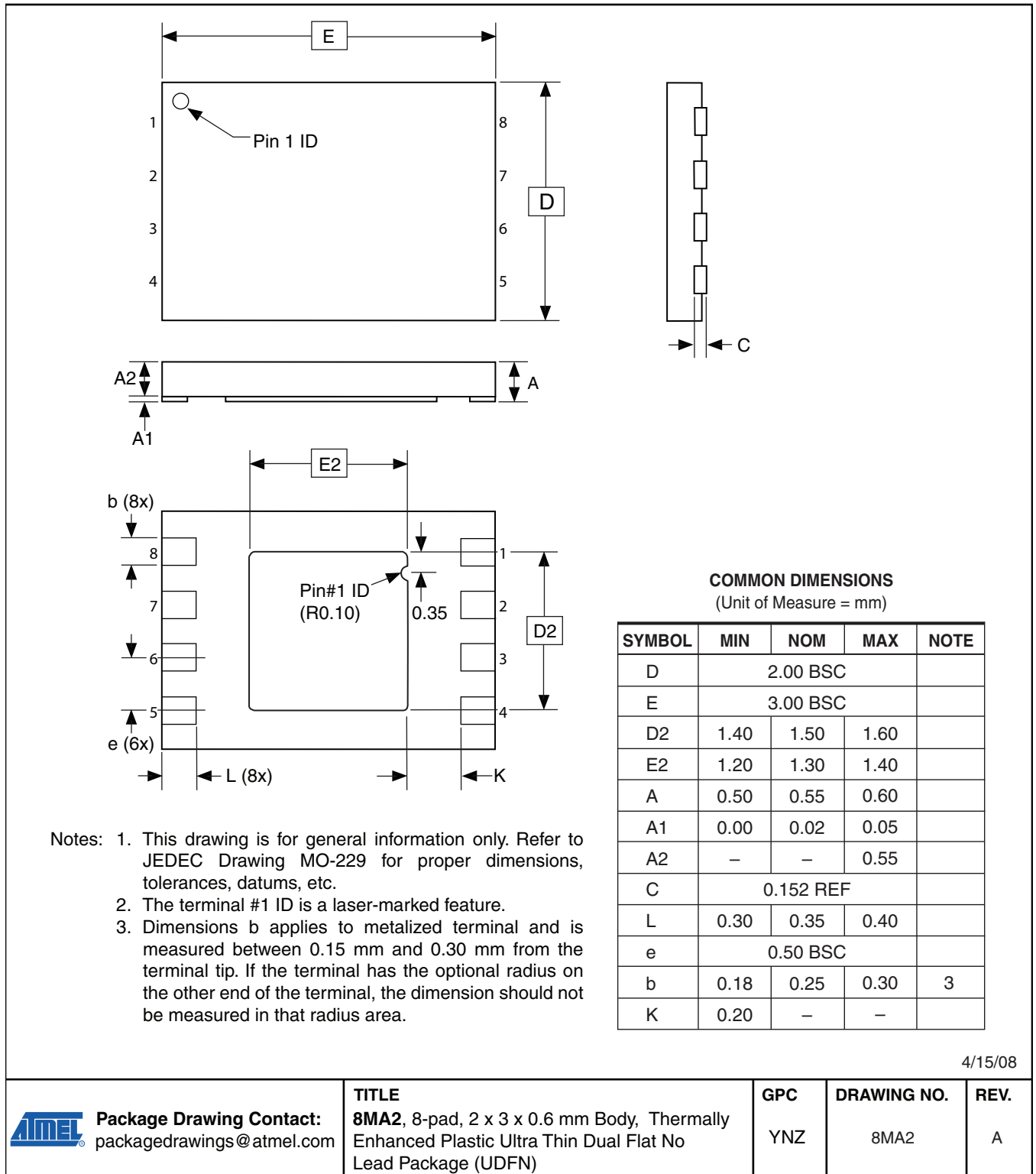
8S1 – JEDEC SOIC



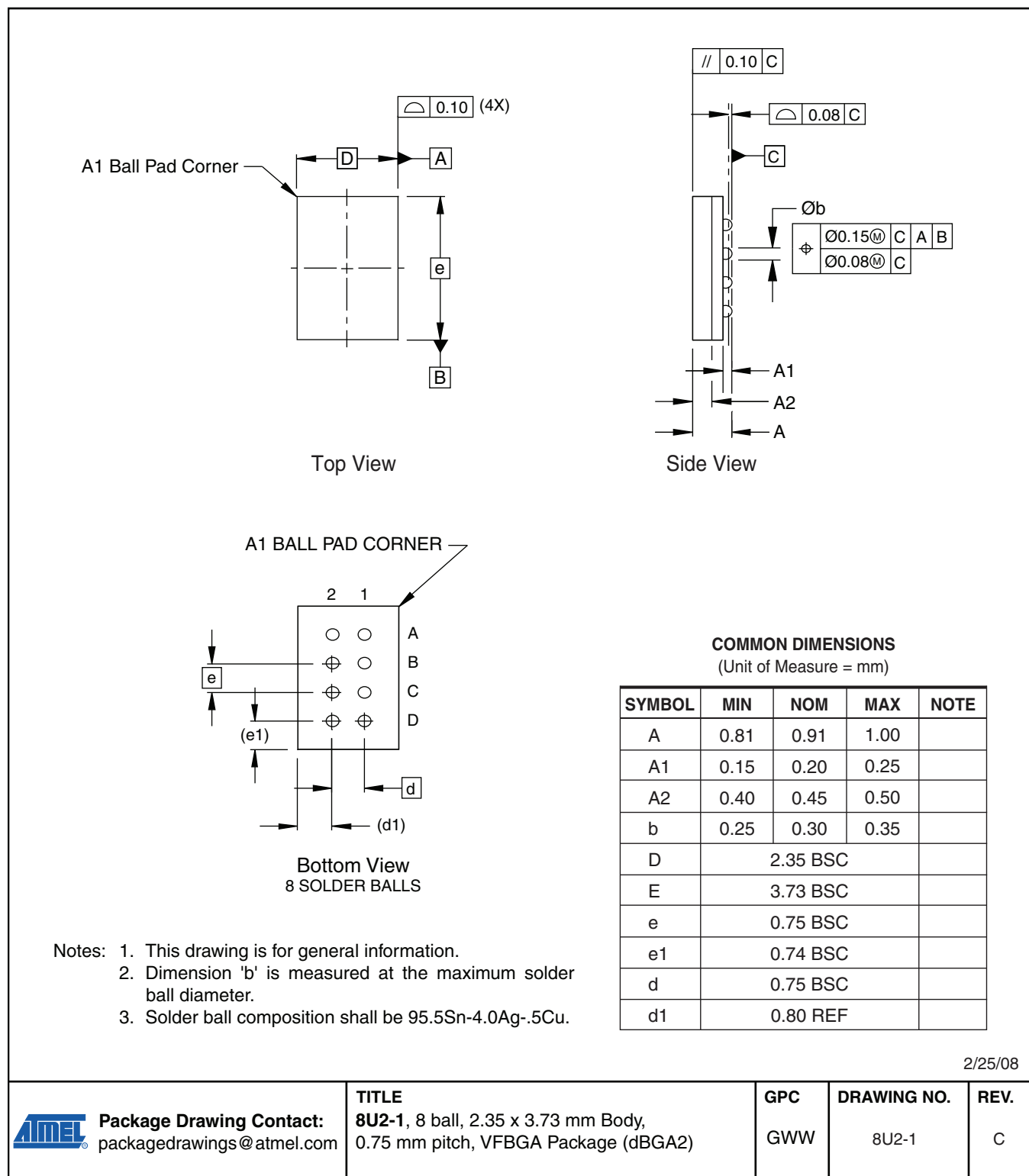
8A2 – TSSOP



8MA2 - UDFN



8U2-1 – VFBGA



9. Revision History

| Doc. Rev. | Date | Comments |
|-----------|---------|--|
| 8698B | 03/2010 | Update Catalog Numbering Scheme. Update Ordering Information and package types. |
| 8698A | 12/2009 | Initial document release. |



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