PCLT-2A

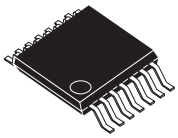
Dual current limited over-voltage protected digital termination

Applications

- Type 1, 2 and 3 logic input termination for industrial automation
- AS-Interface bus input termination
- I/O termination in programmable logic controller
- Proximity detector interface
- Decentralized Input / Output modules

Features

- 2 channel topology
  - Low side input with common ground
- Wide range input DC Voltage:
  - V_I = - 0.3 to 30 V with R_I = 0 Ω
  - V_I = - 30 to 35 V with R_I = 750 Ω
- Current limiter:
  - 3 to 7.5 mA programmable reference
  - I_{LIM} = 6.1 mA to 8.8 mA with R_{REF} = 10 kΩ
  - I_{LIM} = 2.8 mA to 4.3 mA with R_{REF} = 22 kΩ
  - Narrow limiter spread: < 17 %
  - Temperature compensated operation
- Output drive:
  - No output activation below 2 mA input current
  - 1.5 mA minimum output activating current in opto-coupler mode
  - Programmable CMOS output mode option (V_{MOD} > 2.9 V)
- LED drive for sensor status: 4.4 mA typical with R_{REF} = 10 kΩ
- Input protection (R_I = 750 Ω C_{IN} = 22 nF)
- IEC61000-4-2 electrostatic discharge ESD, Level 4
  - In contact, ± 8 kV; in air, ± 15 kV
  - Criteria B: temporary disruption



TSSOP14
Exposed pad

- IEC61000-4-5 voltage surge, Level 3
  - ± 500 V with 42 Ω series resistor in differential mode
  - Criteria B: temporary disruption
- IEC61000-4-4 transient burst immunity
  - ± 4 kV peak voltage; 5 kHz repetitive rate
  - Criteria A: fully functional
- IEC61000-4-6 conducted Radio Frequency Interference immunity
  - 10 V_{RMS} voltage
  - Criteria A: fully functional
- Input protection against -30 V reverse polarity
- Ambient temperature: -25 to 85 °C

Benefits

- Enable input to meet type1, 2 and 3 characteristics of IEC61131-2 standard
- Compatible operation with 2 & 3 wires proximity sensor according EN60947-5-2 standard
- Flexible configuration driving either opto coupler, or CMOS bus controller input, or 12 V AS-interface network
- Reduced overall dissipation
- Enhanced functional reliability
- Compact with high integration
- Surface Mount Package for highly automated assembly
- Insensitive to the on state sensor impedance

1 Characteristics

1.1 IEC61000-4 standard compliance application diagrams

Figure 1. Isolated digital input diagram with opto-coupler driving output

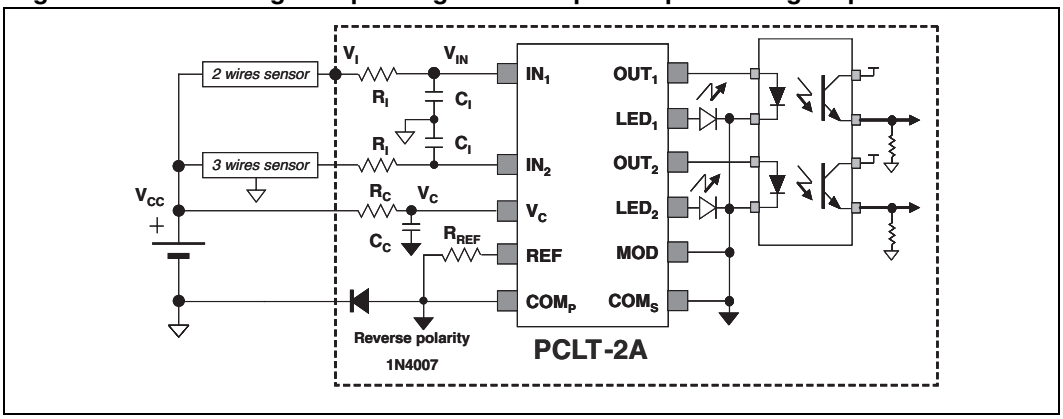
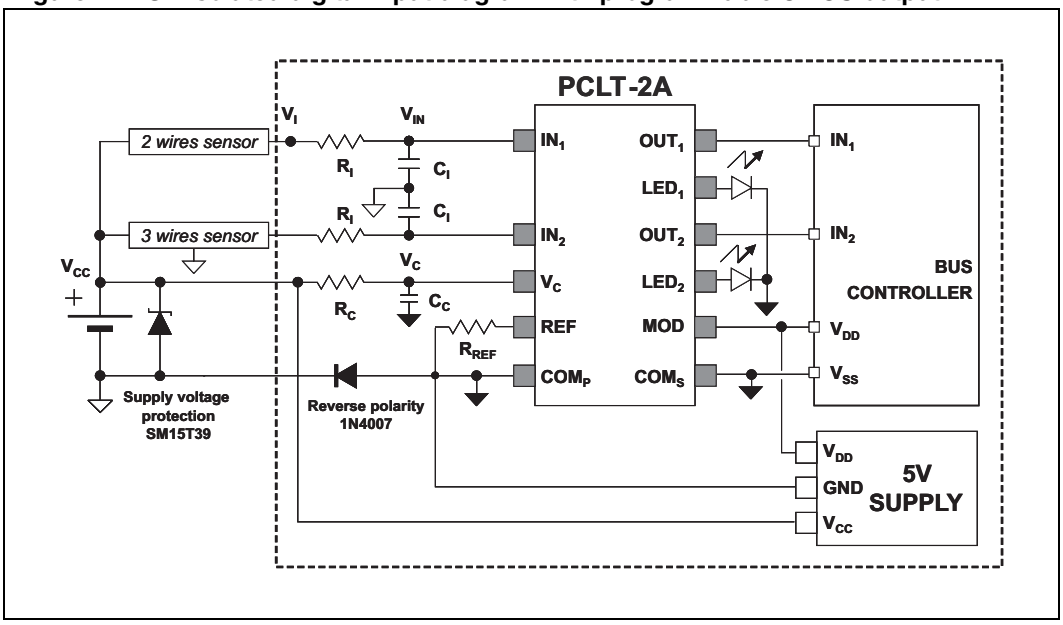
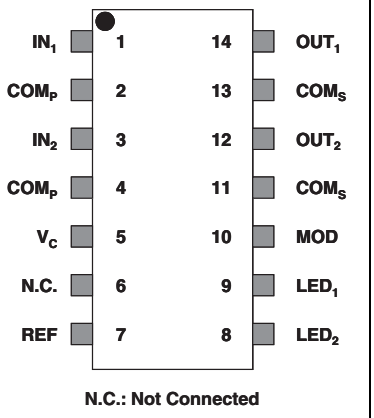


Figure 2. Un-isolated digital input diagram with programmable CMOS output



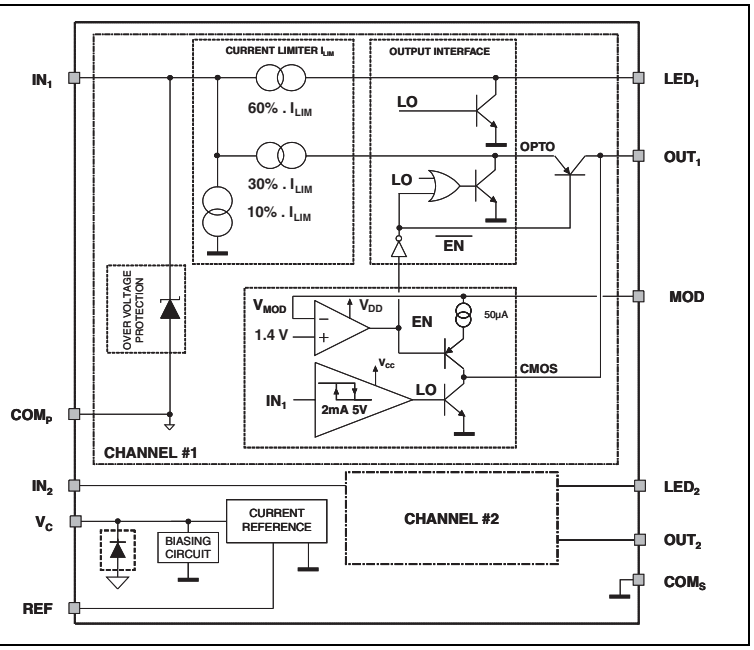
1.2 PCLT-2A Pinout and current limited termination block diagram

Figure 3. Pinout

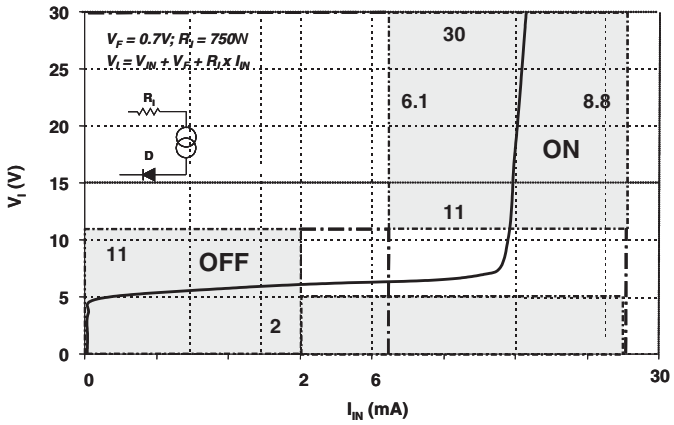


N.C.: Not Connected

Figure 4. Termination block diagram



1.3 Static characteristic of a type-2 digital input using PCLT-2A



1.4 Absolute ratings

Symbol	Pin	Parameter name & conditions	Value	Unit
V_{CC}	V_C	Power supply steady state voltage, R_C = 2.2 kΩ	- 0.3 to 35	V
V_C	V_C	Supply steady state voltage, R_C = 0 kΩ	- 0.3 to 30	V
V_{IN}	IN	Input steady state voltage, R_I = 0 kΩ	- 0.3 to 30	V
V_I (*Note: 1*)	IN	Input steady state voltage, R_I = 750 Ω	-30 to 32	V
		Input repetitive pulse voltage, R_I = 750 Ω	-30 to 35	V
I_{IN}	IN	Input maximum forward current R_I = 750 Ω R_C = 2.2 kΩ	10	mA
		Input maximum reverse current R_I = 750 Ω RC = 2.2 kΩ (Note *2*)	20	mA
V_{MOD}	MOD	Maximum applied CMOS supply voltage	14	V
V_{OM}	OUT, LED	Maximum applied output voltage, V_{MOD} < 0.75 V	2.5	V
		Maximum applied output voltage, V_{MOD} > 2.9 V	14	V
I_{OM}	OUT, LED	Output driver current	- 4 to 7	mA
T_J	ALL	Junction temperature range	- 25 to 150	°C

1.5 Recommended operating conditions

Symbol	Pin	Parameter name & conditions	Value	Unit
V_{CC}	V_C	Power supply steady state voltage, R_C = 2.2 kΩ	19 to 35	V
V_C	V_C	Power supply voltage range	14 to 27	V
V_I (Note *1*)	IN	Input repetitive pulse voltage R_I = 750 Ω R_C = 2.2 kΩ	- 30 to 30	V
V_{MOD}	MOD	Operating CMOS mode voltage range	2.9 to 5.5	V
		Maximum operating 12V Analog voltage	13.5	V
T_{AMB}	ALL	Operating Ambient temperature range	- 25 to 85	°C
T_J		Operating Junction temperature range	- 25 to 150	°C

Note: 1 $V_I = V_{IN} + V_F + R_I$ x I_{IN} with V_{IN} = voltage at the PCLT-2A input pin; $V_{CC} = V_C + R_C$ x I_{CC} with V_C = voltage at the PCLT-2A power supply pin.

2 Respect to the reverse polarity test of one input as shown on Figure 12.

1.6 Electromagnetic compatibility ratings

T_J=25 °C, R_I = 750 Ω R_C = 2.2 kΩ , & reverse diode connected (unless otherwise specified)

Symbol	Node	Parameter name & conditions	Value	Unit
V_{ESD}	IN V_{CC}	ESD protection, IEC 61000-4-2, per input, in air	± 15	kV
		ESD protection, IEC 61000-4-2, per input, in contact	± 8	kV
		ESD protection, IEC 61000-4-2, per input, in air, R_I = 0 Ω	± 3	kV
		ESD protection, IEC 61000-4-2, per input, in contact, R_I = 0 Ω	± 3	kV
V_{PPB}	V_I	Total Peak Pulse Voltage Burst, IEC61000-4-4 C_C = 33 nF, C_I = 22 nF, F = 5 kHz (Note *1*)	± 4	kV
V_{PP}	V_I	Peak Pulse Voltage Surge, IEC61000-4-5, R = 42 Ω (Note *2*)	± 500	V
V_{PP}	V_I	Peak Pulse Voltage Surge, IEC61000-4-5, R = 42 Ω R_I = 1200 Ω (Note *2*)	± 1000	V
V_{PP}	V_{CC}	Peak Pulse Voltage Surge, IEC61000-4-5, R = 2 Ω (Note *2*)	± 1000	V

Note: 1 Test diagram described on Figure 1 using the application PCB with a normalized capacitive coupling clamp

2 Test diagram described on Figure 1

1.7 Thermal resistance

Symbol	Parameter name & conditions	Value	Unit
$R_{TH\ JA}$	Thermal resistance Junction to ambient Board copper surface = 1.25 cm², copper thickness = 35 µm, single face	100	°C/W

1.8 DC electrical characteristics

(T_J = 25 °C, V_{CC} = 24 V, R_{REF} = 10 kΩ R_C = 2.2 kΩ and referred to COM pin voltage, unless otherwise specified)

Symbol	Pin	Name	Conditions	Min	Typ	Max	Unit
Current limitation							
I_{LIM}	IN	Input limiting current	V_{IN} = 4.5 to 26 V V_{OUT} = 0.9 to 1.5 V V_{LED} = 1.5 to 2.5 V T_{AMB} =-25 to 85 °C R_{REF} = 10 kΩ	6.1	7.6	8.8	mA
I_{LIM}	IN	Input limiting current	V_{IN} = 5.5 to 26 V V_{OUT} = 0.9 to 1.5 V V_{LED} = 1.5 to 2.5 V T_{AMB} =-25 to 85 °C R_{REF} = 22 kΩ	2.8	3.6	4.3	mA
V_{LOW}	IN	Low current input voltage	I_{IN} = 100 µA		1.5	3	V
		Current limiter activation voltage	I_{IN}=6 mA	-	2.6	-	V
			I_{IN}=2 mA, R_{REF}=22 kΩ	-	2.3	-	V
Input & Supply Protection							
V_{CL}	IN, V_C	Clamping voltage	I_{IN} = 7 mA, t_P = 1 ms, R_{REF} open	31	38	-	V
Output interface operation							
I_{OFF}	OUT LED	Off state output current	V_{MOD} = 0 V, V_I = 5 V, (Note *1*)	-	10	40	µA
			V_{MOD} = 0 V, I_{IN}=2 mA, (Note *2*)	-	10	40	µA
V_{OFF}	LED	Off state LED voltage	I_{IN} = 2 mA		0.1	0.2	V
V_{OFF}	OUT	Off state output voltage	V_{MOD} = 0 V, I_{IN} = 2 mA		0.02	0.1	V
			V_{MOD} > 2.9 V, I_{IN} = 2 mA			20 % V_{MOD}	V
I_{ON}	OUT	On state opto-coupler current	V_{MOD} = 0 V, V_{OUT} = 1.5 V V_{IN} =4.5 V	1.5	2		mA
			V_{MOD} = 0 V, V_{IN} = 5.5 V, R_{REF} = 22 kΩ , V_{OUT} = 1.5 V	0.5	0.9		mA
V_{ON}	OUT	On state output voltage	V_{MOD} > 2.9 V R_{REF} = 10 kΩ , V_{IN} > 4.5 V R_{REF} = 22 kΩ V_{IN} > 5.5 V	80%. V_{MOD}			
I_{ON}	LED	On state LED current	V_{IN} = 4.5 V, V_{LED} = 2.5 V (Note *3*)	3.5	4.4		mA
			V_{IN} = 5.5 V, R_{REF} = 22 kΩ V_{LED} = 2.5 V	1.4	2.1		mA

Symbol	Pin	Name	Conditions	Min	Typ	Max	Unit
Output operation selection circuit							
$V_{TH\ MOD}$	MOD	Opto-CMOS threshold		0.75		2.9	V
I_{OUT}	OUT	CMOS output current	V_{MOD} = 12V	35	50	65	µA
Power supply circuit							
I_C	V_C	Supply current	V_{CC} = 30V		1.5	2	mA
I_{DD}	MOD	CMOS supply current	V_{MOD} = 5V, V_{IN} open		0.25	0.35	mA
			V_{MOD} = 12V, V_{IN} open		0.4	0.8	mA

Note: 1 According to application diagram (Figure 1) with the use of a R_I = 750 Ω resistor a reverse diode from COM to GND (V_F = 0.7 V) and an opto-coupler (R_{LED} (0V) = 15 kΩ , V_F=1.2 V).

2 Same as note 1 above, but R_I= 0 .

3 When no LED diode is used, connect LED pin to the COM_P ground.

1.9 Switching electrical characteristics

(T_J=25°C, V_{CC} = 24 V, R_C = 2.2kΩ, C_I = 0 and COM pin voltage referred unless otherwise specified)

Symbol	Pin	Name	Conditions	Min	Typ	Max	Unit
F_{MAX}	IN-OUT	Input to output operating frequency	Duty cycle = 50%		5		kHz
T_{PLH}	IN-OUT	Input Lo to Hi propagation time	C_I = 0		16		µs
T_{PHL}	IN-OUT	Input Hi to Lo propagation time	C_I = 0, V_{MOD} = 0 V		0.1		µs
			C_I = 0, V_{MOD} = 5 V C_{OUT} = 50 pF		7.6		

1.10 Functional characteristics

Figure 5. Variation of the input-output propagation delay time T_{PLH} at rising edge versus the supply voltage V_{CC} with R_C = 2.2 kΩ

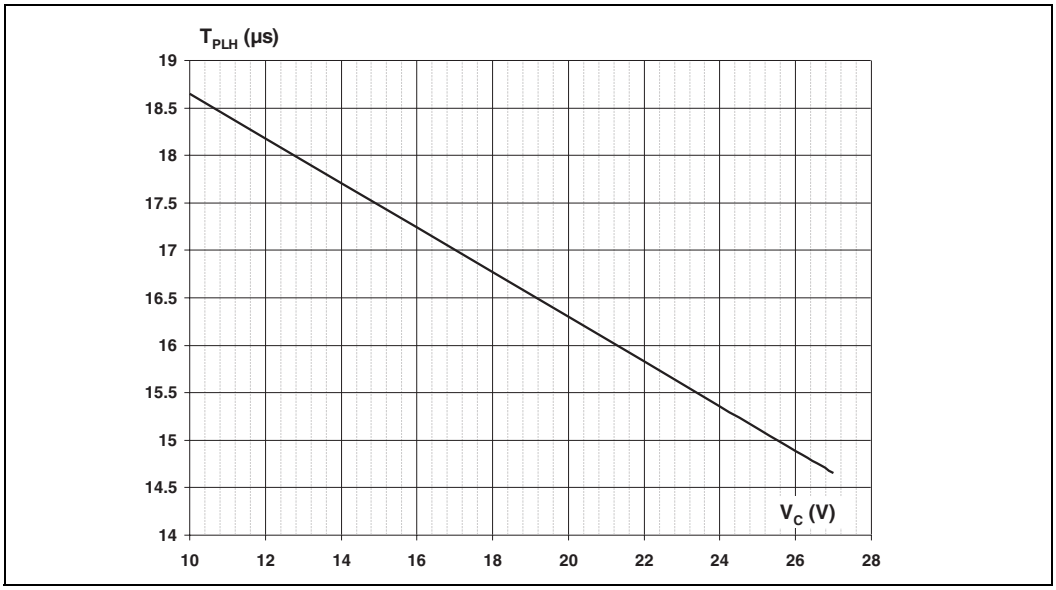


Figure 6. Typical current limiter variation versus junction temperature

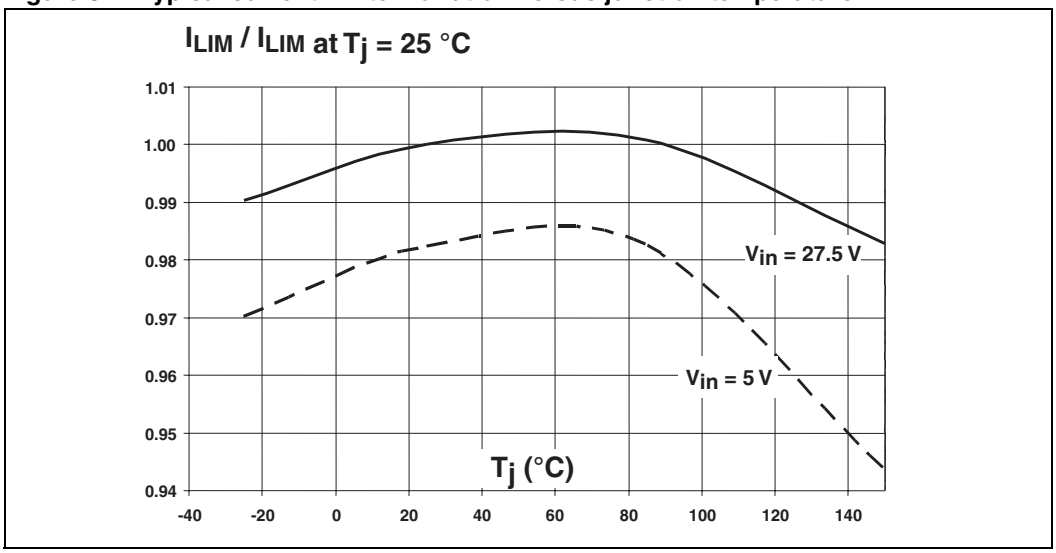


Figure 7. Typical current limiter variation versus reference resistance R_{REF}

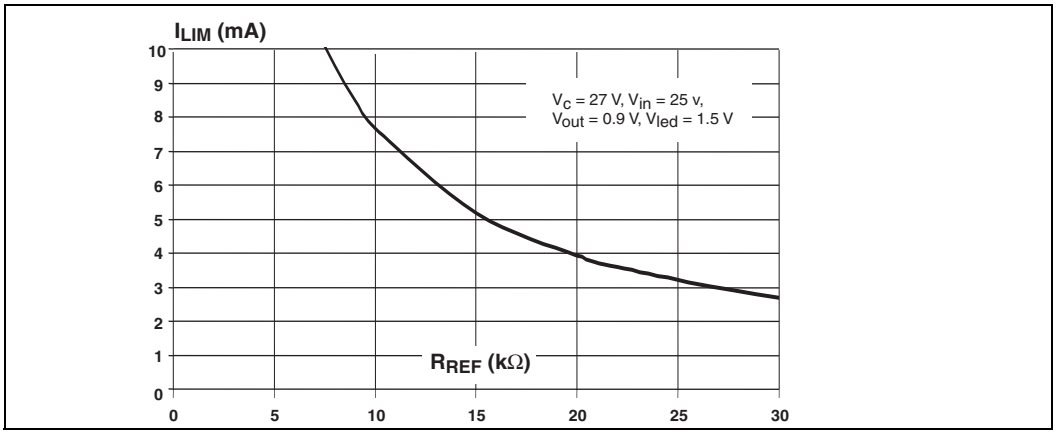


Figure 8. Typical limiter activation voltage variation versus junction temperature

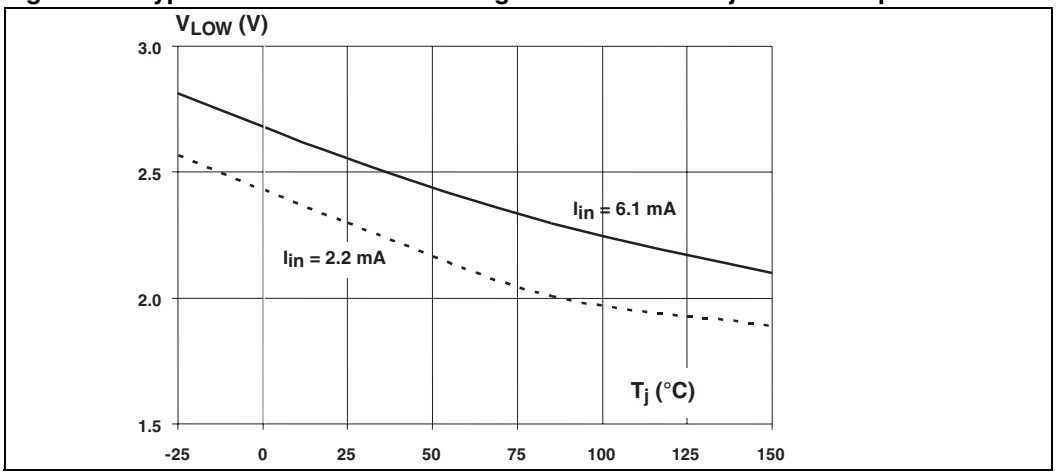
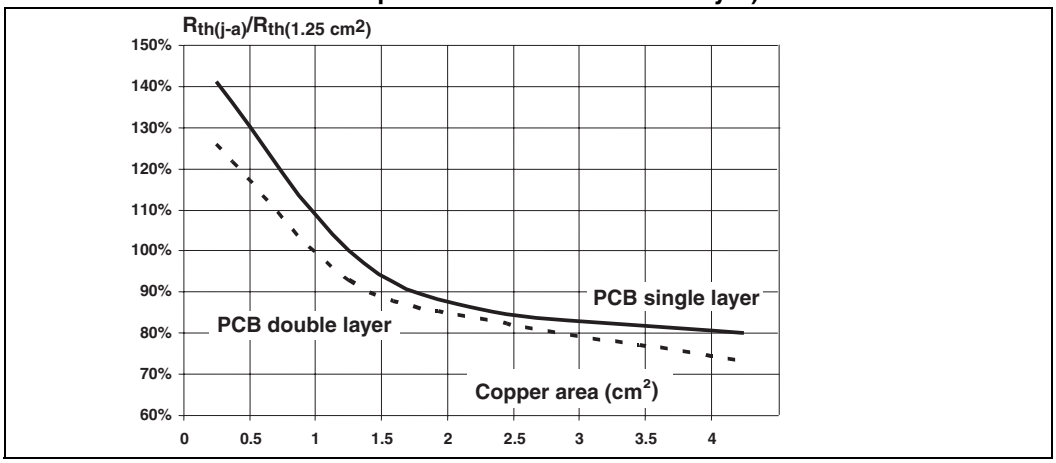


Figure 9. Thermal resistance variation versus copper area (35 µm layer thickness; 50vias/cm^2 and 300 µm via diameter in double layer)



2 Functional description

The PCLT-2A is a dual input termination device designed for 24 V DC automation applications. It achieves the front-end circuitry of a digital input module (I/O) in industrial automation.

Available in a two channels configuration, it offers a high-density termination by minimizing the conducting dissipation and the external components count. It is housed in a surface mount package to reduce the printed board size.

Made of an input voltage protection, a serial current limiting circuit and an output interface, each channel circuit terminates the connection between the logic input and its associated high side sensor or switch.

The PCLT-2A is a current limited dual channel circuit compatible with the type 2 (7.5 mA) or type 3 (3 mA) characteristic of the IEC61131-2 standard. An external resistance R_{REF} allows the limiting current value to be adjusted from 3 to 7.5 mA.

The unique structure of the PCLT limiter allows its activation threshold to be low and insensitive to the output voltage up to 2.5 V.

Each input voltage clamping block protects the module input against electromagnetic interferences such as those described in the IEC61131-2 standard and IEC61000-4-2 (ESD), 4-4 (transient burst), 4-5 (voltage surge) and 4-6 (conducted radio frequency interferences) standards. The supply input is also designed with such a protection structure.

The current limiting circuit connected between the input and the output pins is compensated all over the temperature range. Thanks to its low tolerance, the current limitation allows reducing drastically the dissipation of the input compared to a resistive input. Furthermore, the PCLT2 is housed into a very low R_{TH} exposed pad TSSOP14 package that allows the PCB cooling pad to be reduced: the overall module becomes smaller and the hot spot effect is reduced.

The output block of each termination channel transfers the input logic state to a logic output and a Light Emitting Diode (LED) that allows this state to be checked visually.

2.1 The V_{MOD} pin

The voltage V_{MOD} applied to the selector pin MOD allows the output OUT to be configured either in an opto-coupler driver for V_{MOD} less than 0.75 V or in a CMOS output able to interface directly a bus controller circuit for V_{MOD} higher than 2.9 V.

In CMOS mode, the V_{MOD} pin activates a CMOS compatible buffer output, able to source up to a 50 µA current powered by the MOD pin.

2.2 OFF state

In accordance with IEC61131-2 standard, for both opto-coupler and CMOS configuration modes when the input current is less than 2 mA (type 2) or 1.5 mA (type 3) the output circuits divert all the input current and maintain both LED and output in OFF state.

2.3 ON state

When the module input voltage V_I, including the 750 Ω input resistor and the reverse diode, is higher than 11V corresponding to a PCLT input voltage V_{IN} of 5V, both LED and output circuits are in ON state. The input current is then shared between the internal circuitry, the LED (about 60 %), and the driver output (about 30 %) in case of opto-coupler mode.

In CMOS mode, the CMOS level is defined by the V_{MOD} voltage that is equal the supply voltage V_{DD} of the bus controller: it can be 3.3 V or 5 V. The output voltage is delivering 80 % of V_{DD} for high state and 20 % V_{DD} for low state.

When no LED diode is used, the LED outputs pin must be connected to the ground COM_P of the circuit to allow the current to flow back to the power supply.

3 Surge voltage test circuit

The input and supply pins are designed to withstand electromagnetic interferences. They are protected by a clamping diode that is connected to the common pin COM. Combined with the serial input resistance RI, this clamping diode is effective against the fast transient bursts (±4 kV, IEC61000-4-4) and the voltage surges (±1 kV,IEC61000-4-5).

This topology allows the surge voltage to be applied from each input to other inputs, the ground and the supply contacts in differential or common modes (see figure 10).

Thanks to its high resistance R_C = 2.2 kΩ and the conventional power supply protection that uses a clamping diode such as the SM15T39C Transil™, the supply pin V_C withstands ±1000 V surge voltage according to IEC61000-4-5 (see figure 11).

Figure 10. Input pin IN voltage surge test circuit

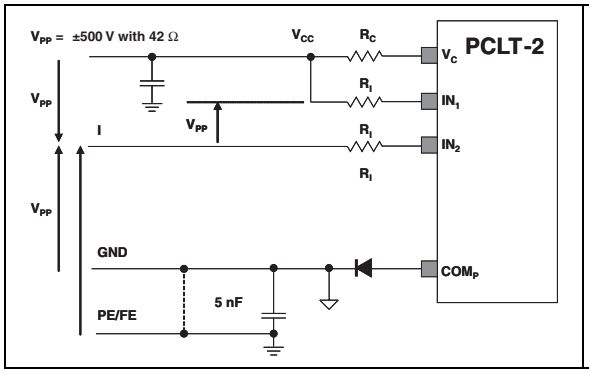
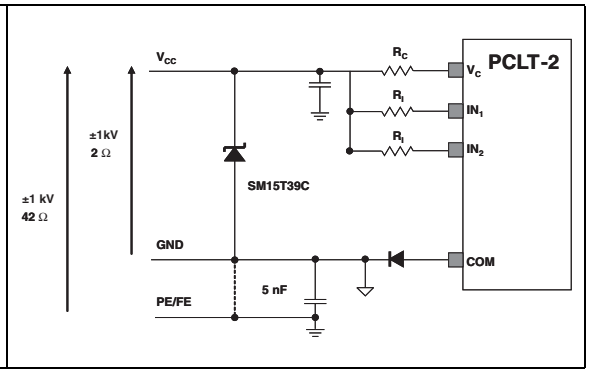


Figure 11. Supply pin V_C voltage surge test circuit



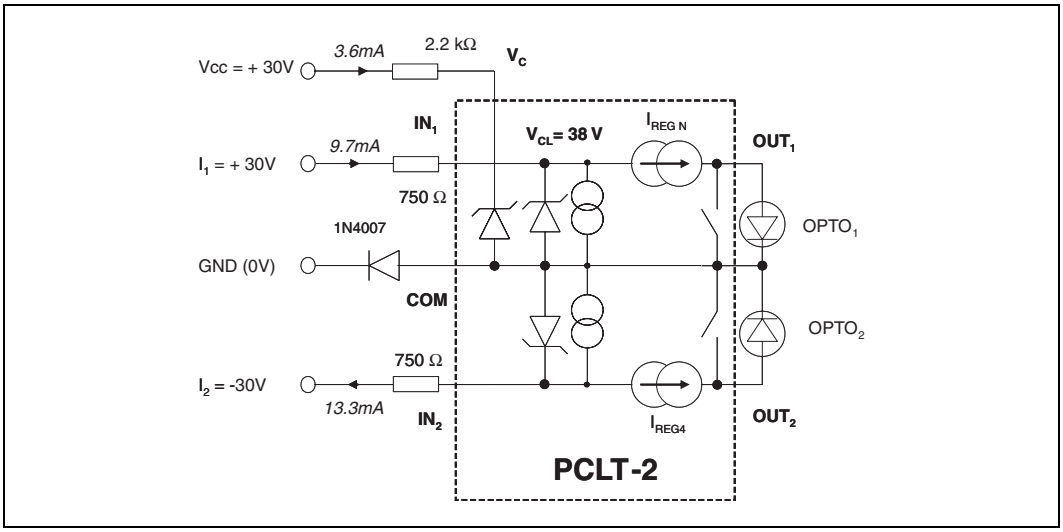
TM: Transil is a trademark of STMicroelectronics

4 Input reverse polarity robustness

Each input of the PCLT circuit may be biased to a reverse polarity equal to - V_{CC}. This case corresponds to a connection mistake or a reverse biasing that is generated by the demagnetization of a monitored inductive solenoid.

The involved input withstands the high reverse current up to 20 mA; its opto-coupler is OFF and is protected by the conducting input diode. The input remains operational, and some extra dissipation should be take place in their clamping protections.

Figure 12. Current sharing in the PCLT device when IN_2 is biased at -30 V and IN_1 at +30 V.



Considering the supply operation, a reverse blocking diode can be connected between the module ground and the common pin COM to protect the PCLT device against any spurious reverse supply connection. Then, the whole module supply voltage rating is extended to ± 30 V.

5 Programming of the PCLT-2A according to the input type requirement

The operation of the PCLT-2 can be set to the various logic input types defined in the IEC61131-2 standard. The current reference of the input-limiting block of each channel is programmable thanks to an external resistor R_{REF}. Moreover, because the operating current is different for each type, the external input resistor R_I can be changed to improve the over-voltage robustness of the whole circuit. *Table 1* describes the input characteristics requirements according to the IEC standard, and *Table 2* the resistance values for the 1, 2, and 3 types and the corresponding performances of the PCLT input.

Table 1. IEC61131-2 requirements for logic input

		Type	1	3	2
State	**Parameter**	**Unit**			
OFF	$I_{OFF\ MAX}$	mA	0.5	1.5	2
	$V_{OFF\ MAX}$	V	5 15 @ I_{OFF}	5 11 @ I_{OFF}	5 11 @ I_{OFF}
ON	$I_{ON\ MIN}$	mA	2	2	6
	$V_{ON\ MIN}$	V	15	11	11

Table 2. PCLT-2A setting for each type of logic input

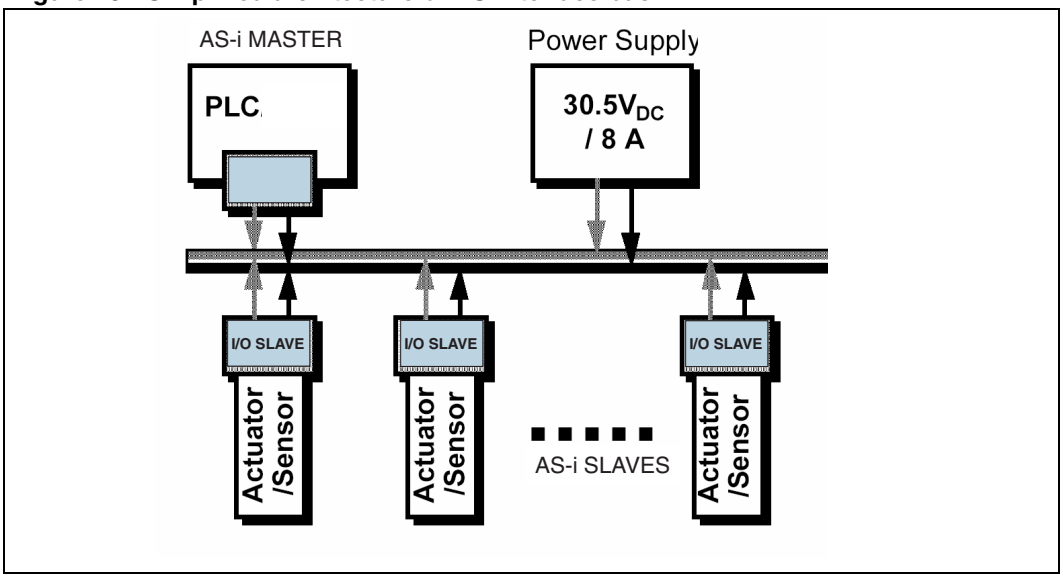
Type		1	3	2
Setting	**Unit**			
R_{REF}	kΩ	22	22	10
R_I	kΩ	2.2	1.2	0.75
R_C	kΩ		2.2	
PERFORMANCES				
$I_{IN\ MIN}$	mA	2.8	2.8	6.1
$I_{IN\ TYP}$	mA	3.6	3.6	7.6
$I_{IN\ MAX}$	mA	4.3	4.3	8.8
$I_{LED\ TYP}$	mA	2.1	2.1	4.4
SURGE w/R_I	kV	> 1	1	0.5
ESD with R_I	kV	8 in contact, 15 in air (class 4)		

6 Unisolated ASI-interface bus application diagram

6.1 AS-Interface Bus application overview

The AS-Interface bus is a low-end field bus for actuators and sensors in manufacturing & industrial automation. Its electrical architecture uses an unshielded 2-wire yellow cable that transports both the 24 V power supply of the field nodes and the serial bi-directional data communication.

Figure 13. Simplified architecture of AS-Interface bus.



The data communication is achieved with a current carrier modulation superimposed over the power wires. Therefore, the power bus terminals are filtered in order to maintain identical and calibrated differential and common mode impedances measured by both master and slave units.

6.2 Isolation of the sensor section and the supply from data/supply bus

The PCLT can be designed as an interface between a proximity sensor and its associated slave controller unit.

The sensor power supply is generated from the bus power supply with a filter and a regulator that are inserted in the slave unit. In the same manner, the sensor logic signal is isolated from the AS- Interface power supply bus to avoid any degradation of the data transmission.

A conventional way to achieve the interface with the PCLT and the AS- Interface controller is to insert an opto-coupler between the AS-Interface controller and the PCLT that runs in opto-coupler mode as shown on figure 1 (MOD=0).

6.3 Un-isolated connection of the PCLT with AS-Interface controller

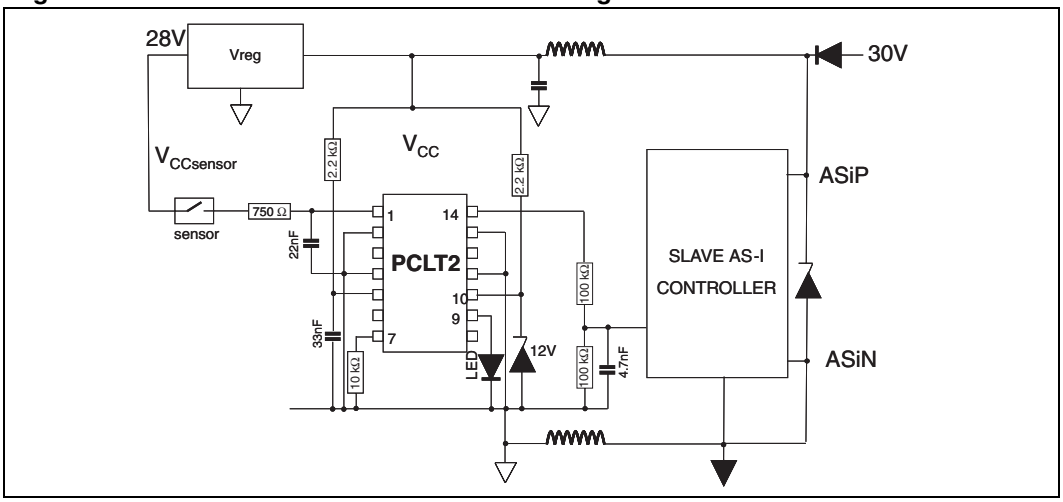
To remove the opto-coupler the operation of the PCLT has been extended to fit the AS-Interface application. A precaution is required on its interface with the bus controller: the impedance between the two circuits must be high in order to maintain the impedance isolation.

To achieve this impedance isolation, the PCLT runs in CMOS mode (MOD=V_{CC}) and the buffer operation is extended up to V_{CC} = 12 V. In the application, the V_{CC} voltage is generated with a Zener diode reference fed from the sensor bus.

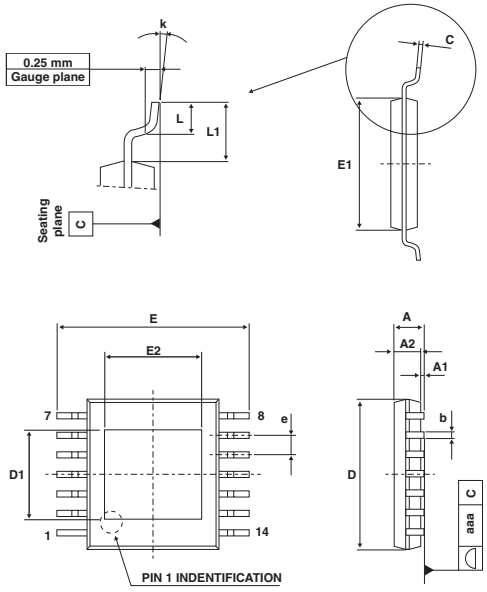
Because of the buffer voltage increase, it becomes possible to insert high impedance between the PCLT output and the AS-Interface bus controller input. Typically a 100kΩ resistor is designed while keeping a 5 V CMOS operation on the input of the bus controller.

Figure 14 shows the application diagram where the PCLT is connected to the slave bus controller through a 100 kΩ resistor. The logic signal is transmitted with a low level of less than 20% of the V_{DD} supply voltage and a high level of at least 3.5 V defined by the PCLT output buffer limiting its current to 35 µA minimum and the 100 kΩ pull down resistor (0.035 mA times 100 kΩ).

Figure 14. AS-Interface slave controller unit using the PCLT in an un-isolated manner.

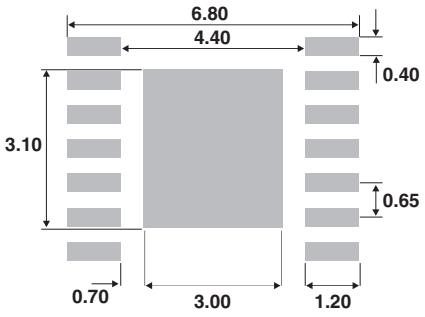


7 Package mechanical data



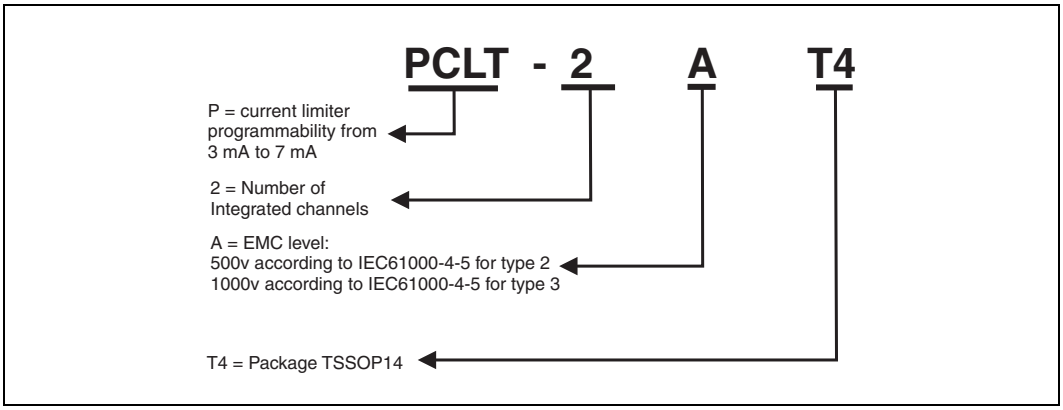
REF.	DIMENSIONS					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2	0.8	1.0	1.05	0.031	0.039	0.041
b	0.19		0.3	0.007		0.012
c	0.09		0.2	0.003		0.008
D	4.9	5.0	5.1	0.193	0.197	0.200
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.5	0.169	0.173	0.177
e		0.65			0.025	
L	0.45	0.6	0.75	0.018	0.024	0.029
L1		1.0			0.039	
k	0°		8°	0°		8°
aaa			0.1			0.004
D1		3.6			0.142	
E2		3.0			0.118	

Figure 15. Footprint



dimensions in mm

8 Ordering information scheme



9 Ordering information

Ordering Code	Marking	Package	Weight	Base Qty	Delivery Mode
PCLT-2AT4	PCLT-2AT4	TSSOP14(1)	0.057g	96	Tube
PCLT-2AT4-TR	PCLT-2AT4	TSSOP14(1)	0.057g	2500	Tape & reel

1. Exposed pad version

10 Revision history

Date	Revision	Changes
16-Nov-2005	1	Initial release.