USBULC6-2M6

Ultra large bandwidth ESD protection

Features

- 2 data line 15 kV ESD protection
- Protects 5 V V_{BUS} when applicable
- Ultra low capacitance: 0.65 pF at F = 240 MHz
- Very low leakage current: 0.5 µA max.
- Fast response time compared with varistors
- µQFN 6 lead package
- RoHS compliant

Benefits

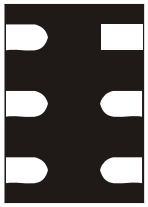
- ESD protection of V_{BUS} (when applicable)
- High bandwidth to minimize impact on data signal quality
- Low PCB space occupation
- Low leakage current profides longer operation of battery powered devices
- Higher reliability offered by monolithic integration

Complies with these standards:

- IEC 61000-4-2 level 4
  - 15 kV air discharge
  - 8 kV contact discharge

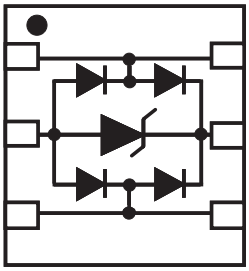
Applications

- USB 2.0 ports including Hi-Speed USB ports up to 480 Mb/s as well as full and low speed USB ports
- Ethernet port: 10/100/1000 Mb/s
- Video line protection
- Portable electronics



µQFN
(pin view)

Figure 1. Functional diagram (top view)



Description

The **USBULC6-2M6** is a monolithic, application specific discrete device dedicated to ESD protection of high speed interfaces.

Its ultra low line capacitance provides high bandwidth and secures a high level of signal integrity without compromizing the protection of downstream sensitive chips against the most stringent characterized ESD strikes.

1 Characteristics

Table 1. Absolute ratings

Symbol	Parameter		Value	Unit
V_{PP}	Peak pulse voltage	IEC 61000-4-2 air discharge IEC 61000-4-2 contact discharge MIL STD883G-Method 3015-7	±15 ±15 ±25	kV
T_{stg}	Storage temperature range		-55 to +150	°C
T_j	Maximum junction temperature		150	°C
T_L	Lead solder temperature (10 seconds duration)		260	°C

Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max	
I_{RM}	Leakage current	V_{RM} = 5 V			0.5	µA
V_{BR}	Breakdown voltage between V_{BUS} and GND	I_R = 1 mA	6			V
V_{CL}	Clamping voltage	I_{PP} = 1 A, t_p = 8/20 µs Any I/O pin to GND			12	V
		I_{PP} = 5 A, t_p = 8/20 µs Any I/O pin to GND			17	V
$C_{i/o-GND}$	Capacitance between I/O and GND	V_R = 0 V, F = 1 MHz Any I/O pin to ground		0.95	1.1	pF
		V_R = 0 V, F = 240 MHz Any I/O pin to ground		0.65	0.85	
$\Delta C_{i/o-GND}$	Capacitance variation between I/O and GND	V_R = 0 V, F = 1 MHz Any I/O pin to ground		0.020		
$C_{i/o-i/o}$	Capacitance between I/O	V_R = 0 V, F = 1 MHz Ground not connected		0.5	0.55	
		V_R = 0 V, F = 240 MHz Ground not connected		0.35	0.4	

Figure 2. Line capacitance versus frequency (typical values)

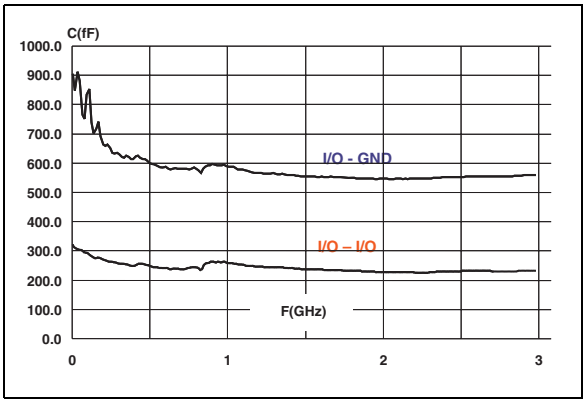


Figure 3. Relative variation of leakage current versus junction temperature (typical values)

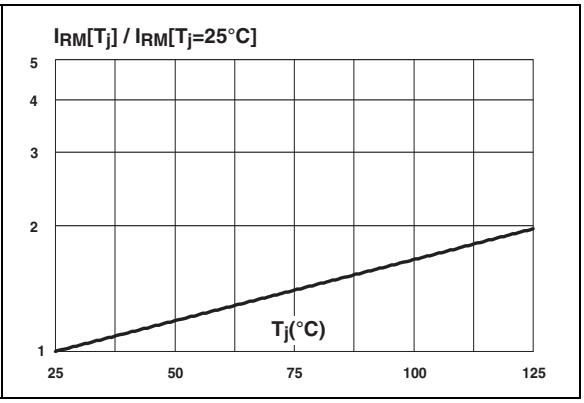


Figure 4. Attenuation measurement

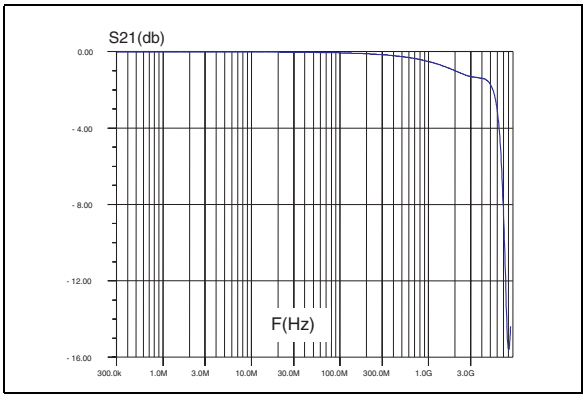


Figure 5. Crosstalk measurements

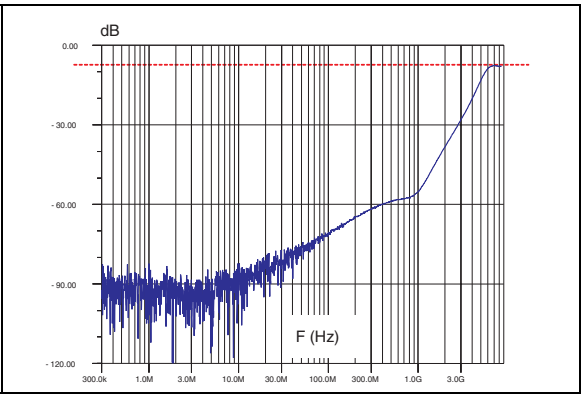


Figure 6. Remaing voltage on I/O1 after the USBULC6-2M6 during positive ESD surge (15 kV Air)

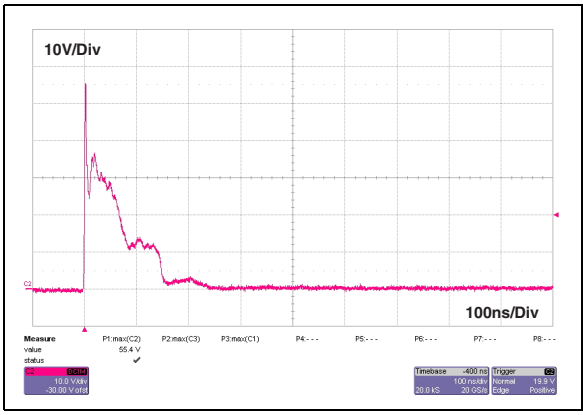


Figure 7. Remaing voltage on I/O2 after the USBULC6-2M6 during negative ESD surge (15 kV Air)

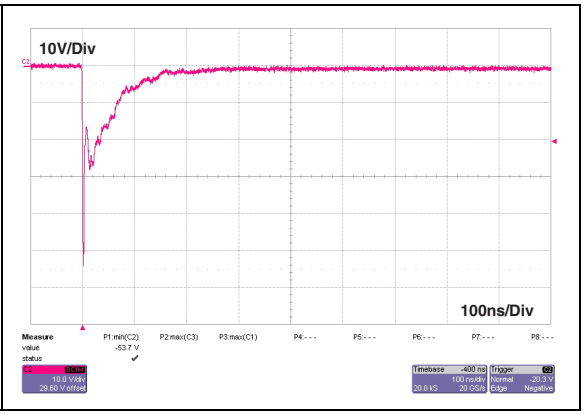


Figure 8. Remaing voltage on V_{BUS} after the USBULC6-2M6 during positive ESD surge (15 kV Air)

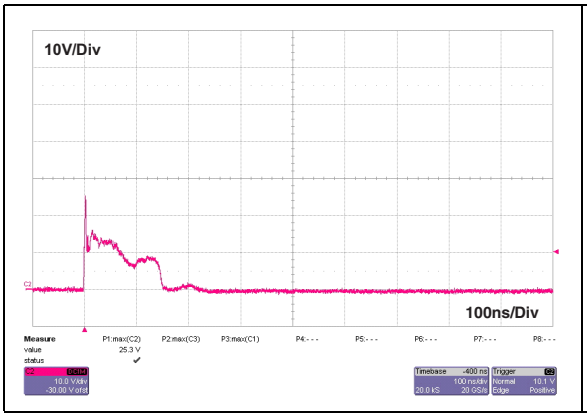


Figure 9. Remaing voltage on V_{BUS} after the USBULC6-2M6 during negative ESD surge (15 kV Air)

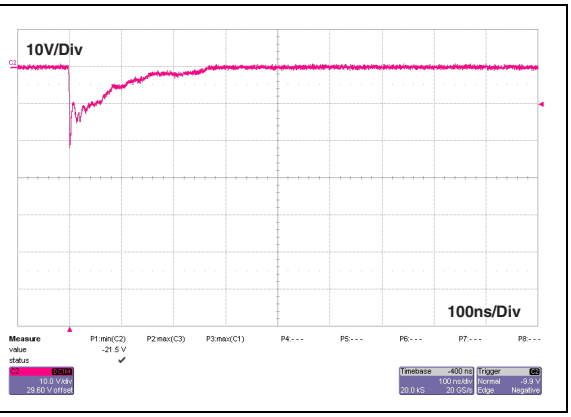


Figure 10. Eye diagram PCB only 400 mV amplitude, F = 480 Mbps

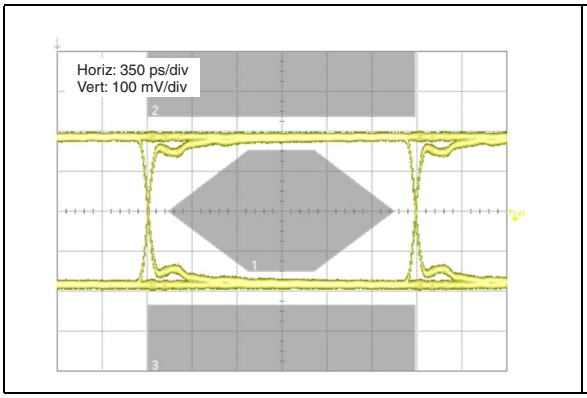


Figure 11. Eye diagram PCB + USBULC6-2M6 400 mV amplitude, F = 480 Mbps

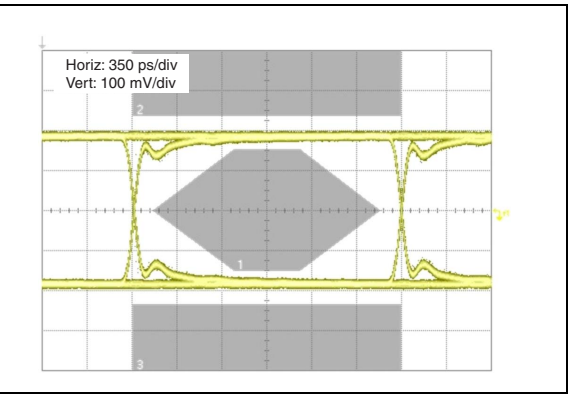
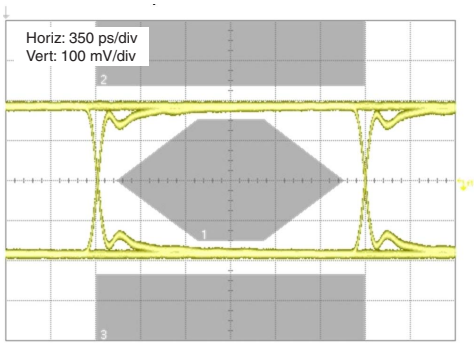
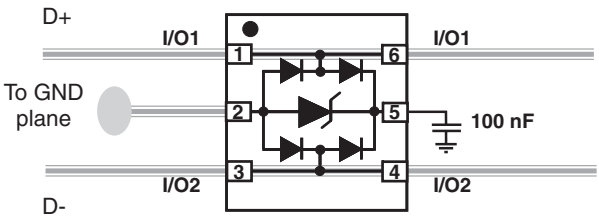


Figure 12. Eye diagram PCB + USBULC6-2M6, +5 V on V_{BUS} decoupling capacitor 100 nF, 400 mV amplitude, F = 480 Mbps



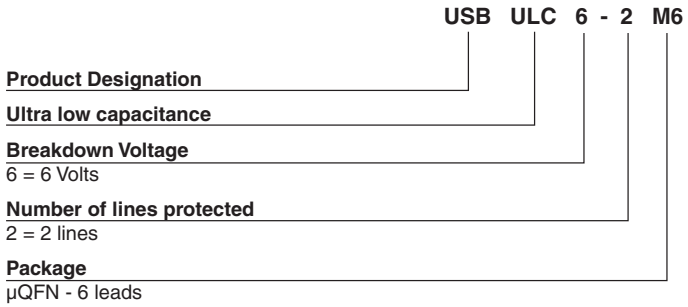
2 Application example

Figure 13. One differential line



3 Ordering information scheme

Figure 14. Ordering information scheme



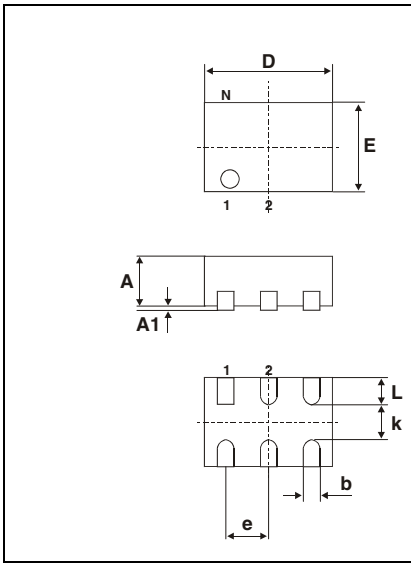
4 Package information

- Epoxy meets UL94, V0

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are Lead-free. The category of second level Interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 3. Micro QFN 1.45x1.00 6L dimensions

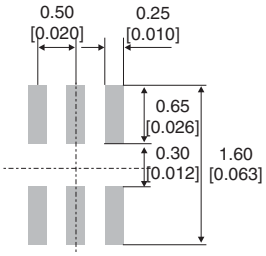


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	0.02	0.05	0.000	0.001	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
D(1)		1.45			0.057	
E(1)		1.00			0.039	
e(2)		0.50			0.020	
K	0.20			0.008		
L	0.30	0.35	0.40	0.012	0.014	0.016

1. ± 0.1 mm
2. ± 0.05 mm

Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

Figure 15. Footprint dimensions in mm [inches]

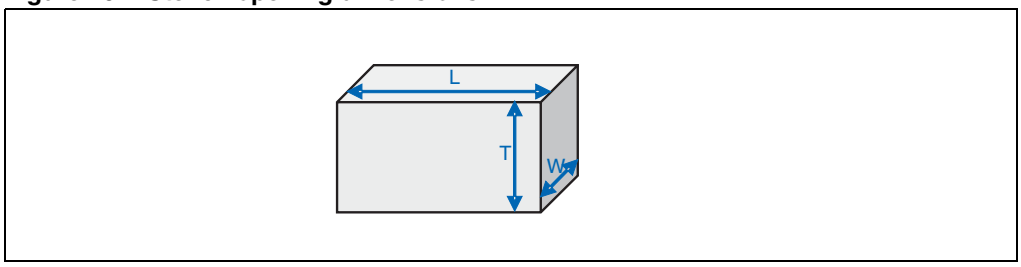


5 Recommendation on PCB assembly

5.1 Stencil opening design

1. General recommendation on stencil opening design
   a) Stencil opening dimensions: L (Length), W (Width), T (Thickness)

Figure 16. Stencil opening dimensions.



   b) General Design Rule

   Stencil thickness (T) = 75 ~ 125 µm

$$\text{Aspect Ratio} = \frac{W}{T} \geq 1.5$$

$$\text{Aspect Area} = \frac{L \times W}{2T(L + W)} \geq 0.66$$

2. Reference design
   a) Stencil opening thickness: 100 µm
   b) Stencil opening for leads: Opening to footprint ratio is 90%.

5.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed
4. Solder paste with fine particles: powder particle size is 20-45 µm.

5.3 Placement

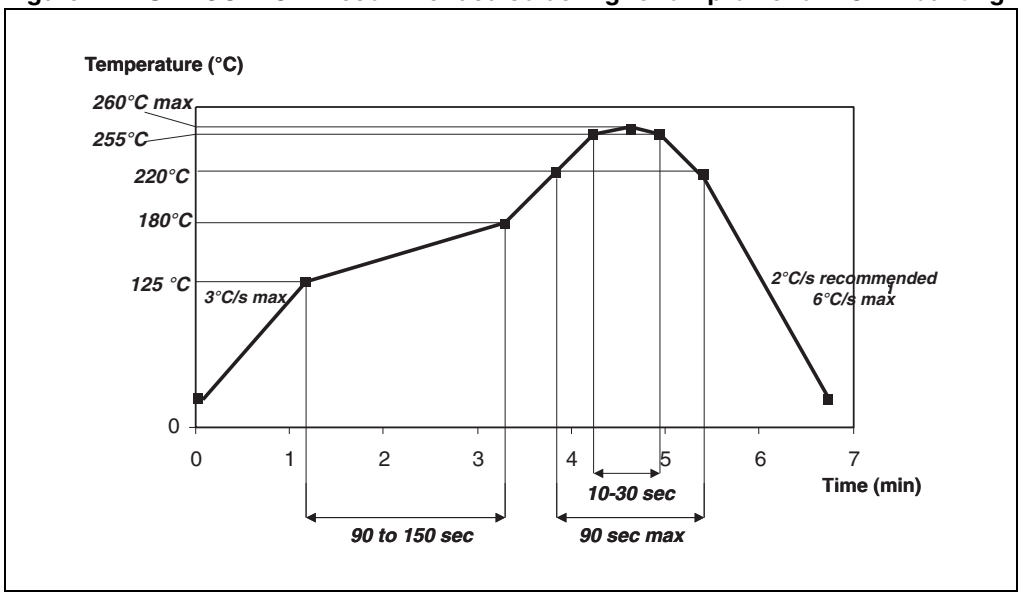
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ± 0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

5.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. The symmetrical layout is recommended, in case any tilt phenomena caused by asymmetrical solder paste amount due to the solder flow away.

5.5 Reflow profile

Figure 17. ST ECOPACK® recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

6 Ordering information

Table 4. Ordering information

Order code	Marking	Package	Weight	Base qty	Delivery mode
USBULC6-2M6	T(1)	µQFN	2.2 mg	3000	Tape and reel

1. The marking can be rotated by 90° to diferentiate assembly location

7 Revision history

Table 5. Document revision history

Date	Revision	Description of changes
29-Nov-2007	1	First issue

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